Guest Editorial: Special Issue on New Trends in Smart Chips and Smart Hardware

MACHINE learning and computational intelligence, which are key to artificial intelligence, have attracted intensive attention in the past years. Although machine learning applications (especially those based on deep learning techniques) have been widely explored and deployed successfully recently, most implementations are based on large training datasets and expensive computing environments (especially in cloud servers). These may hinder the potential wide deployment of machine learning techniques in the emerging Internet of Things (IoT). Although the ongoing wave of artificial intelligence focuses more on big data analysis and cloud intelligence, the next peak of machine learning and computational intelligence technologies will most likely be in the area of IoT. Low power and low latency smart chips and smart hardware may finally transform a variety of things into intelligent components of the IoT, and thus enable us to move into the new era of pervasive learning and pervasive intelligence. Recent progress in machine learning theory, biological learning, neuroscience, CMOS and post-CMOS devices (e.g., memristive devices) could have a significant impact on smart chips and smart hardware for future machine learning and computational intelligence applications.

This special issue aims to promote novel research investigations in low power and low latency of smart chips and smart hardware for machine learning and biologically-plausible learning. After rigorous review, three papers on hardware implementation of biologically inspired learning models, in particular, neuromorphic architecture of Hierarchical Temporal Memory (HTM), memristive paradigm of Extreme Learning Machines (ELM), and FPGA implementations of Gaussian Wilson-Cowan neocortex model have been finally accepted for inclusion in this special issue.

Hierarchical temporal memory (HTM) is a biologically inspired model of machine learning and computational intelligence. Generally speaking, HTM is based on the interaction of pyramidal neurons in the neocortex of animal brains. It has good promise in invariant representations of spatiotemporal input streams. Zyarah *et al*. propose a full-scale HTM architecture for both the spatial pooler and temporal memory. Synthetic synapse design is proposed to address the potential and dynamic interconnections occurring during learning. The architecture is interweaved with parallel cells and columns that enable high processing speed for the HTM. The proposed hardware architecture achieves 1364 times speedup over the software realization and the power consumed can be as low as 1.39 mW per cell.

Extreme Learning Machines (ELM) have become popular in the past 10 years. ELM is not only efficient in small to medium sized applications, but also showcases the basic learning theories in animal brains. Liang, *et al.* propose a neuromorphic computing paradigm implementation (through memristor) for ELM by simulating the biological synapses with memristors and combining the memory property of memristor with the high efficiency processing ability in ELM. The ELM network weights are represented through the memristive conductance values. The conductance values (network weights) are updated through tuning the voltages. Preliminary experimental results show that the memristor-based ELM achieves the same level of performance as its traditional software counterpart in two benchmark datasets. Thus, this paper shows the good potential for ELM to be implemented in neuromorphic computation paradigms.

GPU has been one of the main computing forces for the current wave of artificial intelligence, especially for cloud intelligence. However, FPGA tends to become a good alternative platform for *edge* learning. Gomar and Admadi study the hardware implementation feasibility of Gaussian Wilson-Cowan model, one of the well-known population-based models which represents neuronal functionality in the neocortex. The hardware model is investigated from both dynamical and timing behavior point of view. The experimental evaluations indicate that the hardware model (implemented in an FPGA board) is able to reproduce the dynamical bifurcations as the original model is capable of.

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Hao Yu has been a senior research staff at Berkeley Design Automation (BDA) since 2006, one of top-100 start-ups selected by Red-herrings at Silicon Valley. Since October 2009, he has been an Assistant Professor with the School of Electrical and Electronic Engineering, and also an Area Director of VIRTUS/VALENS Centre of Excellence, Nanyang Technological University, Singapore. He has 152 peer-reviewed and referred publications. He is an Associate Editor for the *Journal of Low Power Electronics*. His main research interest is about the emerging technology and architecture for big-data computing and communication such as 3D-IC, THz communication, and non-volatile memory. His industry work at BDA is also recognized with an EDN magazine innovation award and multi-million venture capital funding.