

Practical Design and Evaluation of a 1 kW PFC Power Supply Based on Reduced Redundant Power Processing Principle

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Abstract—Using the reduced redundant power processing (R^2P^2) principle, a single-phase power-factor correction (PFC) power supply can achieve a higher overall efficiency as a result of the use of a noncascading structure that involves less repeated processing of the input power. This paper investigates a single-phase noncascading PFC power supply based on the R^2P^2 principle. The circuit employs a current-fed full-bridge converter as the PFC preregulator, and a buck–boost converter as the voltage regulator. This paper addresses the design of this noncascading PFC power supply and in particular the relationships between the gained efficiency, the transient response and the size of the energy storage. Experimental results obtained from a 1 kW laboratory prototype are presented.

Index Terms—Buck–boost converter, continuous conduction mode (CCM), current-fed full-bridge converter, noncascading structure, power factor correction (PFC).

I. INTRODUCTION

LOW INPUT current harmonic distortion is an essential requirement of ac–dc power supplies that derive power directly from the ac mains [1], [2]. Despite its simplicity, the conventional design of ac–dc power supplies based on cascading a power-factor correction (PFC) preregulator and a voltage regulator incurs an efficiency penalty due to redundant power processing, as illustrated in the power flow diagram shown in Fig. 1. To improve the overall efficiency, many noncascading structures have been proposed for ac–dc power supplies [3]–[10]. These noncascading PFC power supplies allow part of the input power to be processed by only one power stage, thereby reducing the amount of power redundantly processed by the two constituent power converters. A unified solution for generating the noncascading PFC power supplies based on the reduced redundant power processing (R^2P^2) principle has been presented in Tse *et al.* [11], [12]. While the basic theoretical considerations and circuit synthesis procedures were reported [11], [12], practical design considerations and evaluations for high power applications have not been addressed. In this paper, we consider the practical design and implementation of a specific noncascading power flow structure of PFC power supplies,

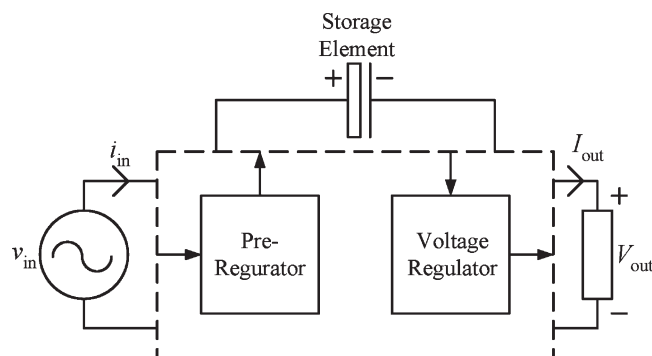


Fig. 1. Power flow diagram for the classical PFC power supply. All power is processed by the two stages serially.

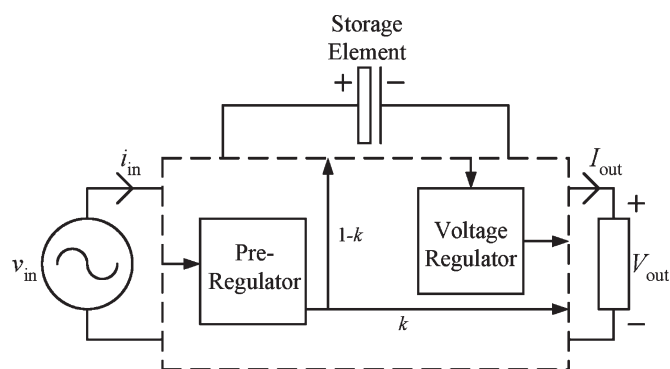


Fig. 2. Power flow diagram for the noncascading PFC power supply under study, where k is the fraction of power that goes to the output directly after being processed by the preregulator.

which is shown in Fig. 2. Specifically, the noncascading PFC power supply studied in this paper belongs to the Type I–IIIB configuration described in [11] and [12]. Other noncascading power supplies have also been reported elsewhere [7]–[10]. However, in much of the previous studies, the focus was on one particular performance area. For instance, the main focus in [7]–[9] was on the efficiency improvement of the power supply, whereas the main focus in [10] was to reduce the voltage of the energy storage capacitor.

Our objective in this paper, however, is to provide a detailed consideration of several practical issues related to the design of a noncascading ac–dc PFC power supply. Specifically, we will examine the relationships between the gained efficiency, the load transient response and the energy storage requirement.

The power supply under study consists of a current-fed full-bridge converter which serves as the PFC preregulator and a

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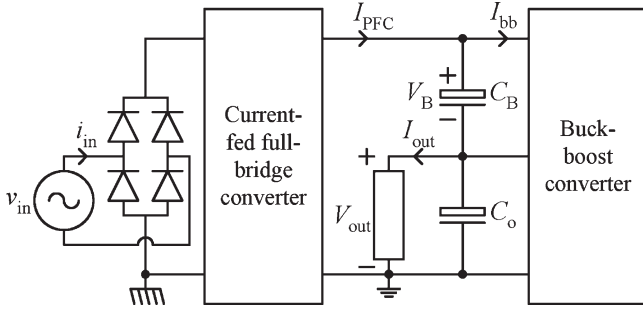


Fig. 3. Schematic diagram of the noncascading PFC power supply.

buck–boost converter which acts as the voltage regulator. Both regulators are operated in continuous conduction mode (CCM). The advantage of CCM is that the current stress of the devices of the regulators is relatively low, and hence is more suitable for high power applications.

Section II shows the theoretical analysis of an ac–dc power supply that adopts the aforementioned noncascading structure and the analysis includes deriving the relationships between the efficiency gain, the load transient response and the size of the energy storage. Section III presents some practical problems related to circuit implementation of the PFC power supply. In Section IV, some experimental results under various operating conditions will be given. Finally, a conclusion is given in Section V.

II. THEORETICAL ANALYSIS OF THE NONCASCADING PFC POWER SUPPLY

The schematic of the PFC power supply under study is shown in Fig. 3. It consists of a current-fed full-bridge converter and a buck–boost converter connected in a noncascading fashion. To maintain power balance, a low-frequency storage element is required to buffer the difference between the instantaneous input power and output power. Capacitor C_B and C_o are connected serially. The series combination forms the loading for the current-fed full-bridge converter. Thus, a portion of the output energy from the converter is transferred directly to the output since C_o is in parallel with the load. Because of the tight regulation of the buck–boost converter, the voltage of C_o is relatively free of low-frequency ripple. Therefore, as far as the current-fed full-bridge converter is concerned, the capacitance of C_o can be considered practically as a voltage source and only C_B serves as an energy storage element. Furthermore, the dc output voltage of the current-fed full-bridge converter must be larger or equal to V_{out} to meet the load voltage regulation requirement.

A. Split Factor Versus Efficiency Gain

One crucial parameter in the design of a noncascading ac–dc PFC power supply is the fraction of input power which is processed only once, i.e., by only one converter [11], [12]. The theoretical efficiency of the noncascading PFC power supply can be evaluated by the following equation:

$$\begin{aligned}\eta_{\text{noncascading}} &= (1 - k)\eta_{P1}\eta_{P2} + k\eta_{P1} \\ &= \eta_{P1}\eta_{P2} + k\eta_{P1}(1 - \eta_{P2})\end{aligned}\quad (1)$$

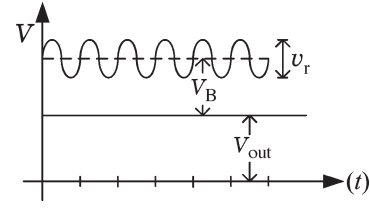


Fig. 4. Ideal voltage waveforms of the noncascading PFC power supply.

where η_{P1} and η_{P2} are the efficiencies of the preregulator and the voltage regulator, respectively, and k is the split factor which is defined as the ratio at which the amount of the input power is split at the output of the preregulator to the output load. The efficiency gain of the noncascading power supply is $k\eta_{P1}(1 - \eta_{P2})$. Obviously, the overall efficiency depends on the preregulator efficiency since the total input power from the ac mains must be processed by the preregulator before it is transferred to the load or the voltage regulator.

B. Split Factor Versus Transient Response

In the noncascading power supply, k affects the efficiency gain and the load transient response. The total current harmonic distortion is independent of this factor due to the input current being fully processed by the PFC preregulator. Referring to Figs. 3 and 4, we can write

$$P_{\text{PFC}} = I_{\text{PFC}} \left(\frac{v_r}{2} \sin 2\omega t + V_B + V_{out} \right) \quad (2)$$

$$P_{\text{direct}} = I_{\text{PFC}} V_{out}. \quad (3)$$

From (2) and (3), we have

$$P_{\text{direct}} = \frac{V_{out}}{\frac{v_r}{2} \sin 2\omega t + V_B + V_{out}} P_{\text{PFC}} \quad (4)$$

where P_{PFC} and I_{PFC} are the output power and the output current of the current-fed full-bridge converter, and P_{direct} denotes the amount of output power of the converter directly transferred to the load. Also, $(v_r \sin 2\omega t)/2$ and V_B represent the low-frequency ripple voltage and the static voltage of C_B , respectively, and ω is the angular frequency of the ac mains. Therefore, the low-frequency ripple voltage affects k according to

$$k(t) = \frac{V_{out}}{\frac{v_r}{2} \sin 2\omega t + V_B + V_{out}}, \quad \text{for } 0 < k(t) < 1. \quad (5)$$

Moreover, for calculating the overall efficiency, $k(t)$ can be averaged over the ac mains period and represented by

$$\langle k(t) \rangle_T = \frac{V_{out}}{V_B + V_{out}} \quad (6)$$

which is consistent with the results reported by Garcia *et al.* [7], [8]. Furthermore, according to (5), the input voltage of the buck–boost converter is determined by V_{out} and $k(t)$. Now, if we ignore the effect of the controller on the load transient

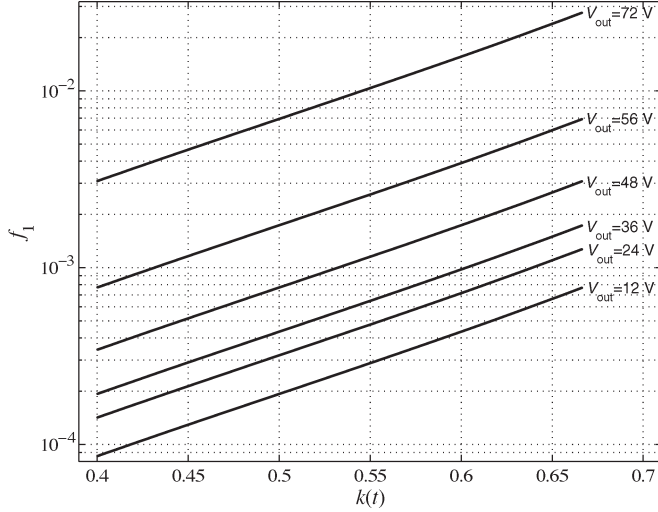


Fig. 5. Normalized transient response, f_1 , versus the split factor k for different output voltages and the static voltage. $\langle k(t) \rangle_T$ is equal to 0.5.

response, the transient response time is purely controlled by the input voltage of the voltage regulator. From Fig. 3, we have

$$\frac{\Delta I_{bb}}{\Delta t} = \frac{\frac{v_r}{2} \sin 2\omega t + V_B}{L_2} \quad (7)$$

where ΔI_{bb} is the change in input current of the buck–boost converter at the load transient period, Δt is the transient response time, and L_2 is the inductance of the converter. Assume that the duty cycle is unity in the transient period. Since the current-fed full-bridge converter is controlled by a low bandwidth (one-fifth of the ac mains frequency) voltage control loop to maintain PFC [13], only the buck–boost converter would provide transient power to the load. Suppose the load changes from 10% to 90% of the full load condition during transient. Then, we have

$$\Delta I_{bb} = \frac{(0.9P_{out} - 0.1P_{out})}{\eta_{P2} \left(\frac{v_r}{2} \sin 2\omega t + V_B \right)} \quad (8)$$

where P_{out} is the full output power drawn from the load. Therefore, putting (8) in (7), the transient response time is expressed as

$$\Delta t = \frac{(0.9 - 0.1)P_{out}L_2}{\eta_{P2} \left(\frac{v_r}{2} \sin 2\omega t + V_B \right)^2} \quad (9)$$

$$= \frac{(0.9 - 0.1)P_{out}L_2k^2(t)}{\eta_{P2} (V_{out} - V_{out}k(t))^2}. \quad (10)$$

Referring to (5), the low-frequency ripple voltage is one of the parameters that affect the load transient response. Fig. 5 shows the simulation results based on (5) and (10) to illustrate the relation between the transient time and the split factor for different output voltages. For brevity, the transient response time can be normalized as

$$f_1 = \frac{k^2(t)}{(V_{out} - V_{out}k(t))^2} \quad (11)$$

where f_1 is in proportion to the transient response time. In Fig. 5, $\langle k(t) \rangle_T$ is fixed at 0.5, and v_r is equal to V_B . The transient response time of the voltage regulator increases as $k(t)$ and V_{out} increase. Evidently, the split factor $k(t)$ not only controls the efficiency gain of the power supply, but also affects the load transient response of the voltage regulator.

C. Split Factor Versus Size of the Storage Element

The storage element plays an important role in any ac–dc PFC power supplies. Suppose the current-fed full-bridge converter delivers a constant output power, P_{P1} . Then, the power drawn from the ac mains with unity power factor is

$$P_{mains} = \frac{P_{P1}(1 - \sin 2\omega t)}{\eta_{P1}}. \quad (12)$$

The minimum stored energy necessary for achieving unity power factor is equal to the difference between the energy consumed by the constant power load and the energy delivered by the ac mains during one-quarter of its period $\pi/2\omega$ starting with zero energy. The energy consumed by the load during $0 < t < \pi/2\omega$ is

$$E_{dc} = \frac{P_{P1}}{\eta_{P1}} \frac{\pi}{2\omega}. \quad (13)$$

The energy delivered by the ac mains during $0 < t < \pi/2\omega$ is

$$E_{ac} = \int_0^{\frac{\pi}{2\omega}} \frac{P_{P1}}{\eta_{P1}} (1 - \sin 2\omega t) dt = \frac{P_{P1}}{\eta_{P1}} \left(\frac{\pi}{2\omega} - \frac{1}{\omega} \right). \quad (14)$$

The minimum stored energy of the storage element is the difference between the two energies, i.e.,

$$E_{CB_{min}} = E_{dc} - E_{ac} = \frac{P_{P1}}{\eta_{P1}\omega}. \quad (15)$$

In the noncascading PFC power supply, the storage element is a capacitor C_B . Referring to Fig. 4, the energy stored in the capacitor is

$$E_{CB} = \frac{1}{2}C_B \left(\left(V_B + \frac{v_r}{2} \right)^2 - \left(V_B - \frac{v_r}{2} \right)^2 \right) = C_B V_B v_r. \quad (16)$$

Using (15) and (16), we get

$$v_r = \frac{P_{P1}}{\eta_{P1}\omega C_B V_B}. \quad (17)$$

Thus, the voltage ripple amplitude can be reduced by using a large capacitor under a high static stress. In the case of the noncascading PFC power supply, to maintain the unity-power-factor operation and output voltage regulation, the size of the storage capacitance required is minimal if the capacitor voltage is allowed to vary at twice the value of the static voltage during

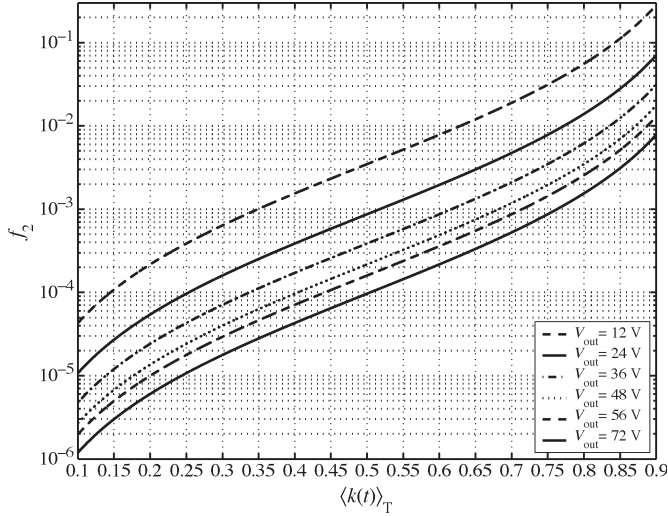


Fig. 6. Normalized minimum storage capacitance, f_2 , versus $\langle k(t) \rangle_T$ for different output voltages.

each half of the ac mains period, i.e., $v_r = 2V_B$. The minimum size of storage capacitance required is

$$C_{B_{\min}} = \frac{P_{P1}}{\eta_{P1} \omega 2V_B^2}. \quad (18)$$

The normalized minimum capacitance can be written as

$$f_2 = \frac{1}{2V_B^2}. \quad (19)$$

According to (5) and (19), the relation between the normalized minimum capacitance f_2 and $\langle k(t) \rangle_T$ at different output voltages are shown graphically in Fig. 6. The minimum capacitance required increases with $\langle k(t) \rangle_T$ and V_{out} , as V_B depends on these two factors. In Fig. 6, we maintain v_r at twice the value of V_B to achieve the condition for minimum storage capacitance. However, in practice, the ripple voltage should be kept as small as possible to provide a stable input voltage source for the voltage regulator operation. Moreover, to maintain a high power factor, the preregulator can only provide a slow output voltage transient response; the buffer energy stored in C_B becomes a critical parameter. The minimum energy stored in C_B is calculated by

$$\text{Energy} = \frac{1}{2} C_B \left(V_B - \frac{v_r}{2} \right)^2 = \frac{P_{out}}{\eta_{P2}} \times \text{Time} \quad (20)$$

where “Time” is the response time of the preregulator voltage control loop. To ensure that the transient response of this noncascading PFC power supply is unaffected by the slow voltage transient response of the preregulator, the energy stored in C_B must be capable of supporting all the transient output power at least within “Time.” In general, the capacitance of the noncascading power supply requires a larger value than that of the classical power supply because the allowable voltage ripple and the static voltage of C_B are limited by V_{out} and $\langle k(t) \rangle_T$.

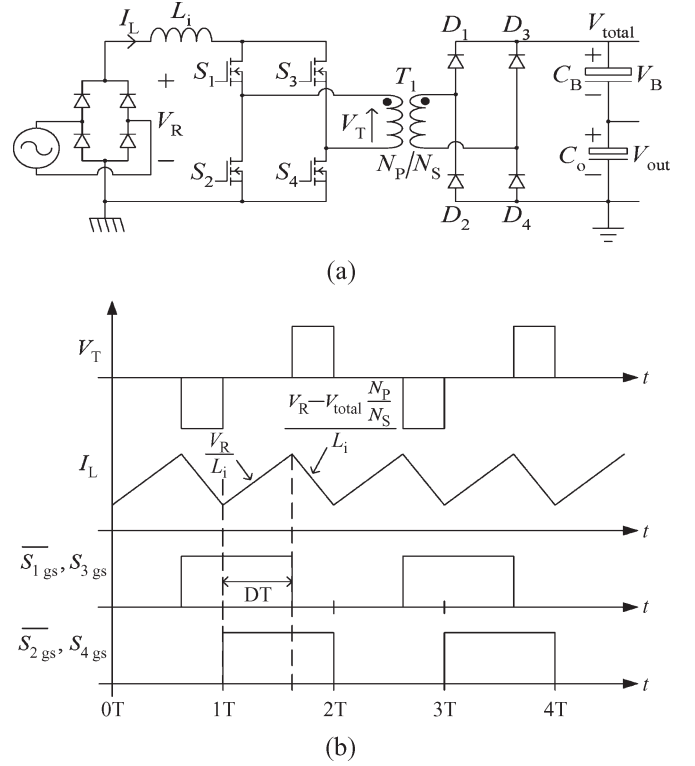


Fig. 7. Current-fed full-bridge converter. (a) Simplified circuit. (b) Gate timing diagram with corresponding waveforms.

III. CIRCUIT OVERVIEW

A. Preregulator Stage

In this paper, we use the current-fed full-bridge converter as the PFC preregulator [4], [14]–[16]. The input current of this converter can be fully controlled to achieve the required PFC function. In addition, the size and cost of the input boost inductor can be reduced due to its frequency-doubling effect. Also, the transformer provides galvanic isolation and steps down the output voltage. However, the leakage inductance of the transformer generates high voltage spikes on the power switches, when the switches are turned off. A simple method to suppress the voltage spikes is to use a passive or active snubber circuit at the expense of some power loss.

The simplified circuit of the current-fed full-bridge converter is shown in Fig. 7(a). The set of waveforms that relate the ideal gate timing with the corresponding inductor current and transformer voltage is shown in Fig. 7(b). It is easy to see that the operation of this converter resembles that of a typical boost converter. The conversion ratio is controlled by the phase difference between S_1 and S_2 . It can be easily derived by applying the principle of volt-second balance to the inductor current waveform, i.e.,

$$\frac{V_R}{L_i} DT = - \left(\frac{V_R - V_{total} \frac{N_p}{N_s}}{L_i} \right) (1 - D)T. \quad (21)$$

Thus, the conversion ratio is

$$\frac{V_{total}}{V_R} = \frac{N_s}{N_p} \frac{1}{(1 - D)} \quad (22)$$

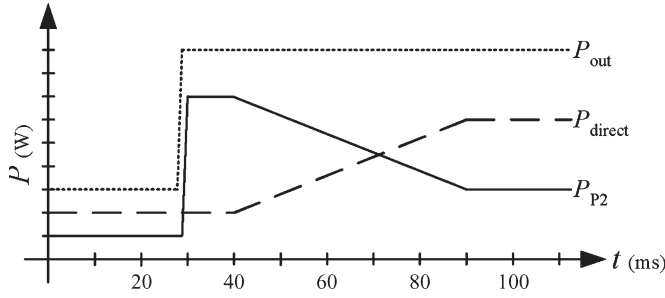


Fig. 8. Simplified power sharing waveforms for the voltage regulator of the noncascading power supply at load transient period for $\langle k(t) \rangle_T = 0.67$.

which is similar to that of a typical boost converter conversion ratio with an additional factor of N_s/N_p due to the transformer turns ratio.

B. Voltage Regulator Stage

Based on the description in Section II, the voltage regulator processes only part of the total output power in the steady-state loading condition. However, during load transient, the buck-boost converter is required to deliver the total transient output power due to the slow voltage control loop of the preregulator. Fig. 8 shows the relation between the power, P_{direct} , drawn from the ac mains through the preregulator to the load and the power, P_{P2} , drawn from C_B through the voltage regulator to the load. The power handled by the voltage regulator is dependent on $\langle k(t) \rangle_T$ and the load transient power level. While the semiconductor devices of the voltage regulator are selected to operate for the maximum output power, the thermal design of the voltage regulator would only need to process part of the total output power, i.e., depending on the split factor. The buck-boost converter, the Ćuk converter and any isolated converters [8], [12] are suitable candidates for the voltage regulator because, in this noncascading configuration, the negative input terminal must be connected to the positive output terminal according to Fig. 3. The buck-boost converter is chosen here because of the simple control circuit design.

The buck-boost converter is required to handle power according to the split factor $\langle k(t) \rangle_T$ and the transient load power level. During load transient, as mentioned earlier, the converter has to provide the total transient output power for a short duration. Our design employs the zero-voltage-transition (ZVT) technique [17], in which the voltage stress of switching devices is clamped at a level equal to $V_B + V_{out}$. The simplified voltage regulator is shown in Fig. 9. The basic components of the buck-boost converter include S_5 , D_5 , and L_2 . ZVT is achieved by an auxiliary switch, S_6 , a power diode, D_6 , and a resonant network, which consists of L_r and C_r . This technique can provide zero-voltage switching in S_5 , and also reduce power loss in D_5 due to a longer reverse recovery time.

IV. EXPERIMENTAL VERIFICATION

A. Implementation

A laboratory prototype has been constructed to meet the following major design specifications: the input voltage is 220 V_{ac}, the ac mains frequency is 50 Hz, the voltage of the

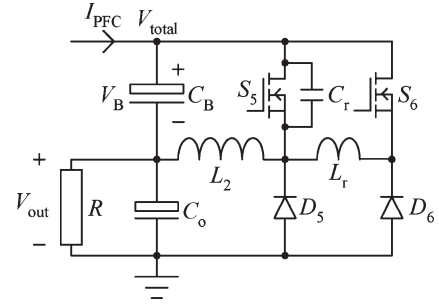


Fig. 9. Simplified schematic circuit of the buck-boost converter using ZVT technique.

TABLE I
LIST OF COMPONENTS FOR THE CURRENT-FED FULL-BRIDGE CONVERTER

Designator	Part No./Value
L_1	500 μ H
BR_1	20ETF10 \times 4
S_1, S_2, S_3, S_4	IXFK 27N80
D_1, D_2, D_3, D_4	DESP 30-03A
T_1 Core	ETD 54 Philips 3C90
T_1 Magnetizing Inductance	18 mH
T_1 Primary Leakage Inductance	9.4 μ H
T_1 Primary Winding	58 T
T_1 Secondary Winding	21 T
C_{S1}, C_{S2}	4.7 nF, 2 kV
R_{S1}, R_{S2}	100 Ω , 25 W
D_{S1}, D_{S2}	MUR4100

TABLE II
LIST OF COMPONENTS FOR THE BUCK-BOOST CONVERTER

Designator	Part No./Value
S_5	IXFK73N30
S_6	IXFK48N50
D_5	APT30D30
D_6, D_7, D_8	BYV29-400
L_2	100 μ H
L_r	10 μ H
C_B	2700 μ F \times 5, 160 V
C_0	680 μ F \times 4, 100 V
C_r	2.2 nF, 630 V
C_{S3}	2 nF, 1 kV
R_{S3}	360 Ω , 2 W
D_{S3}	MUR460

energy storage element is 83 V_{dc}, the output voltage is 72 V_{dc}, the output power is 1 kW, and the switching frequency for both regulators is 50 kHz. The list of components of the preregulator and the voltage regulator are shown in Tables I and II, respectively. Fig. 10 shows the implemented schematic diagram of the noncascading PFC power supply with the control circuitries. Two passive snubber circuits are added in the primary side to suppress the primary switch voltage stress. In the voltage regulator, to prevent the parasitic ringing between L_r and the output capacitor of S_6 , two diodes, D_7 and D_8 , are added. A turn-off snubber circuit is also attached in the secondary side power switch, S_5 , to clamp the voltage stress.

Average current mode control based on the PFC controller UC3854A is employed to control the current-fed full-bridge converter. There are four active switches, which have to be controlled to realize the PFC function. Thus, additional logic circuits are required to generate the required gating pulses according to Fig. 7(b). For simplification, the circuit design

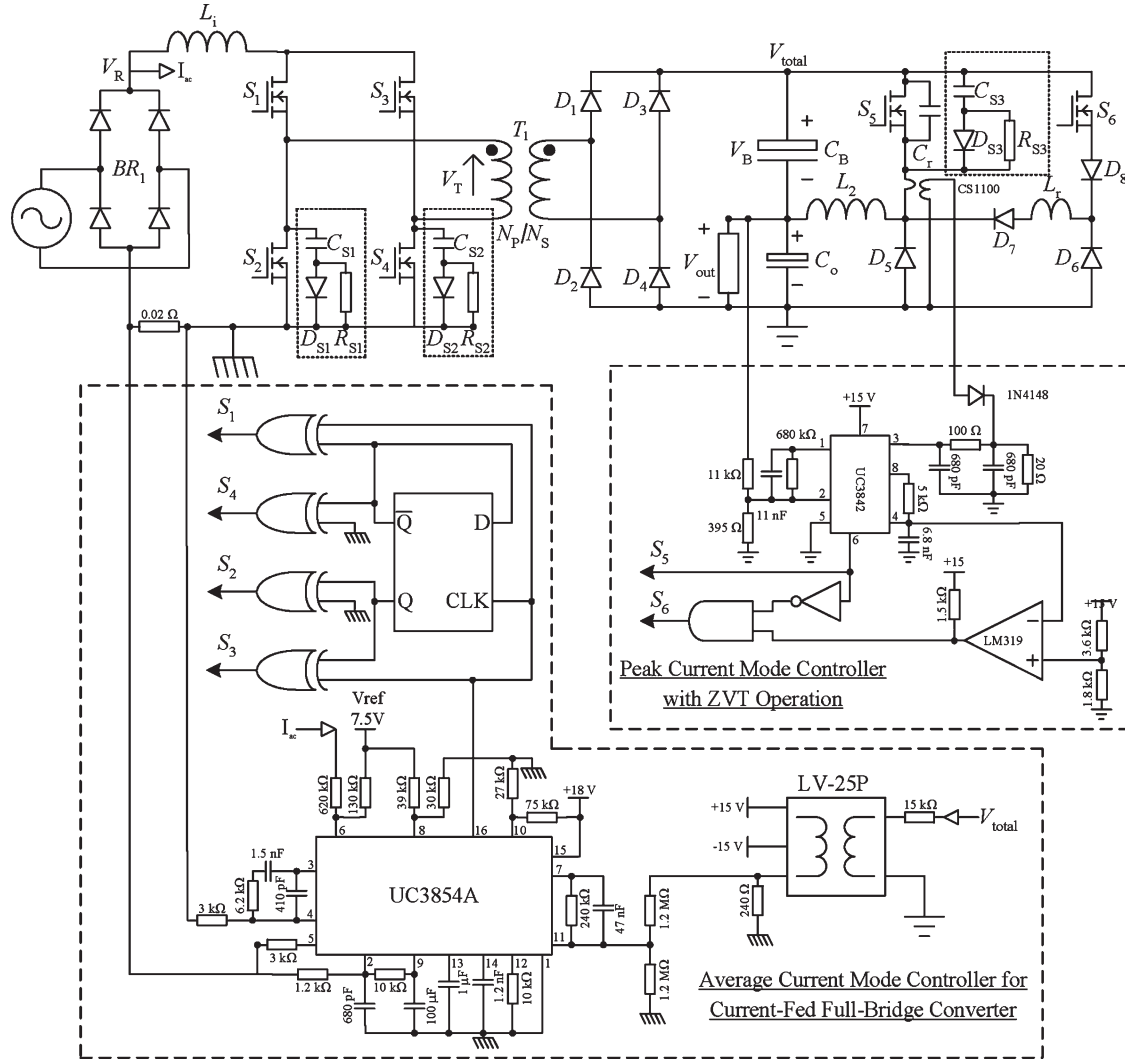


Fig. 10. Schematic diagram of the experimental noncascading PFC power supply prototype.

peak current mode control based on UC3842 is employed in the buck–boost converter to provide the voltage regulation. The subharmonic oscillation will occur when the converter duty cycle is larger than 0.5. Therefore, 0.46 is an appropriate value of $\langle k(t) \rangle_T$ to keep the duty cycle below 0.5 for this circuit. If $k(t)$ is larger than 0.5, the average current mode control can be employed in the buck–boost converter but the control circuit is relatively complicated. The gate signal of the auxiliary switch for ZVT operation is attained by a voltage comparator with a simple logic circuit.

B. Experimental Results

In this section, the advantages of the noncascading power supply are demonstrated experimentally. Fig. 11 shows two overall efficiency curves to confirm the efficiency formulas (1) and (6). The measured overall efficiency of the power supply under study is 87% at 1 kW output power. The main power loss is in the snubber circuits of the preregulator. Fig. 12 shows the efficiency comparison of the noncascaded connection with the

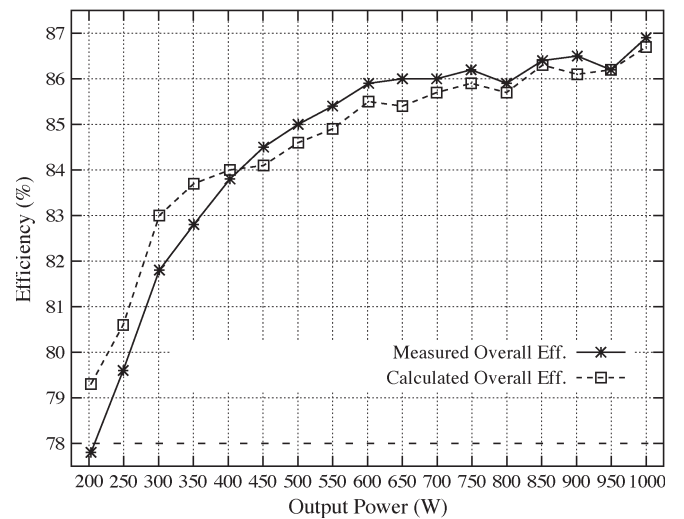


Fig. 11. Efficiency versus output power from 200 W to 1 kW for $k = 0.46$, confirming the efficiency formulas [(1) and (6)]. Calculated values are based on efficiency formula and measured values of η_{P1} and η_{P2} . Measured values are from direct measurement of the overall efficiency.

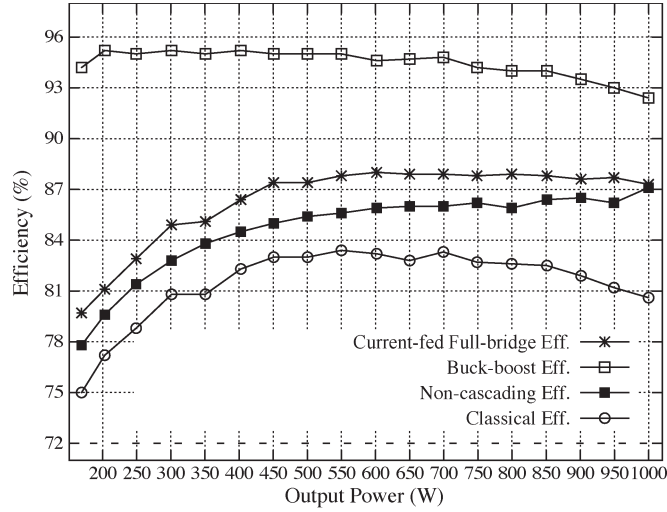


Fig. 12. Efficiency comparison showing improved overall efficiency of the noncascading structure, for $k = 0.46$, over the classical connection. The top two curves are the efficiencies of the individual converters. The lower two curves are the overall efficiencies of the noncascading and conventional power supplies.

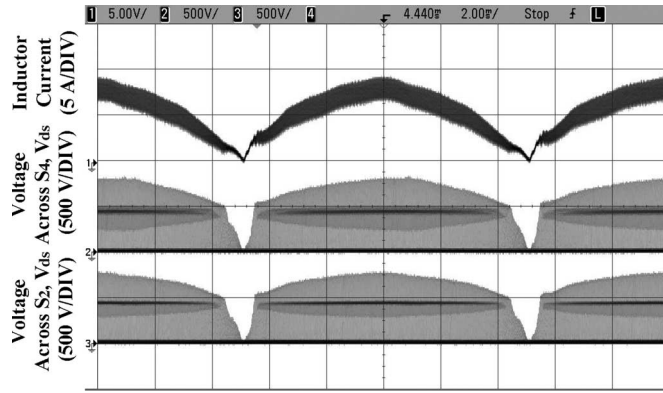


Fig. 13. Measured waveforms of the preregulator: input inductor current (upper trace), V_{ds} of S_4 (middle trace), and V_{ds} of S_2 (lower trace). Time scale is 2 ms/div.

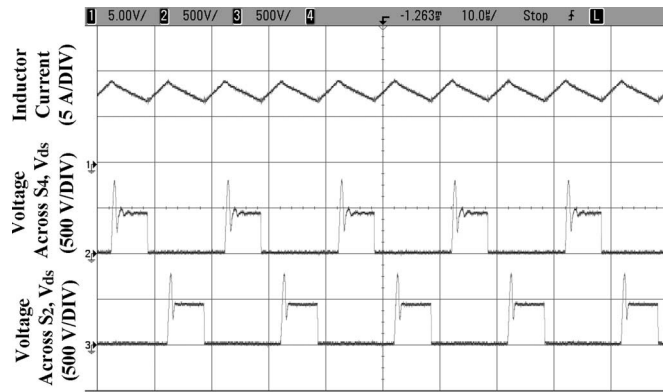


Fig. 14. Measured waveforms of the preregulator: input inductor current (upper trace), V_{ds} of S_4 (middle trace), and V_{ds} of S_2 (lower trace). Time scale is 10 μ s/div.

classical two-stage cascade structure. The circuit is tested over a power range from 170 W to 1 kW, as the buck–boost converter is designed to provide 1 kW output power for a short duration.

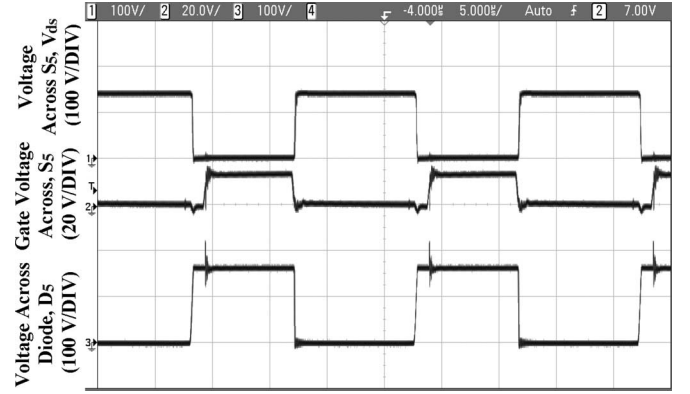


Fig. 15. Measured waveforms of the voltage regulator with ZVT operation: V_{ds} of S_5 (upper trace), V_{gs} of S_5 (middle trace) and the voltage across D_5 . Time scale is 5 μ s/div.

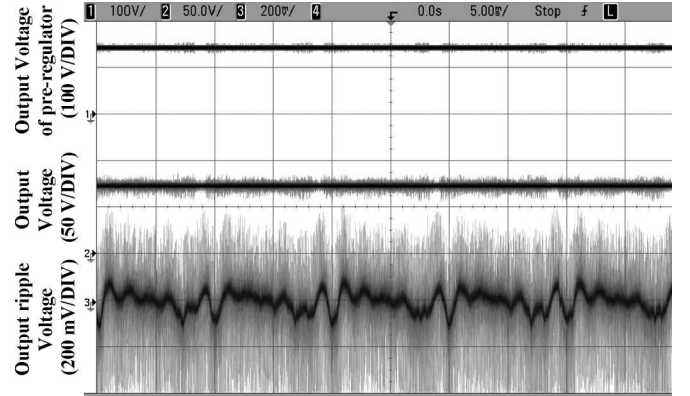


Fig. 16. Measured waveforms of the output voltage of preregulator (upper trace), output voltage (middle trace) and ripple voltage (lower trace). Time scale is 5 ms/div.

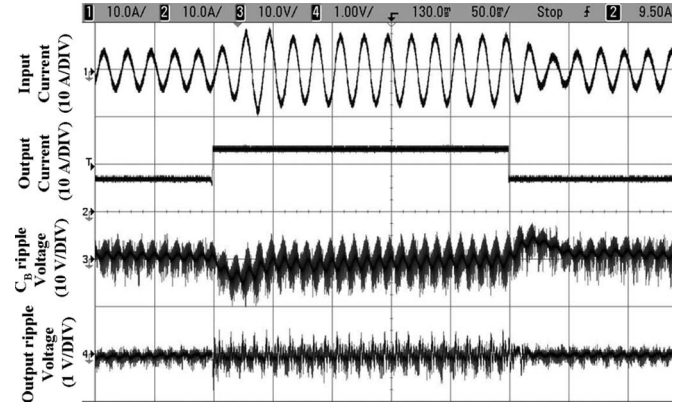


Fig. 17. Measured waveforms of the filtered input current of preregulator (upper trace), load current (middle trace), C_B ripple voltage (third trace), and output ripple voltage (lower trace). Time scale is 50 ms/div.

The efficiency gain of the noncascaded connection is around 6% at 1 kW, compared with the classical (cascade) connection.

Figs. 13 and 14 show the waveforms of the current-fed full-bridge converter at 1 kW output power. The upper trace is the current of the inductor, L_i . The middle trace and the lower trace are V_{ds} of S_2 and V_{ds} of S_4 , respectively. The voltage spikes on the switches are around 750 V at full load condition. The spikes are generated by a resonant network, which is composed of

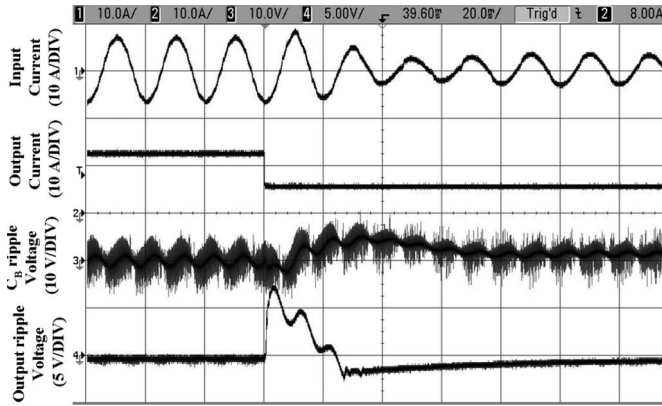


Fig. 18. Measured waveforms under a negative load step at the maximum input power are shown. Filtered input current of preregulator (upper trace), load current (middle trace), C_B ripple voltage (third trace), and output ripple voltage (lower trace). Time scale is 20 ms/div.

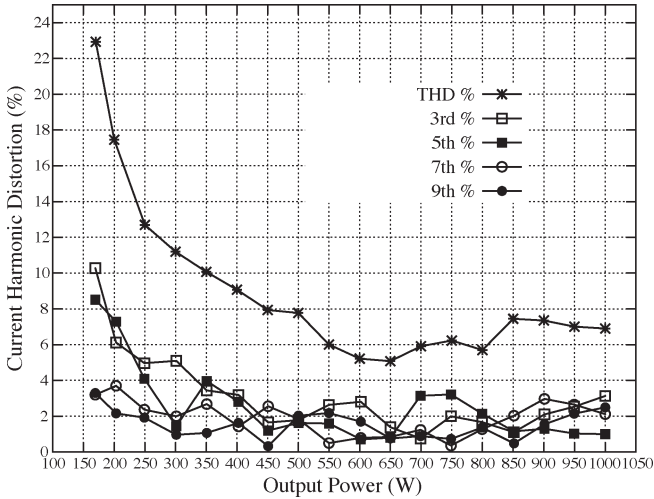


Fig. 19. Measured harmonic distortion versus output power.

the leakage inductance of the power transformer and the output capacitors of the switches.

Fig. 15 shows the voltage waveforms of the major devices of the voltage regulator. The upper trace and the middle trace show that S_5 is operated in zero voltage switching. The lower trace is the voltage waveform of the power diode, D_5 . Fig. 16 shows the different output voltage waveforms of the preregulator and the voltage regulator. Fig. 17 depicts the performance of the noncascading power supply for a step load change from 500 W to 1 kW. Fig. 18 shows the power supply waveforms under a negative load step from 1 kW to 500 W at the maximum input power condition. The output voltage is inevitably overshoot because the output power of the preregulator is controlled by the slow response voltage control loop.

Finally, to verify the PFC function, the harmonic distortions are measured for different output power levels, as shown in Fig. 19. A comparison is made between the maximum permissible harmonic current limits for Class A equipment of EN 61000-3-2:2005 [1] and the noncascading power supply input current at 1 kW power output, as shown in Fig. 20. The input voltage (upper trace) and the filtered input current (lower trace) at full load condition are shown in Fig. 21.

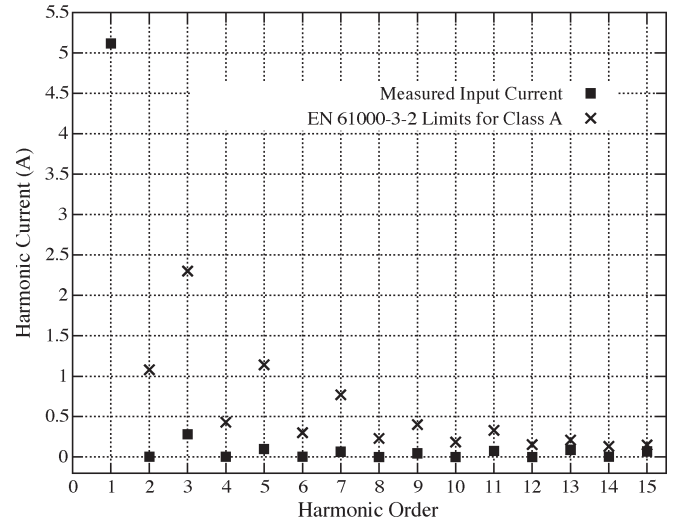


Fig. 20. Harmonic current comparison between the measured input current at 1 kW output and EN 61000-3-2 harmonic current limits for Class A equipment.

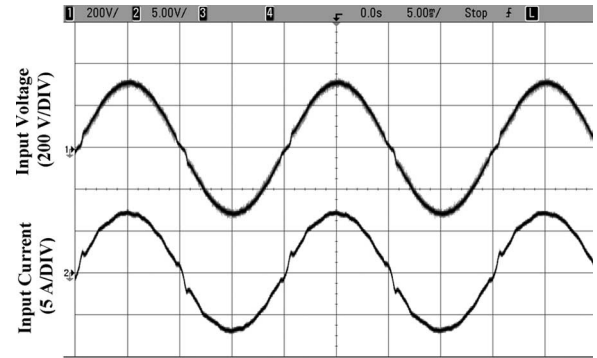


Fig. 21. Measured waveforms of the input voltage (upper trace) and the filtered input current (lower trace) at full load condition. Time scale is 5 ms/div.

Obviously, the overall efficiency of the noncascading PFC power supply is generally improved, but often at a price. The split factor $\langle k(t) \rangle_T$ is one crucial parameter in the design. It affects the overall efficiency, the transient response and the size of the energy storage, as mentioned before. Therefore, care should be taken to select $\langle k(t) \rangle_T$ to optimize the performance of this noncascading PFC power supply according to the specific application concerned.

V. CONCLUSION

In this paper, the practical design constraints of power-factor-correction power supplies that use a noncascading structure have been studied. The results complement the prior study on the topologies and basic synthesis processes, and provide further information about the design of such power supplies. In particular, a 1 kW isolated PFC power supply using a noncascading connection of a current-fed full-bridge converter and a buck-boost converter has been thoroughly investigated. According to the (R^2P^2) principle, the overall efficiency of the noncascading power supply can be improved because part of the output power of the preregulator is transferred directly from the input to the regulated output. This paper presents

some design criteria for this noncascading PFC power supply, which include the relationships between the split factor, the load transient response and the energy storage requirement. The overall efficiency can be improved by increasing the split factor, but the load transient response time and the energy storage requirement will be deteriorated. Furthermore, to maintain the output voltage of the power supply without low frequency ripple voltage, a substantial energy storage is required. Some practical problems related to the implementation of the current-fed full-bridge converter and the buck–boost converter are discussed. A 1 kW experimental prototype has been built with zero-voltage-switching incorporated in the voltage regulator stage. The measured results are presented to validate the analytical prediction.

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