FPGA-Based Real-Time Power Converter Failure Diagnosis for Wind Energy Conversion Systems

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Abstract— **This paper discusses the design, implementation, experimental validation and performances of a FPGA-based real time power converter failure diagnosis for three-leg fault tolerant converter topologies used in Wind Energy Conversion Systems (WECS). The developed approach minimizes the time interval between the fault occurrence and its diagnosis. We demonstrated the possibility to detect a faulty switch in less than 10 µs by using a diagnosis simultaneously based on a "time criterion" and a "voltage criterion". To attain such a short detection time, a FPGA (Field Programmable Gate Array) fully digital implementation is used. The performances of the proposed FPGA-based fault detection method are evaluated for a new fault tolerant back to back converter topology suited for WECS with Doubly Fed Induction Generator (DFIG). We examine the failure diagnosis method and the response of the WECS when one of the power switches of the fault tolerant back to back converter is faulty. The experimental failure diagnosis implementation based on "FPGA in the loop" hardware prototyping verifies the performances of the fault tolerant WECS with DFIG.**

Index Terms— **Field Programmable Gate Array (FPGA), Diagnosis, Fault tolerant, Wind Energy Conversion System.**

NOMENCLATURE

C_{dc}	DC link capacitor.
i_{abcg}	Grid currents.
i_k	Rotor side converter currents.
$i_{k'}$	Grid side converter currents.
J	Total moment of inertia (turbine and DFIG).
L_s, L_r	Stator and rotor inductances.
M	Mutual inductance.
p	Number of pairs of poles.
P_g, Q_g	Active and reactive grid power.
R_f, L_f	Grid side converter filter.
R_s, R_r	Stator and rotor resistances.
S_n	DFIG nominal power.
v_{dc}	Nominal DC voltage.
σ	Leakage factor.

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I. INTRODUCTION

The demand for continuously available electronic power systems is increasing. Power systems are mostly feeding loads requiring non-stop and fault tolerant operation. WECS are typical application cases where the efficient production is directly linked to economic benefits. In variable speed operation, a control method designed to extract maximum power from the turbine and provide constant grid voltage and frequency is required [1]. A wide range of control schemes, varying in cost and complexity, have been investigated [2]. More, many converter topologies have been studied in the literature [3]; most of them implement three-leg power topologies, usually connected together by a DC link and used in rectifier and/or inverter mode [4]. Many current papers studied fault tolerant control of electrical drive [5], [6], [7] or fault detection and diagnosis of rotating machinery [8], [9]. However, to our knowledge, FPGA-based real time power converter failure diagnosis for fault tolerant WECS with electrical machine has never been presented.

WECS are highly sensitive to power switch failure. A sudden failure in one of the power switches decreases system performances and leads to disconnect the system. Moreover, if the fault is not quickly detected and compensated, it can lead to hard failure [6]. Hence, to reduce the failure rate and to prevent unscheduled shutdown, real-time fault detection, isolation and compensation scheme must be adopted.

Recently, the fault mode behaviour, protection and fault tolerant control of three-phase voltage source power converters have been covered in a large number of papers. Most of the methods presented take at least one fundamental period to detect the fault occurrence [7], [10]. There have been also special methods recently developed to minimize the time between fault occurrence and detection. Riberio et al. [11] proposed different techniques for fault detection in three-phase voltage power converter. These techniques are a kind of knowledge based procedure. With these techniques the fault can be detected in one fourth of the fundamental cycle.

This paper discusses the design, implementation, experimental validation and performances of a FPGA-based real time power converter failure diagnosis for three-leg fault tolerant converter topologies used in WECS. The approach introduced in this paper minimizes the time interval between the fault occurrence and its diagnosis. This paper demonstrates the possibility to detect a faulty switch in less than 10 µs by using a new methodology based on a "time criterion" and a "voltage criterion". To attain this short detection time, a FPGA (Field Programmable Gate Array) is used. The proposed fault detection method is implemented using a FPGA and evaluated

in the application case of a back to back converter used in a new fault tolerant WECS topology with Doubly Fed Induction Generator (DFIG). We examine the proposed failure diagnosis method and the response of the WECS when one of the power switches is faulty. Two cases are studied: the fault can either occur over the Grid Side Converter (GSC) or over the Rotor Side Converter (RSC). The experimental results based on "FPGA in the loop" hardware prototyping verify the theoretical study and the performances of the proposed diagnosis method. The WECS can still operate in nominal conditions even if a power switch is faulty.

II. Fault Tolerant Converter Topology

Fig. 1 shows the proposed fault tolerant converter topology. It consists of a classical three-leg power topology connected by bidirectional switches (triacs for example) to a redundant leg ($S_7 - S_8$). This leg will replace the faulty one after failure diagnosis. In Fig. 1, R_t and L_t are the Thevenin resistance and the Thevenin inductance; e_{kn} ($k = 1, 2, 3$) is the Thevenin voltage of the connected system. When a fault occurs in one of the power switches ($S_1 - S_6$), the power converter failure diagnosis detects the fault occurrence and isolates the faulty leg. If this fault is an open-circuit, the isolation is implemented by removing the gate signal from the switches of the faulty leg. In the case of short-circuit, the faulty leg is isolated by fast acting fuses. In both cases, the reconfiguration scheme triggers the suited bidirectional switch to connect the faulty phase to the midpoint of the redundant leg. In summary, the fault compensation is achieved by the following steps:

- Detection of the faulty leg (detailed in next section);
- Removing the control orders of the two drivers of the faulty leg;
- Triggering the suited bidirectional switch t_k;
- Using the control orders of the faulty leg for the redundant one;
- Stopping the fault detection scheme.

III. Fault Detection Scheme

Power switch fault detection is based on the comparison between measured and estimated pole voltages, v_{ko} ($k = 1, 2, 3$), respectively noted v_{kom} and v_{koes}. The estimated voltages can be expressed by:

$$v_{koes} = (2\delta_k - 1)\frac{v_{dc}}{2} \tag{1}$$

Where $\delta_k = \{0, 1\}$ is the switching pattern of the top semi-conductor switch of the leg number k and v_{dc} is the dc-link voltage. The fault occurrence can be determined by analysing the voltage error obtained from the difference between the measured and estimated pole voltages. This voltage error is given by:

$$\varepsilon_{ko} = v_{kom} - v_{koes} \tag{2}$$

First we suppose that the switches are ideal. With this supposition in normal operation, the measured and estimated pole voltages are equal and thus their difference is zero. The value of the voltage error, ε_{ko}, and the post-fault behaviour in both open-circuit and short-circuit cases are discussed in the following.

A. Open-circuit fault

In this section, open-circuit fault in one of the top semi-conductor switches, S_k ($k = 1, 2, 3$), is considered; then, the voltage error, ε_{ko}, and the measured pole voltage, v_{kom}, are calculated analytically. An open-circuit fault reduces the pole inverter topology to the equivalent circuit presented in Fig. 2. In this circuit, the measured pole voltage and the voltage error for phase k depends on the phase current i_k and the switching pattern of the switches of the leg number k. The analysis of the post-fault behaviour can be divided in two cases.

In the first one, i_k is assumed to be different from zero and in the second one, the zero crossing is considered.

1) Post-fault behaviour when $i_k \neq 0$

Even though the estimated voltage, v_{koes}, depends only on the switching pattern of the S_k, the measured pole voltage, v_{kom}, can be changed with the sign of the phase current i_k:

$$\text{if } i_k > 0 \;\Rightarrow\; v_{kom} = -\frac{v_{dc}}{2} \tag{3a}$$

$$\text{if } i_k < 0 \text{ and } \delta_k = 0 \;\; (\delta_{k+3} = 1) \;\Rightarrow\; v_{kom} = -\frac{v_{dc}}{2} \tag{3b}$$

$$\text{if } i_k < 0 \text{ and } \delta_k = 1 \;\; (\delta_{k+3} = 0) \;\Rightarrow\; v_{kom} = \frac{v_{dc}}{2} \tag{3c}$$

Table I presents the voltage error, ε_{ko}, for this case. We note that when $i_k \neq 0$, the fault is detected only if $i_k > 0$ and $\delta_k = 1$ ($\delta_{k+3} = 0$), otherwise the leg number k operates correctly and the voltage error is zero.

2) Post-fault behaviour when $i_k = 0$

When δ_k is one and i_k becomes zero, the values of v_{kom} and ε_{ko} depend on the state of the bypass diodes D_k and D_{k+3}. In this case, the state of these bypass diodes depends on the switching pattern δ_i and δ_j of the switches S_i and S_j ($i \neq j \neq k \in \{1, 2, 3\}$) and on the phase voltage e_{kn}.

By using the Kirchhoff laws, we obtain the following equations for ($k = 1, 2, 3$):

$$L_t \frac{d}{dt} i_k + R_t i_k + e_{kn} - v_{kn} = 0 \tag{4}$$

Assuming the grid voltages balanced and the sum of the phase currents being null, we deduce:

$$v_{1n} + v_{2n} + v_{3n} = 0 \tag{5}$$

The output voltages of the inverter can be expressed as:

$$v_{kn} = v_{ko} + v_{on} \tag{6}$$

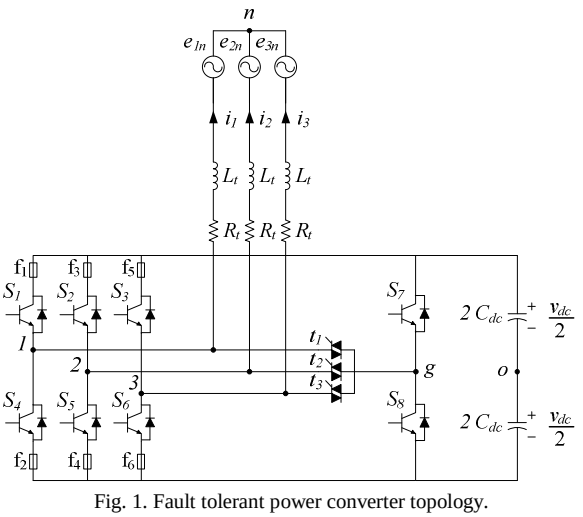

Fig. 1. Fault tolerant power converter topology.

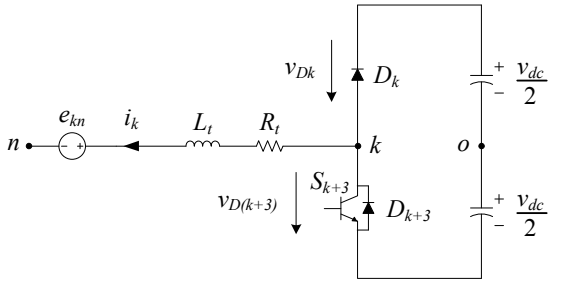

Fig. 2. Equivalent circuit for open-circuit fault in the switch S_k *(k = 1, 2, 3)*.

From expressions (5) and (6), we obtain:

$$v_{on} = -\frac{1}{3}(v_{1o} + v_{2o} + v_{3o}) \tag{7}$$

When i_k is equal zero, the output voltages of the inverter v_{kn} is equal the phase voltage e_{kn}. Thus v_{ko} can be given by:

$$v_{ko} = v_{kn} - v_{on} = e_{kn} - v_{on} \tag{8}$$

From expressions (7) and (8), we obtain:

$$v_{on} = -\frac{1}{2}(v_{io} + v_{jo} + e_{kn}) \qquad (i \neq j \neq k \in \{1, 2, 3\}) \tag{9}$$

The voltages across the bypass diodes D_k and D_{k+3} are expressed by:

$$v_{Dk} = v_{kn} - (\frac{v_{dc}}{2} + v_{on}) \tag{10}$$

$$v_{D(k+3)} = (-\frac{v_{dc}}{2} + v_{on}) - v_{kn} \tag{11}$$

We now study the states of the bypass diodes D_k and D_{k+3}:

Case 1: $\delta_i = \delta_j = 0$

$v_{Dk} = e_{kn} - [\frac{v_{dc}}{2} + \frac{1}{2}(v_{dc} - e_{kn})] = -v_{dc} + \frac{3}{2}e_{kn} < 0 \Rightarrow D_k$ is off

TABLE I

OPEN-CIRCUIT FAULT IN THE SWITCH S_K ($K = 1, 2, 3$) WHEN $i_K \neq 0$

i_k	δ_k	D_k	D_{k+3}	v_{kom}	v_{koes}	ε_{ko}
>0	1	Off	On	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$-v_{dc}$
>0	0	Off	On	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	0
<0	1	On	Off	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	0
<0	0	Off	Off	$-\frac{v_{dc}}{2}$	$-\frac{v_{dc}}{2}$	0

$v_{D(k+3)} = [-\frac{v_{dc}}{2} + \frac{1}{2}(v_{dc} - e_{kn})] - e_{kn} = -\frac{3}{2}e_{kn} \Rightarrow$ if $e_{kn} > 0$ then D_{k+3} is off, else D_{k+3} is on

Case 2: (δ_i =1 and δ_j = 0) or (δ_i =0 and δ_j = 1)

$v_{Dk} = e_{kn} - \frac{1}{2}(v_{dc} - e_{kn}) = -\frac{v_{dc}}{2} + \frac{3}{2}e_{kn} \Rightarrow$ if $e_{kn} < \frac{v_{dc}}{3}$ then D_k is off, else D_k is on

$v_{D(k+3)} = -\frac{1}{2}(v_{dc} + e_{kn}) - e_{kn} = -\frac{3}{2}e_{kn} - \frac{v_{dc}}{2} \Rightarrow$ if $e_{kn} > -\frac{v_{dc}}{3}$ then D_{k+3} is off, else D_{k+3} is on

Case 3: $\delta_i = \delta_j = 1$

$v_{Dk} = e_{kn} - [\frac{v_{dc}}{2} - \frac{1}{2}(v_{dc} + e_{kn})] = \frac{3}{2}e_{kn} \Rightarrow$ if $e_{kn} < 0$ then D_k is off, else D_k is on

$v_{D(k+3)} = [-\frac{v_{dc}}{2} - \frac{1}{2}(v_{dc} + e_{kn})] - e_{kn} = -v_{dc} - \frac{3}{2}e_{kn} < 0 \Rightarrow D_{k+3}$ is off

With the considerations of the above study, Table II presents the voltage error between the measured and estimated pole voltages for open-circuit fault in the switch S_k when i_k crosses zero during post-fault operation. In this case, when D_k is on, i_k becomes negative and the leg number k operates correctly, thus the voltage error is zero. When D_{k+3} is on, i_k becomes positive and thus the voltage error is $-v_{dc}$ and the fault can be detected. When D_k and D_{k+3} are off, i_k remains zero and the voltage error depends on the phase voltage e_{kn} and the fault can be detected. Same analysis can be used for the open-circuit fault in one of the bottom semi-conductor switches, S_k ($k = 4, 5, 6$).

B. Short-circuit fault

In this section, short-circuit fault in one of the top semi-conductor switches, S_k ($k = 1, 2, 3$), is considered. A short-circuit fault reduces the pole inverter topology to the equivalent circuit presented in Fig. 3. Table III presents the voltage error, ε_{ko}, for just after fault occurrence.

TABLE II
OPEN-CIRCUIT FAULT IN THE SWITCH S_K WHEN δ_k IS ONE AND i_k CROSSES ZERO.

case	δ_i	δ_j	e_{kn}	D_k	D_{k+3}	v_{kom}	ε_{ko}
1	0	0	> 0	Off	Off	$-\frac{v_{dc}}{2}+\frac{3}{2}e_{kn}$	$\frac{3}{2}e_{kn}-v_{dc}$
			≤ 0	Off	On	$-\frac{v_{dc}}{2}$	$-v_{dc}$
2	1 0	0 1	$\ge \frac{v_{dc}}{3}$	On	Off	$\frac{v_{dc}}{2}$	0
			$>-\frac{v_{dc}}{3}$ $<\frac{v_{dc}}{3}$	Off	Off	$\frac{3}{2}e_{kn}$	$-\frac{v_{dc}}{2}+\frac{3}{2}e_{kn}$
			$\le -\frac{v_{dc}}{3}$	Off	On	$-\frac{v_{dc}}{2}$	$-v_{dc}$
3	1	1	≥ 0	On	Off	$\frac{v_{dc}}{2}$	0
			< 0	Off	Off	$\frac{v_{dc}}{2}+\frac{3}{2}e_{kn}$	$\frac{3}{2}e_{kn}$

We note that when $\delta_k = 1$ ($\delta_{k+3} = 0$) the leg k operates correctly and the voltage error is zero. But when δ_k is equal to zero ($\delta_{k+3} = 1$) a dc-link shoot through occurres (see Fig. 4a). This case is dangerous, so a reliable protection must be used to isolate the faulty leg. Some possible locations of fuses in VSI have been discussed in [12]. More, several tests with short-circuit of IGBT have been performed to study the rupture phenomena and examine how a fuse protects an IGBT [12-16]. These papers demonstrated that one fast acting fuse in series with each IGBT can efficiently protect it against overcurrent.

After dc-link short-circuit occurrence (see Fig. 4a), different cases could occur depending on the fuses clearing time and the fault detection time. If the fuses clearing time is smaller than the fault detection time, before fault detection the faulty leg is isolated by its fuses. Thus the faulty leg current and the phase current become zero. This condition corresponds to the 3 situations with zero current mentioned in Table II (D_k and D_{k+3} off). Table IV presents the voltage error between the measured and estimated pole voltages for this case. If the fuses clearing time is grater than the fault detection time, the fault is detected before faulty leg isolation. So, the reconfiguration scheme removes the control orders of the two drivers of the faulty leg and then uses them for the redundant leg. Also, it triggers the suited bidirectional switch to connect the faulty phase to the midpoint of the redundant leg. In this case dc-link short-circuit is not yet cleared and consequently the overcurrent appears in the bottom semi-conductor switches S_8 placed in the redundant leg (see Fig. 4b). Since there is only one fuse in the short-circuit current path, the short-circuit is cleared after fuse operation.

Same analysis can be made for the short-circuit fault in one of the bottom semi-conductor switches, S_k ($k = 4, 5, 6$).

TABLE III
SHORT-CIRCUIT FAULT IN THE SWITCH S_K ($K = 1, 2, 3$)

δ_k	v_{kom}	v_{koes}	ε_{ko}
1	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	0
0	0	$-\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$

TABLE IV
SHORT-CIRCUIT FAULT IN THE SWITCH S_K ($K = 1, 2, 3$) WHEN δ_k IS ZERO AND THE FUSES CLEARING TIME IS SMALLER THAN THE FAULT DETECTION TIME

δ_i	δ_j	v_{kom}	ε_{ko}
0	0	$-\frac{v_{dc}}{2}+\frac{3}{2}e_{kn}$	$\frac{3}{2}e_{kn}$
0 1	1 0	$\frac{3}{2}e_{kn}$	$\frac{v_{dc}}{2}+\frac{3}{2}e_{kn}$
1	1	$\frac{v_{dc}}{2}+\frac{3}{2}e_{kn}$	$v_{dc}+\frac{3}{2}e_{kn}$

C. Time fault detection criterion

As a result of the previous theoretical discussion with ideal switches consideration, the fault occurrence in each leg can be determined with a comparator that compares the measured and estimated pole voltages. However, in real case, because of turn-off and turn-on propagation time and interlock dead time generated by the switches drivers, the voltage error is not null and constituted of peak during switching time. To avoid false fault detections due to power semi-conductors switching, we think of transforming the "voltage" error signal in a "time" error signal. The time error signal, n_k, is achieved for each phase by first taking the absolute value of the voltage error signal, applying that to a comparator with a threshold value h as presented in Fig. 5. The output of the first comparator, c_k, is equal to zero if $|\varepsilon_{ko}| \le$ h and equal to one if $|\varepsilon_{ko}| >$ h. Thus, the output of this comparator is a repetitive square waveform due to semi-conductors switching. The up-counter is enabled and starts to count when the output of the first comparator is equal to one. The output of the up-counter, n_k, is equal to the number of clock pulses while the output of the first comparator is one, if counting is initialised to zero after each square waveform. With consideration of the clock pulse frequency, the output of the up-counter means the time during which v_{kom} and v_{koes} are different. Finally, the up-counter output is applied to a second comparator with a threshold value, N_t, several times larger than the switching time. Consequently, the fault occurrence is detected using simultaneously a "time criterion" and a "voltage criterion". By this way, we avoid false fault detection due to semiconductor switching and we can detect the fault condition in less than 10 µs. The resulting signal f_k from the fault detection scheme is used to isolate the faulty leg, trigger the suited switch t_k and stop the fault detection scheme.

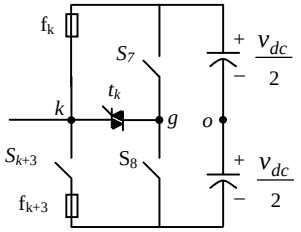

Fig. 3. Equivalent circuit for short-circuit fault in the switch S_k *(k = 1, 2, 3).*

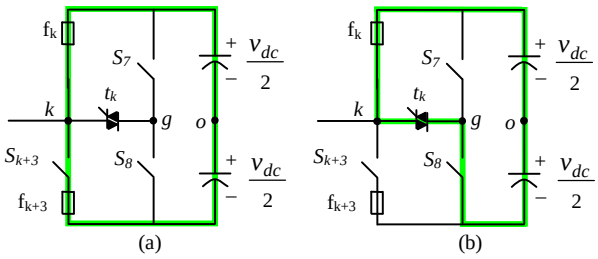

Fig. 4. Short-circuit current path; (a) after fault occurrence; (b) when the fuses clearing time is grater than the fault detection time.

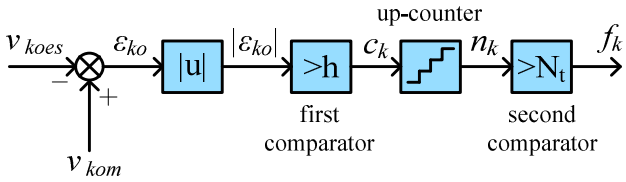

Fig. 5. Proposed fault detection.

IV. Application Case: Fault Tolerant WECS with DFIG

A. Fault tolerant topology

The studied fault tolerant WECS is based on an horizontal axis wind turbine model with Maximum Power Point Tracking (MPPT) and pitch control [1], [17]. For the modeling of the DFIG, the classical (d-q) DFIG model in the Park reference frame has been used [18]. The generator used in the studied WECS is controlled to provide the grid with a constant frequency with unity power factor capability [18].

Fig. 6 shows the fault tolerant WECS topology. It is based on a classical back-to-back converter and uses a common redundant leg for both three-phase power converters. The redundant leg composed of the switches S_7 and S_8 and will replace the faulty one of the other legs under any power switch failure in the GSC or the RSC.

Fig. 7 shows the fault tolerant system. In healthy condition, the FPGA-based fault detection and compensation block directly apply the switching patterns, determined by the RSC and GSC controllers, to the power converters. In faulty case, the fault detection scheme (see Fig. 5) detects the fault (in the RSC or the GSC) and the control orders of the two drivers of the faulty leg are removed. More, the fault signal f_k triggers the suited bidirectional switch and the control orders of the faulty leg are applied to the redundant one. Finally, the fault detection scheme is disabled by the same fault signal f_k.

B. Experimental validation of the real time diagnosis

1) "FPGA in the loop" prototyping methodology

The large benefits of using FPGAs for controlling industrial electrical systems, drived by a power converter were outlined by Monmasson et al. in [19] and [20]. A typical example consists in current controller implementation [20] because of the ability of the FPGA-based controllers to execute quasi-instantaneously their tasks. In our case, to perform fast fault detection, a FPGA digital implementation of the real time diagnosis is used [21].

Designing and testing digital control systems for electric drives and power electronic applications can be costly and time consuming. Traditional software based simulation has the disadvantage of being unable to exactly replicate real operating conditions. It does not take into account the limitations of the digital controller, like saturation of values in fixed point DSP systems during the intermediate calculations. It also does not take into account the finite resolution of DSP registers. Also, in virtual prototyping of digital controllers based on mixed simulation such as VHDL-Analog and Mixed-Signal Extension Language (VHDL-AMS) and ModelSim, the real controller is not experimentally tested [22-24]. One way for designing and testing the digital control system is the use of the real digital controller as "controller in the loop" hardware prototyping while eliminating the risk of damaging the actual drive or plant [25].

To test experimentally the proposed diagnosis, a new "FPGA in the loop" hardware prototyping method is used [26].This method is based on an unique modelling and FPGA-based experimental environment to prototype the studied real time diagnosis in the complete industrial electronic system. A Stratix DSP S80 development board, which comprises the Stratix EP1S80B956C6 FPGA chip, was used to implement this real time diagnosis.

The fault tolerant scheme is designed using fixed-point Altera DSP Builder library blocks in the Simulink environment and then the designed system is compiled and downloaded into the FPGA chip.

In Fig. 8, the FPGA implementation flow is shown. The Altera DSP Builder is the software which integrates both high-level algorithm and hardware description language (HDL) development tools to create FPGA designs. For automated design flow, the "Signal Compiler" block, which is at the core of DSP Builder, can generate HDL code and scripts for Quartus II-based synthesis and fitting from within Simulink. Furthermore, the DSP Builder "Hardware in the Loop" (HIL) block enables chip programming for hardware–software co-simulation.

Consider now the "FPGA in the loop" principle. At each time step, the fault tolerant WECS topology (Fig. 6) is simulated using the Matlab/SimPower Systems toolbox in discrete-time mode. Then the Simulink output signals (v_{dc}, v_{kom} and δ_k) are exported to the FPGA.

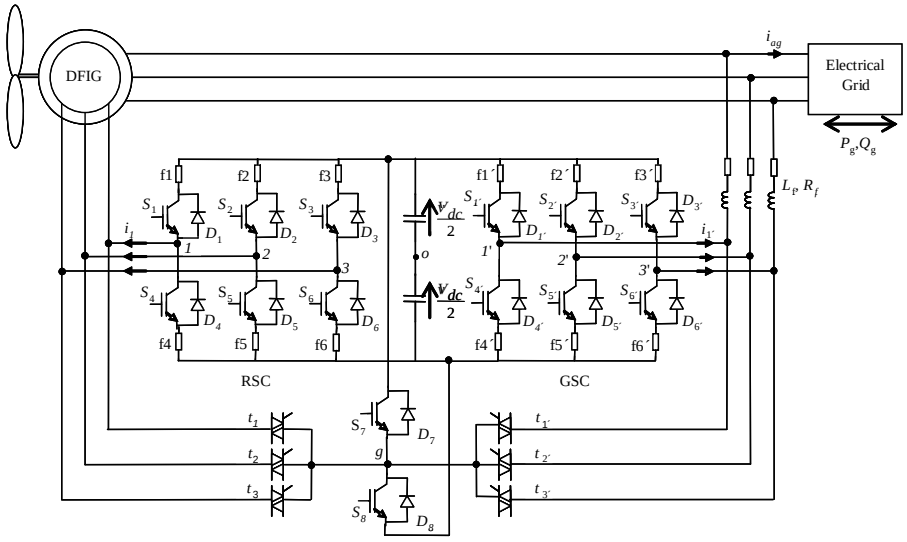

Fig. 6. Fault tolerant WECS topology with DFIG.

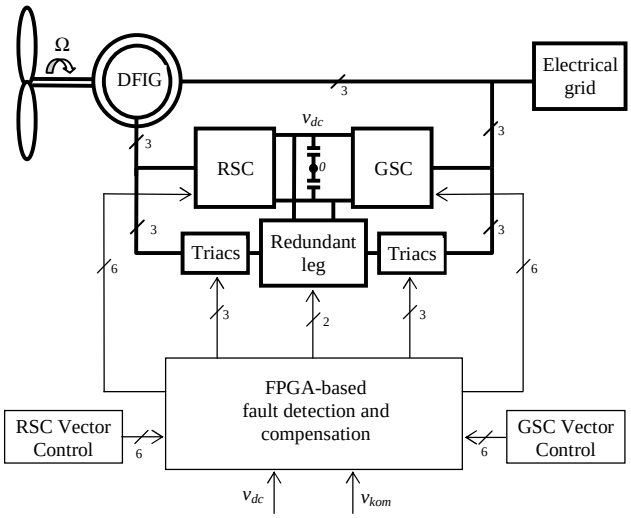

Fig. 7. Fault tolerant system.

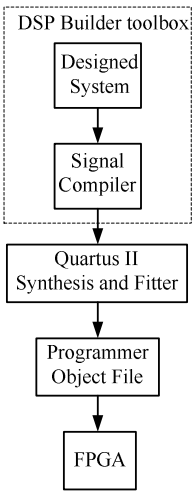

Fig. 8. FPGA implementation flow.

When the FPGA receives these signals, it executes the implemented real time power failure diagnosis for one sample interval. The FPGA returns to Simulink the switching pattern for the power switches, computed during this "FPGA in the loop" step. At this point, one sample cycle of the FPGA in the loop is performed.

In this prototyping method, a Joint Test Action Group (JTAG) interface links Simulink and the FPGA board. Fig. 9 shows the experimental setup used to evaluate the real time power converter failure diagnosis.

2) Fault detection scheme implementation

A Moore Finite State Machine (FSM) is used to implement the fault detection scheme. Fig. 10 presents the state diagram of the fault detection scheme. The control unit of the fault detection scheme is shown in Fig. 11. The up-counter is clocked by a signal with a period of 200 ns, generated from an internal PLL and the threshold value N_t is chosen equal to 50 steps (corresponding to 10 μs).

Notably the fault detection time is not limited by the proposed method because FPGA is fast enough to reduce the fault detection time. However, the minimum fault detection time is limited by the chosen threshold value N_t which depends on the specifications of the devices used in the actual WECS. The threshold value N_t must be chosen regards on:

- the time response of the voltage sensors used for the pole voltages measurement;
- the characteristics and performances of the analog data acquisition, mostly analog to digital converter and interface electronics;
- the dead time of the IGBTs' drivers.

3) Results

In this section, we examine the response of the WECS in two power switch converter failure cases. Open switch fault is considered because of the use of fuses. We considered that the fault appears on the third leg of the RSC or the GSC. The studied cases are the following:

- GSC is faulty (case *a*),
- RSC is faulty (case *b*).

System parameters are given in Table V. The power plant and the controller are simulated in discrete-time mode with 10µs sampling period. PWM frequency is reasonably set to 5 kHz [27]. The choice of this upper switching frequency limit for a 3 MW WECS lets us to validate the proposed failure diagnosis under higher reasonable switching frequency.

Fig. 12 and 13 present the results for the cases *a* and *b* respectively, without fault compensation. In the case *a* the fault is introduced in the top switch of the leg number *3'* ($S_{3'}$) at t = 1.6 s. In the case *b* the fault is introduced in the top switch of the leg number *3* (S_3) at t = 2.1 s. In the GSC fault occurrence case (case *a)*, an open circuit without fault compensation leads to oscillations and discontinuities for the $i_{3'}$ current; consequently the power P_g injected into the grid is fluctuating. For the RSC fault occurrence (case *b*), we either notice oscillations for the i_3 current and consequently the active power P_g is no more regulated.

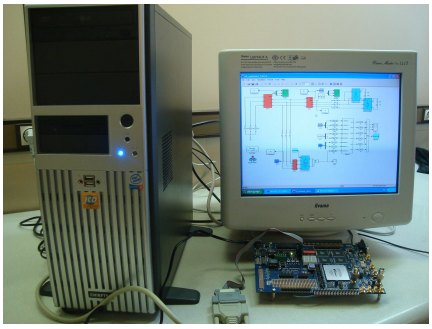

Fig. 9. Experimental "FPGA in the loop" setup.

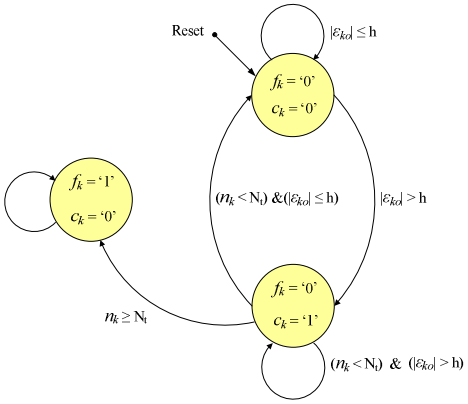

Fig. 10. State diagram of the fault detection scheme.

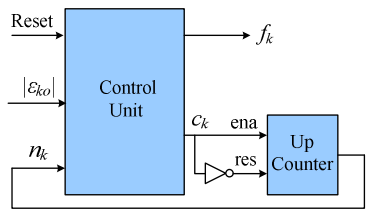

Fig. 11. Control unit of the fault detection scheme.

Fig. 14 and Fig. 15 illustrate experimental "FPGA in the loop" prototyping results for the same faults when the proposed power switch fault detection is used. One can see that for the studied fault tolerant WECS topology, the system can still operate in nominal conditions under any power switch failure.

Fig. 16 and Fig. 17 show zoomed results for a duration of 1 ms for the cases *a* and *b* respectively. In the case *a* before fault occurrence at t = 1.6 s the current $i_{3'}$ is positive and $\delta_{3'}$ is one. Therefore, the fault detection is achieved 10 µs after fault occurrence. In the case *b* before fault occurrence at t = 2.1 s the current i_3 is negative. Thus the fault is not detected until i_3 becomes zero at t = 2.11816 s. At this time, δ_1 is equal to zero and δ_2 is one. Since e_{3n} is equal to 230 V (case 2 in table II) D_3 and D_6 are off, thus i_3 remains zero. Therefore the up-counter is enabled and starts to count. However, the fault is not detected because before 10µs, δ_1 becomes one and then the faulty leg operates correctly (case 3 in table II). At t = 2.11824 s, δ_1 becomes equal to zero and i_3 becomes null and remains zero for the second time. The fault detection is achieved 10 µs after the second time that i_3 becomes zero.

One can notice that with such a small time interval between the fault occurrence and its detection, the fault effect does not appear in the waveforms, because the threshold time (corresponding to the threshold value N_t) is smaller than the switching period.

V. Conclusion

This paper discussed the design, implementation, experimental validation and performances of a fully digital power converter failure diagnosis for fault tolerant WECS. The proposed fault detection scheme was validated by "FPGA in the loop" new prototyping method for a WECS with DFIG. The fault tolerant topology was achieved by adding one redundant leg to the classical back-to-back power converter topology. More, we examined a new fault detection and compensation method without false fault detection due to semiconductor switching. The proposed method minimizes the delay time between the fault occurrence and its diagnosis. The experimental validation of the real time diagnosis demonstrates the possibility to detect a faulty switch in less than 10 µs by using simultaneously a "time criterion" and a "voltage criterion". In actual WECS, when a fault appears on the back-to-back converter, the system is disconnected from the electrical grid. As proposed in this paper, with such a fault tolerant topology, the WECS can still operate in nominal conditions and consequently economic benefits can be realized. More, the fault detection principle detailed in this paper can be used in any WECS with electrical machine using three-phase voltage source inverter and/or rectifier.

TABLE V
SIMULATION PARAMETERS

Grid	Rated voltage: 690 Vrms (line to line), frequency = 50Hz,
Turbine	Diameter = 80 m Gearbox = 70
DFIG parameters	S_n = 3MVA, p = 2, J = 256 kg.m^2, R_s = 2.97mΩ, R_r = 3.82mΩ, L_s = 12.241mH, L_r = 12.177mH M = 12.12mH, σ = 0.0145
Input filter	R_f = 1mΩ, L_f = 0.1mH
DC link capacitor	C_{dc} = 4.7mF Nominal DC voltage v_{dc} = 1200V

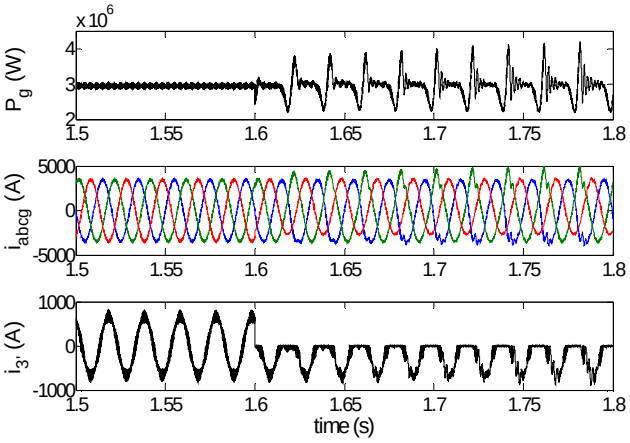

Fig.12. Case *a* without fault compensation

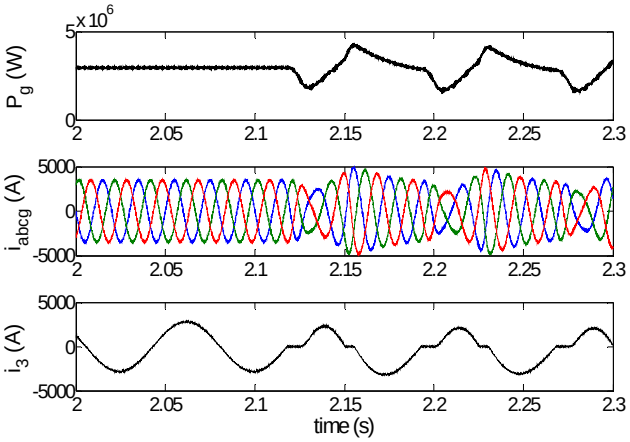

Fig.13. Case *b* without fault compensation

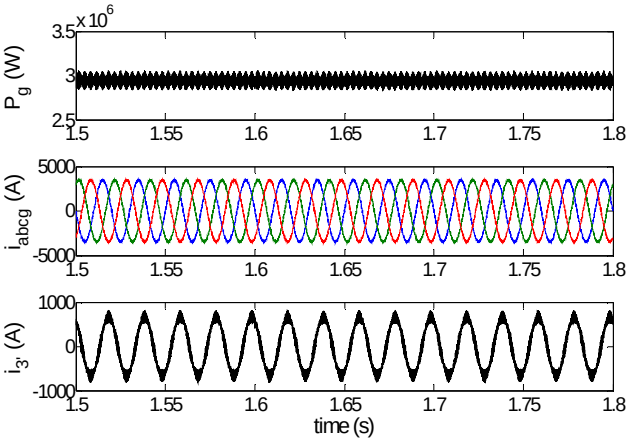

Fig.14. Case *a* with fault compensation

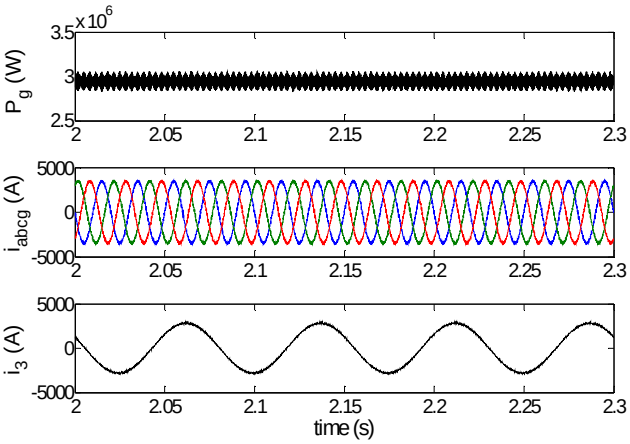

Fig.15. Case *b* with fault compensation

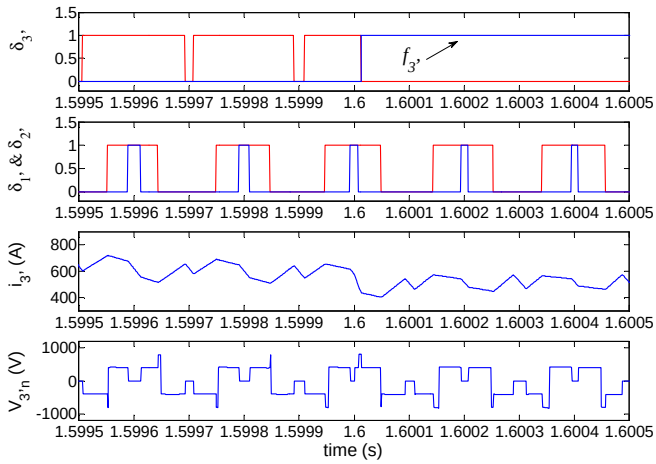

Fig. 16. Zoomed results of the proposed fault detection scheme for case *a*.

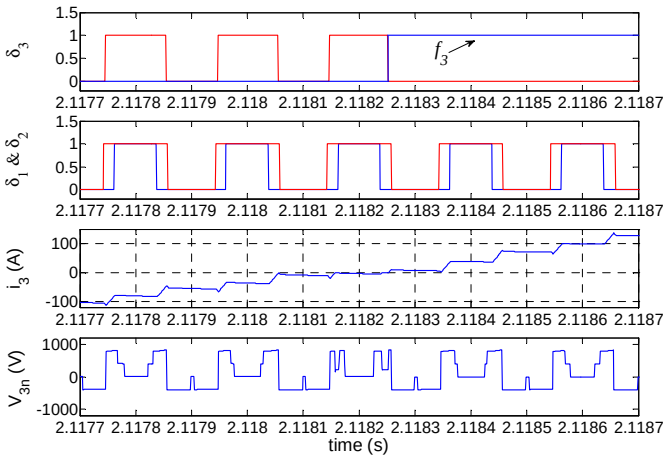

Fig. 17. Zoomed results of the proposed fault detection scheme for case *b*.

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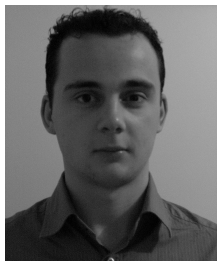

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