Automotive Power-Line Communication Channels: Mathematical Characterization and Hardware Emulator

Automotive Power Line Communication Channels: Mathematical Characterization and Hardware Emulator

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***Abstract*—This paper addresses the design of a channel emulator for the data communication along in-vehicle power distribution networks. Power line communication technology is a promising solution that uses the same physical bundle of wires supplying energy to the large number of components spread within a car, with benefits in terms of budget and weight saving. The communication channel is described by means of a multipath representation while the different noise contributions, supported by a dedicated measurement campaign, include impulsive and very low frequency disturbances. The channel emulator is designed on a Virtex-6 FPGA with a target working frequency of 200 MHz. The proposed emulator has very high programmability and is proven to provide superior performance in terms of bandwidth compared to known state-of-the art hardware non automotive alternatives.**

I. Introduction

Power line communication (PLC) is an attractive technology aiming at reusing existing wires for communication purposes. Initially it gained consideration from researchers and industry for low rate narrow band applications (for instance automated meter reading) in the access domain. At the end of the last century, high rate wide band PLC solutions have begun to be studied for in-home connectivity and successful standards appeared around 2005. Since it has been widely recognized that the power line channel is rather an hostile environment for communications purposes (high and frequency selective attenuations, impulsive noise, etc.), researchers have made several efforts to characterize it, in order to develop proper communication protocols. Moreover, physical channel emulators have been developed: these emulators enable designers testing and refining their prototypes. The advantage is both using an environment similar to the one where future products will be deployed and, while benefiting of real transmitters and receivers, reducing the time needed for particular demanding software simulations.

In the last years, the good achievements obtained in the application of the PLC technology to the access and domestic environments have encouraged the PLC community to broaden its application to alternative, e.g. automotive, domains [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13].

To introduce the PLC technology in a new environment, it is especially helpful for modem designers to tune the communication algorithms in laboratory, with the confidence that they will work on the real communication medium. This result can be obtained by acquiring the knowledge of the environment and developing a framework to reproduce it in the laboratories.

The scope of this study is to present a characterization of the automotive PLC medium, together with the design of an FPGA based real time emulator. The proposed solution is proven to provide a significant improvement compared to currently available alternatives in the literature. On the one hand, it achieves a larger bandwidth than previous emulators [14], [15], [16], [17], [18]. On the other hand, it offers a wide flexibility in terms of both channel and noise waveforms characteristics, which can be dynamically adapted by tuning a set of configuration parameters. These features enable a large range of novel applications that will be expected in the coming years. An outline of the key characteristics of the above state-of-the-art solutions and the comparison with the proposed approach will be discussed hereafter in the paper and summarized in Tab. V.

The structure of the paper follows. Section II summarizes the proposed model representations for both the channel and the noise characterizations, with specific emphasis on the measurements campaign carried out. Section III presents the high level architecture of the hardware model. Sections IV, V, VI detail the three most important units in the automotive power line emulator, namely the configurable tapped delay line, the additive white gaussian noise (AWGN) generator, and the generator for impulsive and very low frequency waveforms. Section VII discusses the results of the synthesis and the comparison of the proposed design with existing alternatives in literature. Final remarks and conclusions are collected in Section VIII.

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II. Mathematical representation

This section briefly introduces the mathematical repres tation assumed to describe the behavior of a link of an vehicle PLC channel. The proposed representation, that in agreement with the modeling framework of the curr state-of-the-art literature, consists of the superposition of *channel* and *noise* contributions. The former accounts for propagation of signals through the power network and latter includes the possible disturbances observed in a power network (e.g., due to the switching activity of the act devices or electrical motors).

A. Channel representation

The car power network consists of a complex structure t can be effectively represented via an interconnected netw of multiconductor lines. In [2], it has been demonstrated t the so-called *multipath model* is suitable to characterize the automotive power line channel. In the frequency domain, its mathematical representation writes:

$$H(j\omega) \approx \sum_{k=1}^{m} g_k \exp(-j\omega\tau_k) \qquad (1)$$

where H is the frequency-domain transfer function of interest (in our case the ratio between the received and the transmitted signals), $\omega = 2\pi f$ is the angular frequency and m is the total number of terms (also labelled as *taps*). For each term in the sum, g_k and τ_k are the complex weighting coefficients accounting for the attenuation and phase distortion of the transmitted signal and the propagation delays, respectively.

According to [19], a sampling frequency of 200 MHz and a number of terms $m = 300$ allow (1) to preserve, with a very high degree of accuracy, the statistics of important channel parameters such as the minimum, the average and the standard deviation of the channel attenuation and the coherence bandwidth. Results of [19] are obtained in the $[1.8, 86]$ MHz band, which is a range specified for in-home PLC modems [20] and that is expected to be used for future automotive PLC modems as well.

Equation (1) is also suitable to describe the channel for frequencies lower than 1.8 MHz (see [2]). In this study, we have also considered the possibility to couple (1) with a simple first order infinite impulse response (IIR) filter $W(j\omega) = j\omega/(j\omega + \omega_0)$: if only the $[1.8, 86]$ MHz frequency range is of interest and the parameters of (1) are optimized for this range, we have observed that the IIR (which is programmable in the emulator) could be helpful to capture the dominant high-pass behavior that is exemplified in the right panel of Fig. 1.

As far as the quantization of the channel taps is concerned, it has been verified that a number of bits greater than or equal to 13 is required to achieve a high accuracy of the channel emulator. We have assessed the loss of accuracy introduced by this quantization by modeling the transmission of an HomePlug AV2 (HPAV2) signal (frequency band $[1.8, 86]$ MHz) and comparing the power spectral densities (PSDs) of the received convolved signals (with or without tap quantization) using the channel measurements of [2]. In a first test, the HPAV2 signal has been assumed with a flat PSD on the whole band: the obtained mean absolute frequency error was lower than 0.04 dB on all the test channels. In a second test, the HPAV2 signal has been assumed with a PSD profile according to the Federal Communications Commission (FCC) regulations [21] . In this case, the obtained mean absolute frequency error was lower than 0.35 dB on all the test channels. The little degradation of the second test is due to the fact that the transmit signal involves a more challenging dynamic range including some notches below 30 MHz and a PSD drop of about 30 dB above 30 MHz (it should be noted that the just mentioned results are also due to the possibility to scale the channel taps, for instance by a proper normalization before programming the emulator, and a compensation of this normalization in the emulator analog signal-to-noise ratio (SNR) circuit).

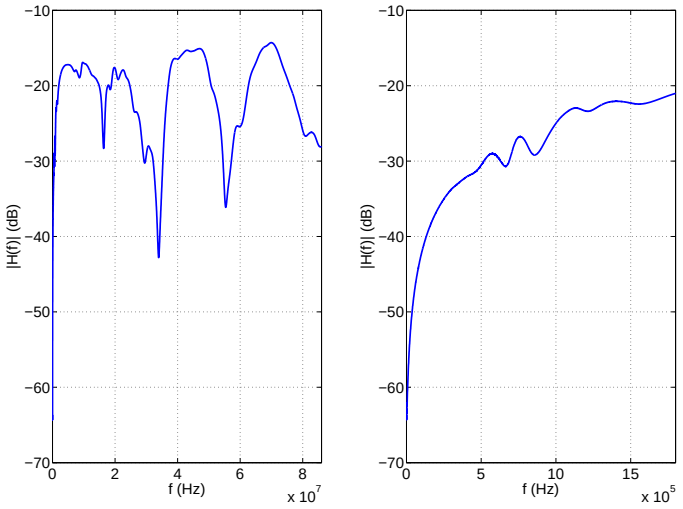

Fig. 1. Frequency-domain PLC channel response between the front right dipped headlight and the front left high beam. Left panel: $[0, 86]$ MHz frequency range. Right panel: closeup on the $[0, 1.8]$ MHz region.

B. Noise representation

In order to collect useful information on the automotive noise characteristics, we have performed a measurement campaign involving a set of time-domain measurements on a popular economy car manufactured by General Motors, which has the dimensions and electronic features typical of many compact cars in the market. The measurements discussed hereafter in this section highlight noise contributions arising from the activity of the electric and electronic equipments and motors spread in the car. The latter disturbances play a key role in the data communication since they unavoidably impact the propagation of signals along the power line network.

The measured probing points are the dashboard light and car-radio connectors, on the front side of the console, the trunk and license plate lights and the front and rear lights (indicators, fog lights, reversing lights, dipped headlights, high-beam and parking-light points are considered). Also, different operating conditions are considered: key inserted, engine on/off, acceleration (2000 r.p.m., 4000 r.p.m.), application of brakes,

active lights and indicator signals, motion of car windows ar windscreen wipers.

Based on these selected probing points and conditions, tim domain voltage waveforms have been measured with a digit scope (LeCroy WavePro 7300A scope, 3 GHz bandwidth, 1 GS/s) and passive voltage probes. Fig. 2 and Fig. 3 sho two exemplary measurements that highlight the main featur of the time-domain disturbances. Fig. 2 corresponds to measurement carried out on the parking light, in the fro right light with engine and lights on: the top left panel show the raw measurement, while the remaining panels (derive from the top left one by appropriate filtering, e.g. of the ver low frequency noise components) will be used to describe th background and impulsive noise components. Fig. 3 corr sponds to a measurement taken on the reversing light, in th rear light with engine and lights on and with the left indicat active: the blue curve is the raw measurement, while the re curve (obtained by the blue one by properly filtering high frequency noise components) will be used to describe the very low frequency noise component.

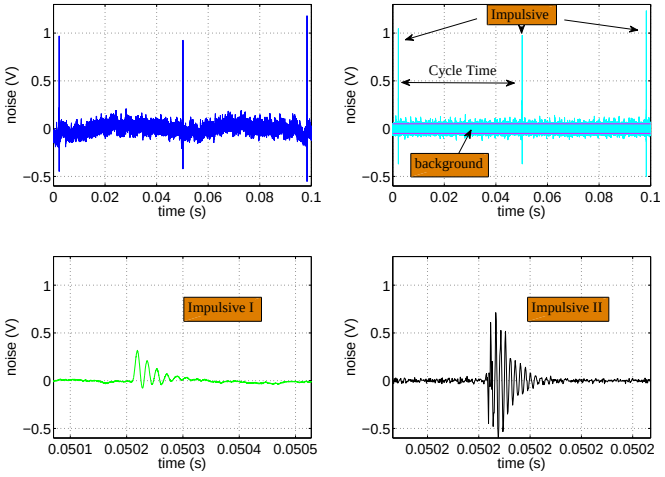

Fig. 2. Example of time-domain voltage measurement highlighting background and impulsive noise components (see text for details).

It is relevant to remark that the waveforms of Fig. 2 and Fig. 3 confirm the behavior of the typical in-vehicle automotive power distribution systems for the noise characterization (e.g., see [5], [22]). The above figures, however, have been selected to provide a picture of the features of this class of noises only since a more detailed discussion of the measurement and data processing is out of the scope of the present contribution. The reader should refer to the state-of-the art literature, where a number of papers focuses on the measurement campaigns (without loss of generality, see [2], [23] and references therein).

The additive noise components considered are:

- *Background noise*. It provides a mathematical description representing the thick background band that can be clearly seen in the curve reported in the top right panel of Fig. 2. According to previous analyses on different brands and models (see for instance [5], [22], [24]),

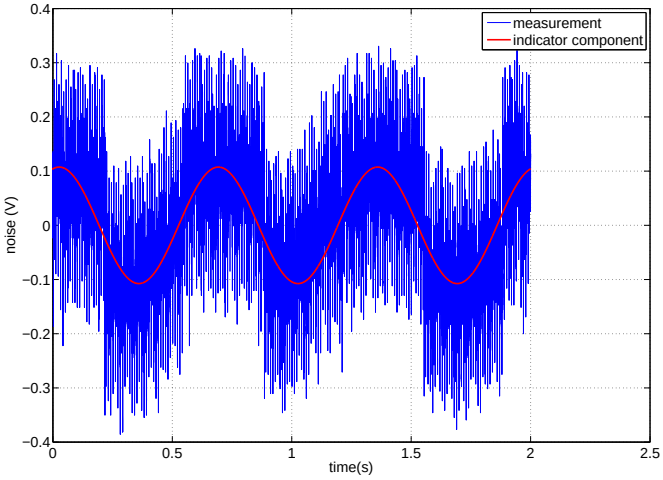

Fig. 3. Example of time-domain voltage measurement illustrating the effect of the very low frequency component (see text for details).

this background disturbance can be effectively modeled as a white Gaussian noise. This choice, that we confirm, unavoidably offers a number of advantages in the hardware implementation, mainly due to the availability of well established routines for the noise generation. However, to obtain an even more realistic representation of the background noise (especially for frequencies below 2 MHz), a possibility would be to modify the white Gaussian component with a proper coloring filter: this idea has been, for instance, proposed in [14] in a non-automotive domain.

- *Impulsive noise*. The curve in the top right panel of Fig. 2 also highlights the effects of the different electrical and electronic equipments that possibly disturb the power line. Motors or switching components unavoidably lead to spurious impulsive disturbances with either periodic or aperiodic nature (in Fig. 2 the three relevant spikes are periodic). Most spikes can be approximated by a damped sinusoidal signal that writes (e.g., for a spike at $t = t_0$)

$$\exp(-\frac{(t-t_0)}{\tau})\sin(\omega(t-t_0)), \quad t \geq t_0 \qquad (2)$$

Based upon our measurements and the literature, we have found that it is useful to have two impulsive noise components (see Tab. I) in the emulator. A component labeled as impulsive I is associated to the frequencies from 1 kHz to 10 MHz with a damping parameter τ in the range $[0.2, 22]$ μs. A second component, impulsive II, is associated to the frequencies from 1 MHz to 40 MHz with damping parameter τ in the range $[0.02, 1.1]$ μs instead (see the bottom panel of Fig. 2 for some examples). It is important to notice that the aforementioned impulsive components can occur at different time instants. For both impulsive components, in Tab. I a cycle time range characterizing the time distance between successive impulses is reported.

In the emulator, the above characterizing parameters

TABLE I
IMPULSIVE NOISE COMPONENTS CHARACTERIZING PARAMETERS.

	Frequency Range (MHz)	τ (μs)	Cycle Time (ms)
Impulsive I	$[10^{-3}, 10]$	$[0.2, 22]$	$[3, 100]$
Impulsive II	$[1, 40]$	$[0.02, 1.1]$	$[10^{-3}, 100]$

have been stored with fine granularity resolutions and a sinusoidal spurious-free dynamic range (SFDR) as reported in Tab. II. Moreover, the emulator also allows: i) transforming the damped sinusoids in pure sinusoids by eventually disabling the exponential part; ii) having sporadic aperiodic and continuous noise situations (corresponding to cycle time ∞ and 0).

TABLE II
CHOICE OF THE TAB. I PARAMETERS IN THE DESIGNED EMULATOR.

	Frequency resolution (Hz)	τ resolution (μs)	SFDR (dB)
Impulsive I	100	0.2	78
Impulsive II	100	0.02	78

- *Very low frequency disturbances*. The third noise contribution considered in this study is a possibly superimposed signal with a low frequency (less than 1 kHz) periodic behavior that could lead to a large amplitude disturbance. As an example, Fig. 3 (red curve) shows the noise introduced by the activated left indicator. Other devices that are sources of very low frequency disturbance are for instance the windscreen wipers and the car windows. Although the frequencies of this class of noise terms are lower than 1 kHz, their characterization is desirable in order to stress the filtering capability of the designed modem at the receiver side. In the proposed emulator, these low frequency disturbances are described as sinusoidal signals (the minimum frequency that can be emulated is 0.7 Hz).

In the emulator, the different noise components (background, impulsive (I and II), very low frequency disturbance) are handled independently, so that they can be separately enabled or disabled. Moreover, for each noise component, the first activation is programmed in the range from 0 to 300 ms, with 5 ns resolution.

III. ARCHITECTURE OF THE HARDWARE EMULATOR

Fig. 4 provides a general picture of the high level structure of the emulator. It consists of an FPGA board that implements the functional channel model and communicates with the transmit (Tx) and receive (Rx) modems via two dedicated analog boards. A personal computer is used to set the parameters of the channel emulator via the USB connections illustrated in the scheme.

In order to better detail the main internal blocks, Fig. 5 shows the logic architecture for the designed FPGA-based

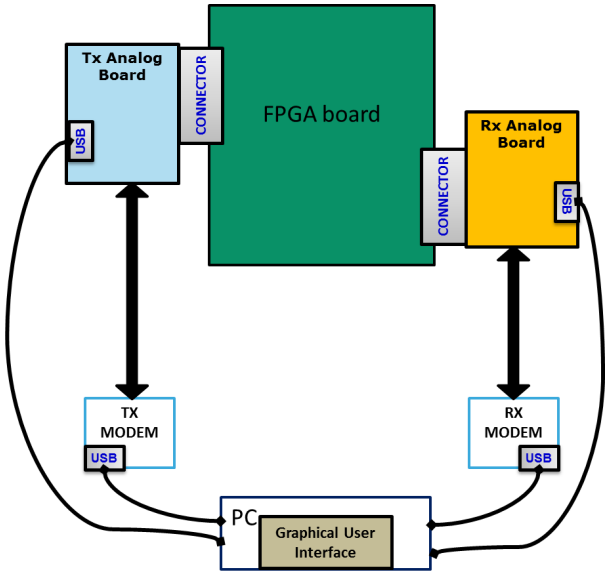

Fig. 4. High level architecture of the FPGA based channel emulator.

power line channel emulator. It was conceived to support both automotive (DC 12 V) (the main target) and indoor power line channels (AC 110-220 V), but it is flexible enough to be extended to also cover new channel models and modems. The emulator consists of two main logic modules: (i) the analog module (physically distributed on the Tx and Rx analog boards), which holds all the analog electronic components necessary to support the channel emulation, including digital to analog and analog to digital converters, and (ii) the FPGA module, which incorporates a Xilinx XC6VLX760 device and supports the digital processing functions and the system configuration task as well. The analog module is connected to the transmitting and receiving modems, while the FPGA module is controlled by the host PC, where configuration parameters for both digital and analog components are generated and sent through USB connection.

The analog module contains the access front end, directly connected to the external modems. It provides the power supply for the connected modems through the mains and it avoids, by low pass filtering, tx signal direct path flow from transmit to receive modem. Both DC and AC coupling are supported.

The Input Stage is a conditioning unit that regulates the access impedance presented to the transmitter and adapts the output coming from the transmitter to the features of the analog to digital converter. The Output Stage has two roles: on the one hand, it allows for independent gain regulation for both signal and noise components provided by the digital part of the system; on the other hand, the Output Stage adds the two contributions to obtain the final signal to be provided to the receiving modem. The choice of performing in the analog domain these two operations, the signal-to-noise ratio regulation and the final addition, guarantees a wide dynamic range. The gains values for signal and noise amplifiers are provided by the host PC, through the configuration interface contained in the FPGA module. The signal conversion unit

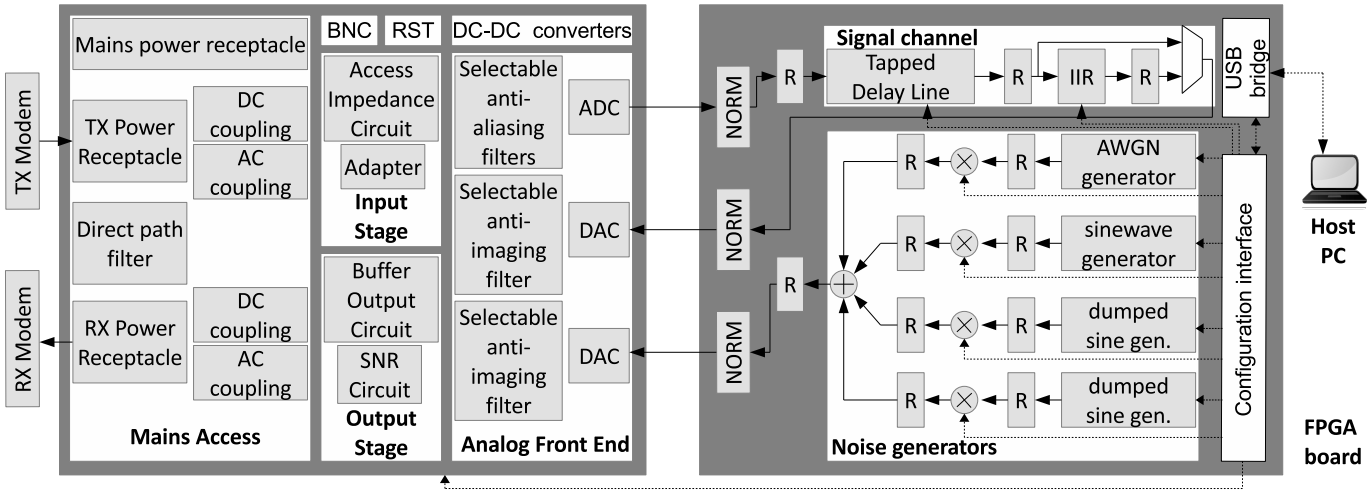

Fig. 5. Logic level architecture of the FPGA based channel emulator.

allows

- digitalizing the transmitted signal and send it to the FPGA module (ADC unit)
- receiving the channel convolution output and convert it to the analog domain (first DAC unit)
- converting the digital noise to the analog representation (second DAC unit)
- properly processing signals by means of selectable filters (anti-aliasing filter for the ADC input, anti-imaging filters for the two DACs outputs).

The Analog Devices AD9634 has been selected as the ADC unit. It is a 12 bit analog-to-digital converter, with sampling speed up to 250 MSPS, wide input bandwidth, and support for a variety of user-selectable input ranges. The DACs are AD9742 devices, which feature 12 bit resolution, conversion rate up to 210 MSPS, differential current outputs (2 mA to 20 mA). Main parameters of the analog modules are the gain values for signal and noise contributions and the selection values for the anti-aliasing and anti-imaging filters. In general, most parameters, including regulation and control parameters such as enablers, are received from the Host PC (through the FPGA module).

The XC6VLX760 device on the FPGA module includes a tapped delay line (TDL), which receives incoming samples from the ADC and the coefficients from a set of internal registers, initially loaded through the Configuration interface. The TDL is chained with the IIR unit and implements the channel representation introduced in Section II. Either the output of the TDL or the output of the IIR filter is sent to the DAC for conversion to the analog domain. Noise contributions (AWGN, sine wave and dumped sine waves) are separately generated and added to filtered samples after conversion to the analog domain. Actually, two instances of the dumped sine wave generator (SWG) are allocated, for Impulsive I and Impulsive II components, respectively (see the noise representation in Section II). Shift and normalize units (NORM) are placed at the input and output of the channel emulator to adapt internal bit width to external ports.

IV. The Configurable Tapped Delay Line

A fully parallel FIR filter architecture has been adopted for the tapped delay line and modeled as VHDL unit, with parameterized length and bit width for both samples and coefficients. The transposed form shown in Fig. 6 is used because it guarantees a shorter clock period and a higher throughput than the direct form.

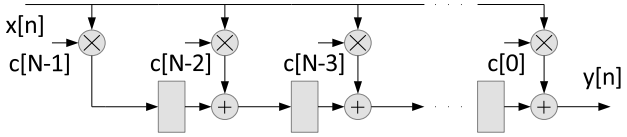

Fig. 6. TDL unit in trasposed form.

The number of coefficients is always equal to the TDL length and therefore the TDL is characterized by a regular and modular architecture, where a tap unit is placed at every delay element. However, any number ($\leq$ TDL length) and location pattern (on a time interval equal to the product of the TDL length by the clock frequency) can be programmed for TDL coefficient by simply setting to zero the coefficient value when the corresponding tap is missing.

The whole TDL is structured into N stages (N is the length of the TDL), where each stage contains a multiplier unit, an adder and a register. The input sample x is distributed in parallel to the N multiplier units. The architecture of the TDL is optimized to achieve high processing throughput. In particular, each TDL unit is designed as a multi-stage component, with several registers placed along the signal flow and able to take full advantage of the pipelined DSP48E1 devices available in the Virtex-6 FPGA. Each multiplier unit also receives a coefficient (c) from the coefficient registers. If a given tap is not required in the generated channel model, the corresponding

coefficient is simply cleared during the configuration phase: in this case, the multiplication leads to zero and no contribution is accumulated to generate the output sample. The obtained products are sent to N adders, which progressively accumulate and delay received values. Each adder combines a product with the previously accumulated sum, received from the previous stage and registered to introduce a delay equal to a sampling period.

Also for the IIR filter, in order to achieve 100 MHz bandwidth, multiple pipelining levels have to be included on each filter stage. This requirement imposes the adoption of look-ahead techniques [25], to unroll the computational structure and insert pipelining registers in the proper positions along the signal flow.

The elements of flexibility incorporated in the described architecture can be classified as static (or design-time) and dynamic (or run-time) parameters. Design-time parameters allow tuning the characteristics of the designed emulator with no re-design of the VHDL model. They are defined in a package and can be set freely before compilation and synthesis. Main design-time parameters are the length of the delay line, the maximum number of taps, the bit width for input samples, coefficients and all intermediate signals.

Run-time parameters are the values of coefficients and the number of bit positions for shift operations required at the input and output of the channel emulator. As these values are not fixed, they are read from external ports. The Configuration Interface component in Fig. 5 receives from the host PC configuration data and forwards to the channel emulator the updated values of defined parameters and coefficients.

V. The Additive White Gaussian Noise generator

Digital generation of accurate AWGN samples is very critical from an implementation point of view. In the literature, several methods for AWGN generation are known [26], such as for example the Box-Muller algorithm, the central limit theorem (CLT) method, the Ziggurat method and the polar method. An extensive work on Gaussian noise generators is available in [27] and some of the reported methods have also been experimented in the context of the power line channel emulation [28]. In most cases, the Box-Muller approach is preferred and actually selected in several practical implementations, including a proprietary IP unit available from Xilinx. The CLT method is recognized as a low complexity solution [27] that suffers from lower statistical accuracy and lower convergence speed than other techniques. However, there exist methods to mitigate these limitations and to achieve good statistical properties and power spectral density of the generated random process, with a very low device occupation and sufficient sample throughput [29].

The CLT states that a Gaussian random variable can be obtained according to

$$S_n^* = \frac{X_1 + X_2 + \ldots + X_m - m\mu}{\sigma\sqrt{m}} \qquad (3)$$

where X_i is a sequence of random variables ($i = 1, \ldots, m$) with the same distribution, average μ, and variance σ^2, and S_n is a normal distribution random variable with average equal to 0 and variance equal to 1. If $m = 12$ uniform random variables are added together, division by $\sigma\sqrt{m}$ can be avoided, so saving hardware complexity.

The high level architecture of the developed AWGN generator is given in Fig. 7. Two uniform generators receive input seeds and generate a pair of uniform and independent samples, U1 and U2, by means of a 43 bit linear feedback shift registers and 37 bit cellular automata shift registers.

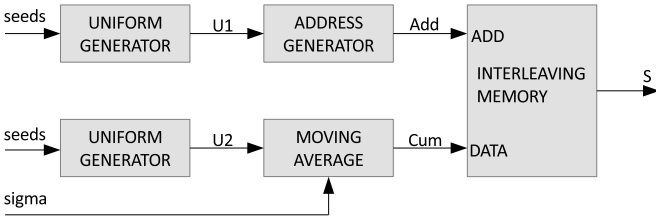

Fig. 7. Architecture of the AWGN generator.

In order to reduce the number of uniform samples to be generated, a moving average is calculated: a single uniform random number generator produces one sample per clock cycle and the 12 most recent samples are added together. After the samples are cumulated, the $-\mu$ term is added. The moving average solution allows for the generation of uniform and Gaussian samples at the same rate, and sampling frequency as high as the clock frequency can be obtained. A moving average unit receives uniform samples U2 and generates initial normal samples (Cum), which are obtained from the accumulated uniform samples.

The output of the moving average block is a normal random variable with average equal to 0 and standard deviation equal to the input sigma. However, the power spectral density of the obtained random sequence is not white and, additionally, its autocorrelation is not low enough (the maximum value for autocorrelation with a non-zero displacement is 0.91). In order to compensate for these limitations, two actions are taken. First, the sign bits of the samples produced by the uniform generator is randomly swapped, so as the sign of the correction term μ results to be a uniformly distributed random value. Second, interleaving is used to reduce sample correlation: samples are stored in a memory in the natural order and retrieved following a random read pattern. In Fig. 7, the address generator calculates addresses (Add) for the interleaving memory, starting from the random input U1 received by the uniform generator. Interleaving memories scramble the sequence of normal samples. Each generated address is first used to read a sample from the memory; then a new sample is written into the same location to prevent the previous one to be read more than once. According to [29], the autocorrelation of random sequences produced by combining the two mentioned strategies is much lower than in the original sequence: a value of 0.011 was obtained for a sequence of nine millions of samples. Moreover, statistical properties of the obtained distribution were proven using the Kolmogorov-Smirnov test,

which was successfully passed with a significance level of 0.05.

VI. The generators for impulsive and very low frequency noise contributions

A numerically controlled oscillator (NCO) is used to generate impulsive and very low frequency noise contributions (Fig. 8). In the shown NCO scheme, the content of a phase accumulator P is updated at each clock cycle by adding the current value stored in the phase accumulator register and a digital number, M, stored in the delta phase register. The output of the phase accumulator is used as the address to the LUT, where each location corresponds to a phase point on the sine waveform from 0 to 2π radians. Alternatively, to reduce the size of the LUT, only values for the range 0 to $\pi/2$ radians are stored and the adder is replaced with a properly controlled adder/subtracter.

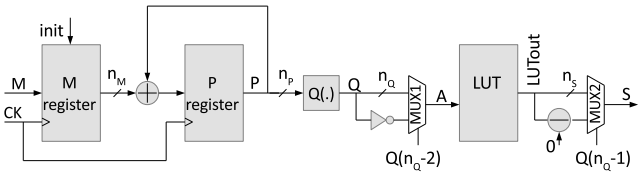

Fig. 8. DDS based sinewave generator.

Let f_{CK} be the clock frequency and n the number of bits in the phase register, the LUT has 2^n locations and the frequency of the generated waveform is given by

$$f = \frac{M f_{CK}}{2^n} \tag{4}$$

Given a LUT size, the signal frequency can be increased by increasing M. Therefore, very large values of n are necessary to achieve low signal frequencies, which results into a large LUT size. In order to reduce the LUT size, the accumulated phase can be quantized on a lower number of bits, $l < n$: this solution allows to trade-off implementation complexity for frequency accuracy.

The signal Q is the quantized version of the accumulated phase P. As the LUT only stores the sine amplitudes for phase range from 0 to $\pi/2$, the waveform in the three remaining quadrants must be corrected. In the second and fourth quadrants, the LUT content must be read in the opposite sequence, from the last location to the first one: this is obtained by taking the one complement of the quantized phase. To this purpose, MUX1 is allocated to generate the LUT address directly from Q for quadrants 1 and 3, while A is equal to the one complement of Q for quadrants 2 and 4. The second most significant bit of Q discriminates between quadrants 1 or 3 and 2 or 4, and it is used to drive MUX1. Moreover, in quadrants 3 and 4, the LUT output must take the negative sign: in Fig. 8, the subtracter calculates the difference $0 - LUT_{out}$ and the multiplexer MUX2 is driven by the most significant bit of Q, which identifies quadrants 3 and 4. Given a specified frequency f and a frequency resolution $\Delta f = f_{CK}/2^n$, the required values for M and n can be easily derived as

$$M = \left\lceil \frac{f}{f_{CK}} 2^n \right\rceil \qquad n = \left\lceil \log_2 \frac{f_{CK}}{\Delta f} \right\rceil \tag{5}$$

It is also known that the number of quantization bits n_Q required to properly represent the phase when a given SFDR is desired can be written as $n_Q = \lceil SFDR/6 \rceil$, with $SFDR$ in dB.

Using (4) and (5), the general waveform generator in Fig. 8 can be customized for the non Gaussian noise components. For components Impulsive I and Impulsive II, since the clock frequency is assumed to be $f_{CK} = 200$ MHz and $\Delta f = 100$ Hz and $SFDR = 78$ dB (see Tab. II in Section II), n is chosen equal to 21 and $n_Q = 13$, which can be reduced to 11 because only the first quadrant needs to be actually stored in the LUT. Moreover, the required value of M is selected starting from the requested frequencies, with the minimum frequency of 1 kHz of component Impulsive I obtained with $M = 10$, and the maximum frequency of 40 MHz of component Impulsive II generated by setting $M = 419430$. For the very low frequency disturbance component (see Section II), the required frequencies are much lower, but they can still be generated with the scheme of Fig. 8, provided that the clock frequency is reduced by means of a divider, so that the P register is updated at a lower rate. Using a prescaling factor equal to 128, the lowest frequency of 0.7 Hz is obtained with $M = 1$ and $f = 1$ kHz is achieved with $M = 1342$. The initial phase of the generated sine wave can be easily made programmable in the range from 0 to $\pi/2$ by enabling the preset of the P register.

For noise components Impulsive I and Impulsive II, a similar structure is used for the generation of the exponential waveforms, which will be then multiplied by a sinusoid, to obtain the final dumped signal.

Time duration and cycle time are programmed for the three sine wave generators, while the exponential waveforms are automatically adapted to the same choices programmed for the corresponding sine waves. Similarly to the approach used in the architecture of microcontrollers, a single free running counter is used to generated start and stop events of each waveform. When a given event (start or stop of a waveform) has to be scheduled, the corresponding scheduling time is loaded into a dedicate register, which is compared to the content of the free running counter: the detection of the equal condition triggers the event and the update of the register with the next scheduling event to be detected.

VII. Synthesis results and comparisons

The previously described units have been initially modelled under MATLAB, using finite precision arithmetic. A VHDL model has then been developed and validated by comparison with the MATLAB version. Finally, logic synthesis and place & route was run under Xilinx ISE version 14.4, targeting a clock period of 5 ns. Figs. 9 and 10 report a comparison between the measurements and the emulated channel and noise.

In Fig. 9 the frequency response of the channel measured between the front left dipped headlight and the rear right indicator light is reported for the [1.8, 86] MHz frequency

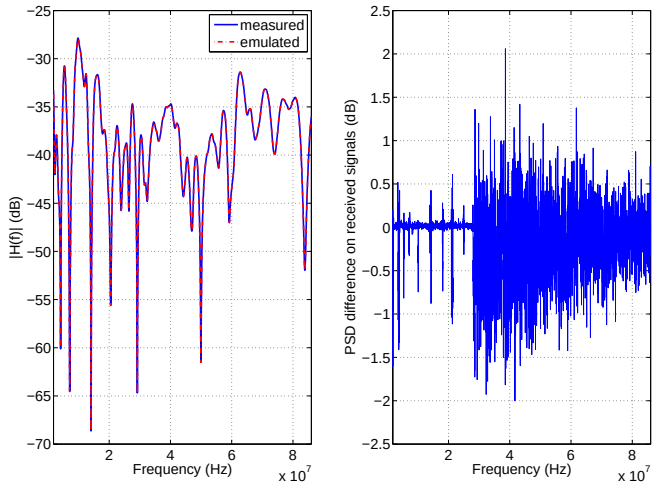

Fig. 9. Channel measurement and emulation (see text for details).

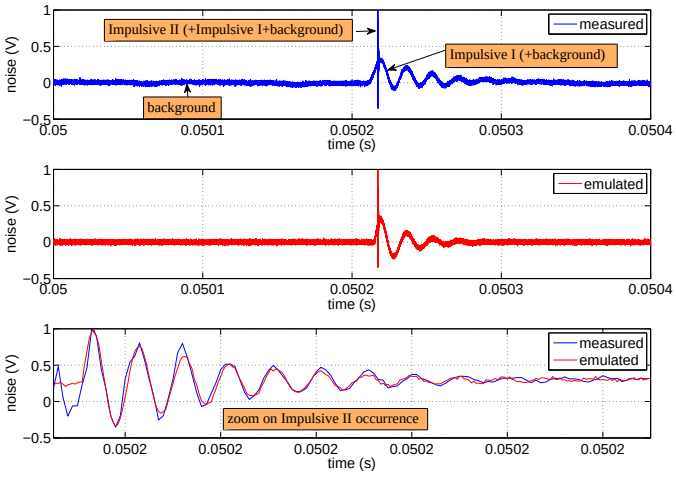

Fig. 10. Noise measurement and emulation for background and impulsive noise components (see text for details).

range together with the emulated one. They are nearly superimposed. An HPAV2 signal has been transmitted and the received PSD has been registered (see the right panel of Fig. 9). For the measured channel, the transmission was done in MATLAB and no noise was added; in the emulator, the noise insertion has been disabled. The effects of the emulator analog part (ADC and DAC) can be perceived: the difference is zero on the average but with up to 2 dB fluctuation on the single frequency. Moreover, as expected, the difference is larger above 30 MHz due to the FCC transmit PSD drop and below 30 MHz where transmission notches take place. In Fig.10 noise measurement and emulation are shown for background and impulsive noise components. The top panel reports the measurement and it is a zoom on the central impulsive peak of the top right panel of Fig. 2. The central panel show the emulated noise: the Impulsive I component has been programmed with frequency 57 kHz and $\tau = 19.2$ μs, while the Impulsive II component is obtained with the following parameters: frequency= 10.5 MHz and $\tau = 280$ ns; Impulsive II waveform starts with a delay of 440 samples with respect to the Impulsive I component. A zoom in the zone of occurrence of the Impulsive II component is reported in the bottom panel of Fig.10. Overall, the obtained noise emulation appears to be satisfying.

TABLE III
FPGA SYNTHESIS RESULTS.

Number of Slice Registers	49,110 out of 948,480
Number of Slice LUTs	24,913 out of 474,240
Number of Slice LUTs used as logic	16,675 out of 474,240
Number of Slice LUTs used as Memory	5,820 out of 132,480
Number of fully used LUT-FF pairs	21,244 out of 474,240
Number used as Dual Port RAM	2,160
Number used as Shift Register	3,660
Number of bonded IOBs	97 out of 1,200
Number of RAMB36E1	0 out of 720
Number of RAMB18E1	0 out of 1,440
Number of DSP48E1	314 out of 864

TABLE IV
PERCENTAGES OF REQUIRED RESOURCES FOR MAIN EMULATOR UNITS.

	AWGN	TDL	IIR	SWG	Interface
Number of Slice Registers	3%	38%	1%	5%	53%
Number of Slice LUTs	4%	58%	0	14%	25%
Number used as logic	2%	65%	0	4%	28%
Number used as Memory	13%	0	0	87%	0
Number of DSP48E1s	1%	96%	1%	2%	0

Target device is the Xilinx XC6VLX760 FPGA. Resource usage, summarized in Tab. III, is about 5% for the selected device.

The breakdown in Tab. IV shows that the TDL is the largest component in the emulator and requires 300 DSP units and more than 15,000 LUTs. The sine wave generator and the configuration interface also consume a relevant portion of slices, while the AWGN is rather inexpensive.

Timing analysis shows that all slacks are positive with achievable clock period of 5 ns and the critical path is along the routing channels between Configuration interface and TDL.

A few previous implementations of hardware emulators for the PLC channel are available in the open literature, and none of them is applied to the automotive case. Tab. V reports the main characteristics of these works.

The frequency-domain approach was used to model the channel response only in [15] and [18], where large fast Fourier transform and inverse fast Fourier transform (FFT and IFFT) units (4096 and 1024 points, respectively) are allocated to convert signals between time and frequency domains; all other implementations adopted the time-domain solution, with adaptive tapped delay lines of various lengths. The supported bandwidth ranges from the 500 kHz assumed as a constraint in initial works, up to 30 or 75 MHz of the most recent papers. The number of emulated taps covers quite a large spectrum,

TABLE V
MAIN FEATURES OF PLC CHANNEL EMULATORS.

Reference	year	application domain	signal model	bandwidth	tap number	background noise	impulsive noise	low frequency noise
[14]	2004	indoor	time	30 MHz	5 to 50	m-sequence	statistical model	-
[15]	2008	indoor	frequency	30 MHz		noise vectors	DDS	-
[16]	2009	indoor	time	500 kHz	1000	PN-sequence	DDS	-
[17]	2011	indoor	time	75 MHz	200		-	
[18]	2011	indoor	frequency	30 MHz		Middelton's model		-
this work	2015	automotive	time	100 MHz	300	CLT	DDS	DDS

TABLE VI
MAIN PROGRAMMABLE PARAMETERS FOR NOISE COMPONENTS.

Parameter	low frequency	impulsive I	impulsive II
frequency range	$[0, 1000]$ Hz	$[1, 10^4]$ kHz	$[1, 40]$ MHz
frequency resolution	1 Hz	100 Hz	1 kHz
SFDR (dB)	78	78	78
duration	$[0, \infty]$	$[0, \infty]$	$[0, \infty]$
cycle time	$[0, \infty]$	$[3, 100]$ ms	$[10^{-3}, 100]$ ms
τ range	-	$[0.2, 22]$ μs	$[0.02, 1.1]$ μs
τ resolution	-	0.2 μs	0.02 μs

from 5 to 1000. The proposed FPGA based emulator is the only one able to reach 100 MHz, with a relevant number of paths. No information is available from most considered papers in terms of complexity. An NVIDIA GeForce GT 240 GPU with 12 processors and 96 cores is used in [18], while in [17] three FPGA devices are used to model up to 200 taps.

Different techniques have been used to generate background noise. [14] uses m-sequences, [15] describes a generator based on a set of stored noise vectors, [16] adopts PN-sequences and the Middlenton's Class A model is exploited in [18] to generate both background and impulsive noise. The emulator presented in this work is the only one using the CLT approach, which is very inexpensive in terms of both processing resources and memory requirements. In order to generate impulsive noise, an ad-hoc statistical model is proposed in [14], while [15] and [16] adopt direct digital synthesis (DDS). Low frequency noise is supported only by the proposed emulator, which includes dedicated DDS resources to support both impulsive and low frequency noise waveforms.

It can be seen from Tab. V that the proposed emulator achieves the largest bandwidth among compared implementations; moreover, it is able to generate a wide spectrum of noise waveforms, through a set of configuration parameters that can be loaded statically or at run time: the main parameters and their limits are reported in Tab. VI.

VIII. CONCLUSIONS

Within the automotive domain, power line communication technology has been proven to be a recent promising alternative to the classical data communication along dedicated in-vehicle bundles of wires. The feasibility and strengths of this technique has to be assessed via systematic performance evaluations of different design scenarios. This is best achieved via a real time emulation of the whole transmission chain, which cannot be done off-line via a software simulation only. In this framework, this paper specifically focused on the design of a dedicated PLC hardware emulator operating at a working frequency up to 200 MHz and yielding superior performances with respect of the currently documented state-of-the-art implementations. The paper provided a self-contained contribution with detailed information on both the mathematical model proposed (including the characterization of both the functional and noisy behavior of the automotive PLC channel) and on the FPGA hardware emulator. Synthesis results obtained for a Virtex-6 device shows that the proposed emulator achieves the largest bandwidth among known hardware implementations. Moreover, it features a high degree of versatility, which allows up to 300 distinct taps and fully programmable dynamic range for signal and noise components.

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