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A Novel Approach to Generate Effective Carrier-Based Pulsewidth Modulation Strategies for Diode-Clamped Multilevel DC-AC Converters

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***Abstract*— Several pulsewidth modulation (PWM) strategies have been proposed for three-phase multilevel converters. Typically, these PWM methods can be either space-vector or carrier-based implemented, where the carrier-based implementation usually presents a lower computation complexity. In this paper, a novel approach for the carrier-based implementation of different existing PWM methods is proposed for three- and four-level dc-ac converters, which can be easily extended to any number of levels. The main features of the proposed approach are its reduced computation complexity and computation time. On the other hand, the proposed approach suggests the derivation of novel PWM strategies which can potentially present improved performance features. As an example, two new discontinuous PWM (DPWM) strategies are proposed for the four-level converter. One of these DPWM strategies presents lower weighted total harmonic distortion than other previously proposed strategies. Simulation and experimental results verify the effectiveness of the proposed approach and novel DPWM strategies.**

I. Introduction

MULTILEVEL converters are widely used for high-power applications. Their main advantages are low output voltage harmonic distortion, high efficiency, low device stress, etc. [1]-[7]. Multilevel conversion is typically considered for medium- and high-voltage applications. However, it has also found its use in low-voltage applications [8]-[10].

Multilevel converter topologies can be classified into three categories: diode clamped, flying capacitor, and cascaded H-bridge [1]-[2]. Among these, the most popular is the three-level diode-clamped topology [8], known as the neutral-point-clamped (NPC) topology. Fig. 1 presents the schematics of three-level (3L) and four-level (4L) three-phase diode-clamped dc-ac converters.

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Several pulsewidth modulation (PWM) strategies have been proposed to control the ac-side voltages of multilevel three-phase dc-ac converters. These strategies can be classified into three main categories: selective harmonic elimination [11]-[12], carrier-based PWM (CBPWM) [13]-[16], and space-vector-based PWM (SVPWM) [17]-[19]. The CBPWM methods compare three-phase reference signals to carrier signals to determine the duty cycle for the converter switches. If the reference signals are sinusoidal, the PWM strategy is called sinusoidal PWM (SPWM). In other carrier-based PWM approaches for three-phase three-wire systems, a common-mode (CM) offset is added to the sinusoidal reference signals without affecting the fundamental line-line ac-side voltages. The CM offset may extend the linear range of the SPWM strategy and significantly reduce the output harmonic distortion at higher modulation indices [20]-[21]. The CBPWM strategies are very easy to implement because they only require adding an offset to a sinusoidal signal to obtain the reference waveform, which is then compared to a carrier signal.

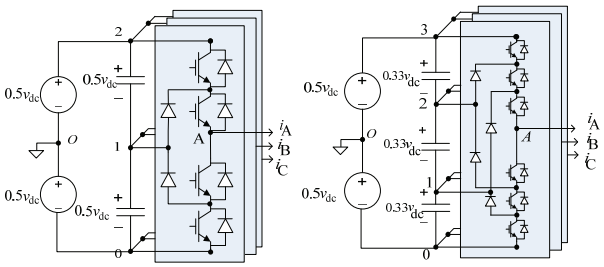

Fig. 1. Schematics of the three- and four-level three-phase diode-clamped dc-ac converters.

As opposed to the CBPWM strategies, which consider each phase reference signal separately, the SVPWM strategy is based on a single reference vector derived from the three-phase reference signals. This reference vector is approximated in a switching cycle by a sequence of converter switching states producing the same volt-second average as the reference

vector. The multilevel converter can generate n^3 switching states, where n is the number of levels, and each switching state corresponds to a space vector. All converter space vectors form the space vector diagram.

The most conventional SVPWM strategy, in each switching cycle, selects and applies a sequence of the three vectors nearest to the tip of the reference vector. The time for which a vector is applied is called the dwell-time for that vector. Among the three nearest vectors, one of them should have an even number of redundant switching states and should be realized by applying two of these redundant switching states for the same amount of time. Thus, this strategy requires several steps: the selection of the three nearest vectors, the vector dwell-time calculation, and the duty-cycle calculation for each switch [17], [22], [23], [26], [27]. To perform these steps, several techniques are proposed [17]-[19], [22]-[23].

The multilevel SVPWM strategies presented in [17], [22], and [23] are based on a recurrent application of the SVPWM strategy for the two-level (2L) converter. Reference [22] considers the space vector diagram of a multilevel converter as a combination of several small hexagons, which are centered at the space vectors of even redundancy. These small hexagons are treated as a space vector diagram of a 2L converter with reduced dc-link voltage. When the tip of the reference vector lies in one of these small hexagons, the vector dwell-times are calculated as in a 2L SVPWM strategy. Due to the need to first identify the small hexagon, this method requires extra computation.

A fast method for small triangle region identification and the vector dwell-time calculation are presented in [24]. After finding a vector dwell-time, it is necessary to identify the switching states to be applied, but the method does not provide any procedure for this.

An efficient way to implement the SVPWM strategies is through finding their CBPWM equivalent. This basically requires finding the proper CM offset to be added to the original sinusoidal reference signals. In multilevel converters, this is done in two steps [14], [16], [20], and [21]. First, a CM offset equal to the average of the maximum and minimum reference signal values is subtracted from them, same as in the case of the 2L converter. Then, the reference signals are modified so their carrier intersections lie within a carrier signal (from the set of $n-1$ carrier signals) using the modulo function [21]. After this, a second CM offset is calculated, equal to the average of the maximum and minimum values of the updated reference signals. Finally, this second CM offset is subtracted from the reference signals, which guarantees equal dwell-time for the redundant switching states in a switching period [14].

The second CM offset can be set to a different value to force that the dwell-time of one of the redundant switching states equals zero. This causes one of the converter legs to stop switching within the switching cycle, and the resulting PWM strategy is then known as discontinuous PWM (DPWM). The DPWM strategies have lower switching losses but higher output harmonic distortion compared to the conventional SVPWM. Reference [20] shows that, for the 3L converter, a DPWM strategy may have low output harmonic distortion if the switching frequency is increased such that the switching losses are the same as the switching losses of the conventional SVPWM strategy with the original lower switching frequency.

This paper presents a novel approach to generate effective CBPWM strategies for the multilevel converters, based on the correlation between the three sinusoidal reference signals and the position of the reference vector within the space vector diagram. It is shown that the location of the reference vector tip can be directly determined from the reference signals, without the need to calculate the reference vector angle and magnitude. In this paper, this approach is applied to implement competitive multilevel PWM strategies through a CBPWM strategy with only one CM offset addition.

The paper is organized as follows. Section II discusses the carrier-based implementation of continuous PWM strategies. Section III discusses the implementation of the DPWM strategies, and two new DPWM strategies are introduced. Section IV presents simulation and experimental results to verify the effectiveness of the proposed carrier-based implementation approach and the performance of two novel DPWM strategies. Finally, Section V presents the conclusions.

II. CONTINUOUS CBPWM

A. Two-Level Case

Three-phase voltage-source dc-ac converters are required to generate a balanced three-phase ac output voltage using PWM methods. The starting point is a set of three normalized reference signals for the phase voltages given by

$$\begin{aligned} v_{\mathrm{A,ref}} &= m\cos(\omega t) \\ v_{\mathrm{B,ref}} &= m\cos(\omega t - 2\pi/3) \\ v_{\mathrm{C,ref}} &= m\cos(\omega t + 2\pi/3), \end{aligned} \tag{1}$$

where $m = \sqrt{2}v_{\mathrm{o}} / (v_{\mathrm{dc}}/2)$ is the modulation index [20], v_{dc} is the dc-link voltage, v_{o} is the rms value of the output ac phase voltage, and ω is the desired fundamental frequency of the output ac voltage. The SPWM strategy directly compares these reference signals with a carrier signal.

In a carrier-based implementation of the conventional SVPWM, a CM offset is added to the reference signals in (1), given by [25]

$$v_{\mathrm{off}}(t) = -\frac{v_{\max}(t) + v_{\min}(t)}{2} \tag{2}$$

where

$$\begin{aligned} v_{\max}(t) &= \max\left(v_{\mathrm{A,ref}}(t), v_{\mathrm{B,ref}}(t), v_{\mathrm{C,ref}}(t)\right) \\ v_{\mathrm{mid}}(t) &= \mathrm{mid}\left(v_{\mathrm{A,ref}}(t), v_{\mathrm{B,ref}}(t), v_{\mathrm{C,ref}}(t)\right) \\ v_{\min}(t) &= \min\left(v_{\mathrm{A,ref}}(t), v_{\mathrm{B,ref}}(t), v_{\mathrm{C,ref}}(t)\right) \end{aligned} \tag{3}$$

Variables v_{max}, v_{mid}, and v_{min} are the maximum, middle, and minimum values of the reference signals at time instant t. In the conventional SVPWM strategy, the redundant switching states are applied for the same amount of time. This is guaranteed by adding the CM offset given by (2) [14]. The resulting reference signals obtained after adding the CM offset are compared to the triangular carrier signal for the generation of each switch duty cycle. This CBPWM strategy only requires a standard sorting algorithm and a few elementary operations and, thus, it is very easy to implement.

B. Multilevel Case

The space-vector-based implementation of a PWM strategy requires a reference vector ($\mathbf{V}_{ref}$) as an input, defined by its α- and β-components, which can be obtained as a function of the normalized reference signals for the phase voltages as

$$v_{\alpha,ref} = \frac{2}{3}\left(v_{A,ref} - \frac{v_{B,ref} + v_{C,ref}}{2} \right)$$
$$v_{\beta,ref} = \frac{1}{\sqrt{3}}\left(v_{B,ref} - v_{C,ref} \right) \quad (4)$$

This reference vector is typically approximated by the three nearest space vectors that can be generated by the multilevel converter. Fig. 2(a) and 2(c) show the space vector diagrams of the 3L and 4L converters, respectively. The switching states are denoted by three digits, where each digit denotes the voltage level to which phases A, B, and C are respectively connected.

There are three points that should be noted for the space vector diagram, its vectors, and the switching states.

First, some switching states produce the same space vector. The 3L converter has 6 large and 6 medium vectors with no redundant switching states, 6 small vectors with even redundancy, and one zero vector with odd redundancy. Similarly, the 4L converter generates 18 vectors with no redundancy, 13 vectors with even redundancy, and 6 vectors with odd redundancy.

Second, the space vector diagram of the multilevel converter has six sectors, and each sector can be divided into several subsectors, whose corners are defined by the tip of the converter space vectors. Subsectors for sector 1 are shown in Fig. 2(b) and 2(d) for the 3L and 4L converter, respectively.

Third, the space vector diagram can be visualized as a combination of small hexagons, centered at the space vectors with an even number of redundant switching states, which are marked with big solid dots in Fig. 2. Each small hexagon can be considered as the space vector diagram of a 2L converter with reduced dc-link voltage. For the 3L converter, there are six vectors of even redundancy which can be regarded as the small hexagon centers. For the 4L converter, there are 13 vectors of even redundancy which can be regarded as the small hexagon centers. For example, a small hexagon for a 4L converter centered at the switching states 210/321 is shown in Fig. 2(d) with bold lines.

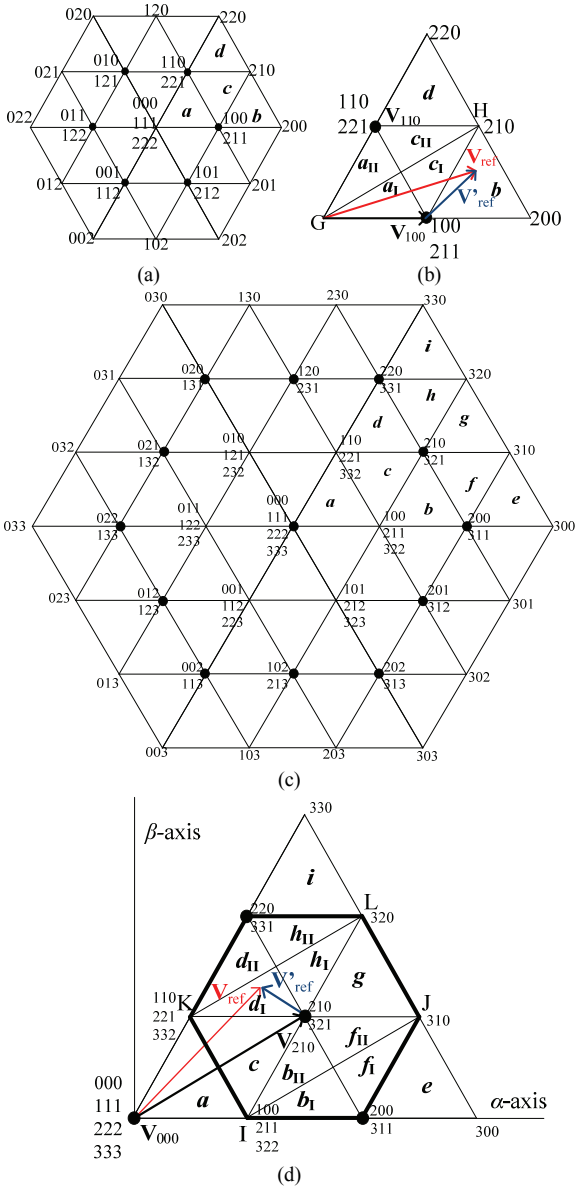

Fig. 2. Space vector diagrams. (a) Full diagram for the 3L converter. (b) Sector 1 for the 3L converter. (c) Full diagram for the 4L converter. (d) Sector 1 for the 4L converter.

In a space-vector-based implementation of a typical PWM strategy, the first step is to identify the space vector with even redundant switching states which is closest to the tip of the reference vector and the subsector where the tip of the reference vector lies. The corners of the subsector define the space vectors which will be used to approximate the reference vector. In the second step, the space vector with even redundancy is subtracted from the reference vector. This way, an updated reference vector ($\mathbf{V}'_{ref}$) is obtained which can be considered as a reference vector in the corresponding small hexagon. In the third step, the angle and magnitude of the updated reference vector is used to calculate the vector dwell-times producing the same volt-second average as the reference

vector. These dwell-times can then be used to calculate the duty cycle of each switch. In summary, this implementation method involves the identification of the nearest space vector with even redundancy, the calculation of the updated reference vector, the vector dwell-time calculation, and the switch duty-cycle calculation. Therefore, the implementation of the modulation strategy with this method is complex.

A simple carrier-based implementation of the conventional SVPWM strategy is proposed in [16], [20], and [21]. However, this requires addition of CM offsets in two steps. An alternate approach to obtain the carrier-based implementation of the conventional SVPWM strategy is presented in the following subsection, where only one CM offset is added to the reference signals.

C. *Simplified Procedure to Obtain the Carrier-Based Implementation of the Conventional SVPWM Strategy*

The proposed approach is derived from the analysis of the space-vector-based implementation and in light of the correspondence between reference vectors and modulating waveforms expressed in (4).

As mentioned before, in the space-vector-based implementation, the first step involves the identification of the vector with even redundant switching states which is closest to the tip of the reference vector. Let us assume a 3L converter whose reference vector lies in sector 1, as shown in Fig. 2(b). If the reference vector tip lies in subsector *b*, the nearest small vector is the one associated to switching states 100 and 211. If the reference vector tip lies in subsector *d*, the nearest small vector is the one associated to switching states 110 and 221. However, if the reference vector tip lies in subsectors *a* or *c*, the nearest small vector depends on the specific reference vector position. To determine this nearest small vector, subsectors *a* and *c* are divided into two regions marked with subscripts I and II. If the reference vector lies in region I, the redundant switching states 100/211 are used, and if it lies in region II, the redundant switching states 110/221 are used [22]. To determine the region where the tip of the reference vector lies, the equation of line GH, which divides the subsectors into two regions, can be used. Since the coordinates of points G and H are (0, 0) and (1, $1/\sqrt{3}$), the equation of line GH is

$$v_{\beta} = v_{\alpha}/\sqrt{3}. \tag{5}$$

According to (1), (4), and (5), the reference vector tip will lie in line GH when

$$v_{\mathrm{B,ref}} = 0. \tag{6}$$

It can be then easily derived that if $v_{\mathrm{B,ref}} < 0$, the reference vector tip lies in region I. Otherwise, the reference vector tip lies in region II. Thus, the reference signal value can be directly used to identify the region within the sector where the reference vector tip lies.

The second step involves the calculation of the updated reference vector corresponding to the small hexagon. If $v_{\mathrm{B,ref}} < 0$, the updated reference vector can be given by

$$\mathbf{V}'_{\mathrm{ref}} = \mathbf{V}_{\mathrm{ref}} - \mathbf{V}_{100}. \tag{7}$$

where $\mathbf{V}_{100}$ represents the space vector corresponding to switching states 100/211. In terms of the α- and β-components

$$\begin{aligned} v'_{\alpha,\mathrm{ref}} &= v_{\alpha,\mathrm{ref}} - v_{\alpha,100} \\ v'_{\beta,\mathrm{ref}} &= v_{\beta,\mathrm{ref}} - v_{\beta,100}. \end{aligned} \tag{8}$$

The αβ-components of $\mathbf{V}_{\mathrm{ref}}$ are given in (4). The αβ-components of $\mathbf{V}_{100}$ are

$$\begin{aligned} v_{\alpha,100} &= \frac{2}{3} = \frac{2}{3}\left(\frac{1}{2} - \frac{1}{2}\left(-\frac{1}{2} - \frac{1}{2}\right)\right) \\ v_{\beta,100} &= 0 = \frac{1}{\sqrt{3}}\left(-\frac{1}{2} + \frac{1}{2}\right), \end{aligned} \tag{9}$$

which, as shown in (9), can be obtained by applying (4) with normalized reference phase voltages ($v_{\mathrm{A,ref}}$, $v_{\mathrm{B,ref}}$, $v_{\mathrm{C,ref}}$) = (1/2, −1/2, −1/2). These normalized reference phase voltages correspond to the average of the normalized reference phase voltages of switching states 100 and 211, which are (0, −1, −1) and (1, 0, 0), respectively.

Substituting (4) and (9) in (8)

$$\begin{aligned} v'_{\alpha,\mathrm{ref}} &= \frac{2}{3}\left(\left(v_{\mathrm{A,ref}} - \frac{1}{2}\right) - \frac{1}{2}\left(v_{\mathrm{B,ref}} + \frac{1}{2}\right) - \frac{1}{2}\left(v_{\mathrm{C,ref}} + \frac{1}{2}\right)\right) \\ v'_{\beta,\mathrm{ref}} &= \frac{1}{\sqrt{3}}\left(\left(v_{\mathrm{B,ref}} + \frac{1}{2}\right) - \left(v_{\mathrm{C,ref}} + \frac{1}{2}\right)\right), \end{aligned} \tag{10}$$

which reveals that the normalized updated reference signals corresponding to the updated reference vector are

$$\begin{aligned} v'_{\mathrm{A,ref}} &= v_{\mathrm{A,ref}} - \frac{1}{2} \\ v'_{\mathrm{B,ref}} &= v_{\mathrm{B,ref}} + \frac{1}{2} \\ v'_{\mathrm{C,ref}} &= v_{\mathrm{C,ref}} + \frac{1}{2}. \end{aligned} \tag{11}$$

Eq. (11) provides the updated reference signals for a reference vector tip lying in subsectors *b*, a_{I}, or c_{I}. If the reference vector tip lies in subsectors *d*, a_{II}, or c_{II}, $\mathbf{V}_{110}$ should be subtracted from the reference vector. Vector $\mathbf{V}_{110}$ has an associated value of the normalized reference phase voltages ($v_{\mathrm{A,ref}}$, $v_{\mathrm{B,ref}}$, $v_{\mathrm{C,ref}}$) = (1/2, 1/2, −1/2). Thus, the updated reference signals are

$$\begin{aligned} v'_{\mathrm{A,ref}} &= v_{\mathrm{A,ref}} - \frac{1}{2} \\ v'_{\mathrm{B,ref}} &= v_{\mathrm{B,ref}} - \frac{1}{2} \\ v'_{\mathrm{C,ref}} &= v_{\mathrm{C,ref}} + \frac{1}{2}. \end{aligned} \tag{12}$$

Due to the six-fold symmetry of the space-vector diagram, the expressions of (11) and (12) will still hold for all sectors if $v_{\mathrm{A,ref}}$, $v_{\mathrm{B,ref}}$, $v_{\mathrm{C,ref}}$ are replaced by $v_{\max}$, v_{mid}, $v_{\min}$, respectively. The resulting general expression to obtain the updated reference signals in all possible locations of $\mathbf{V}_{\mathrm{ref}}$ is

$$
\begin{aligned}
&v'_{\max} = v_{\max} - 1/2 \\
&v'_{\min} = v_{\min} + 1/2 \\
&\text{if}\,(v_{\text{mid}} < 0) \\
&\qquad v'_{\text{mid}} = v_{\text{mid}} + 1/2 \\
&\text{else} \\
&\qquad v'_{\text{mid}} = v_{\text{mid}} - 1/2 \\
&\text{end.}
\end{aligned} \tag{13}
$$

These updated reference signals can be considered as the reference signals of a 2L converter with reduced dc-link voltage. Thus, in order to achieve equal time distribution of the redundant switching states, it seems reasonable to calculate a CM offset analogous to (2) from the updated reference signals in (13). Since it is possible that the phase with the original maximum/minimum reference signal value does not remain maximum/minimum after applying (13), it is necessary to initially resort the updated reference signals

$$
\begin{aligned}
v''_{\max} &= \max\left(v'_{\max}, v'_{\text{mid}}, v'_{\min}\right) \\
v''_{\text{mid}} &= \text{mid}\left(v'_{\max}, v'_{\text{mid}}, v'_{\min}\right) \\
v''_{\min} &= \min\left(v'_{\max}, v'_{\text{mid}}, v'_{\min}\right).
\end{aligned} \tag{14}
$$

The CM offset is then calculated as

$$
v_{\text{off}} = -\frac{v''_{\max} + v''_{\min}}{2}, \tag{15}
$$

and the final modulating signals for the carrier-based implementation are given by

$$
v''_{X,\text{ref}} = v_{X,\text{ref}} + v_{\text{off}}; \quad X \in \{\text{A,B,C}\}. \tag{16}
$$

This method requires only one CM offset addition.

A similar derivation can be performed for the 4L converter. The 4L converter has four vectors with even redundant switching states in sector 1, as shown in Fig. 2(d). The vector with even redundancy nearest to the reference vector tip needs to be identified. If the reference vector tip is in subsector *a*, the nearest vector with even redundancy is the zero vector $\mathbf{V}_{000}$. Therefore, the updated reference signals corresponding to the small hexagon are the same as the original reference signals. To determine if the reference vector tip is in subsector *a*, a condition in terms of the reference signals can be derived from the equation of line IK. This equation is defined by

$$
\begin{aligned}
&v_\beta = -\sqrt{3}\left(v_\alpha - 4/9\right), \\
&\text{or}\; v_{\text{A,ref}} - v_{\text{C,ref}} = 2/3.
\end{aligned} \tag{17}
$$

Thus, if $v_{\text{A,ref}} - v_{\text{C,ref}} < 2/3$, the reference vector tip lies in subsector *a*. Otherwise, it is outside subsector *a*. When the reference vector tip is outside subsector *a*, the nearest space vector with even redundancy, which is required to be subtracted from the reference vector, is determined with the aid of lines IJ and KL. The equation of line IJ is given by

$$
\begin{aligned}
&v_\beta = \left(1/\sqrt{3}\right)\left(v_\alpha - 4/9\right) \\
&\text{or}\; v_{\text{B,ref}} = -2/9,
\end{aligned} \tag{18}
$$

and the equation of line KL yields

$$
v_{\text{B,ref}} = 2/9. \tag{19}
$$

The equations of lines IJ, KL, and IK can be used to easily identify the sector region where the reference vector tip lies. This identification is performed from the reference signal values and does not require the calculation of the reference vector magnitude and angle.

Following a similar derivation as in the 3L case, for sector 1, the updated reference signals, whose corresponding reference vector tip does not lie in subsector *a*, are given by

$$
\begin{aligned}
&v'_{\text{A,ref}} = v_{\text{A,ref}} - 2/3 \\
&v'_{\text{C,ref}} = v_{\text{C,ref}} + 2/3 \\
&\text{if}\; v_{\text{B,ref}} < -2/9 \\
&\qquad v'_{\text{B,ref}} = v_{\text{B,ref}} + 2/3 \\
&\text{elseif}\; v_{\text{B,ref}} > 2/9 \\
&\qquad v'_{\text{B,ref}} = v_{\text{B,ref}} - 2/3 \\
&\text{else} \\
&\qquad v'_{\text{B,ref}} = v_{\text{B,ref}} \\
&\text{end.}
\end{aligned} \tag{20}
$$

Taking into account the six-fold symmetry of the space-vector diagram, the general expression to obtain the updated reference signals in all possible locations of $\mathbf{V}_{\text{ref}}$ is

$$
\begin{aligned}
&\text{if}\left(v_{\max} - v_{\min} < 2/3\right) \\
&\quad v'_{\max} = v_{\max} \\
&\quad v'_{\text{mid}} = v_{\text{mid}} \\
&\quad v'_{\min} = v_{\min} \\
&\text{else} \\
&\quad v'_{\max} = v_{\max} - 2/3 \\
&\quad v'_{\min} = v_{\min} + 2/3 \\
&\qquad \text{if}\; v_{\text{mid}} < -2/9 \\
&\qquad\quad v'_{\text{mid}} = v_{\text{mid}} + 2/3 \\
&\qquad \text{elseif}\; v_{\text{mid}} > 2/9 \\
&\qquad\quad v'_{\text{mid}} = v_{\text{mid}} - 2/3 \\
&\qquad \text{else} \\
&\qquad\quad v'_{\text{mid}} = v_{\text{mid}} \\
&\qquad \text{end} \\
&\text{end.}
\end{aligned} \tag{21}
$$

Finally, the CM offset can be then found from (15), and the resulting modulating signals for the carrier-based implementation are given by (16).

Fig. 3 shows the modulating signals for the carrier-based implementation of the conventional SVPWM strategy in a 3L and 4L converter with $m = 1$. While the proposed approach yields the same modulating signals as given in [20], the generation of the reference signals involves the addition/subtraction operation instead of the modulo function, which reduces complexity. The methodology can be easily extended to converters with higher number of levels.

The proposed approach is based on a simple geometric formulation in terms of the reference signals. Using (6) for the 3L converter and (17)-(19) for the 4L converter, the sector region where the reference vector tip lies can be directly identified from the reference signal values. This can be useful to implement any PWM strategy requiring this identification.

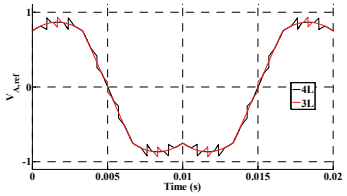

Fig. 3. Phase A modulating signals to implement conventional SVPWM in a 3L and 4L converter with $m = 1$.

In summary, Table I presents the steps of the proposed carrier-based implementation approach. The equation selected in step 3 depends on the converter number of levels. The equation selected in step 5 defines the implemented modulation strategy.

TABLE I
STEPS OF THE PROPOSED CARRIER-BASED IMPLEMENTATION APPROACH

Step	*Description*
1	Calculate $v_{X,\text{ref}}$ with (1)
2	Calculate v_{max}, v_{mid}, v_{min} with (3)
3	Calculate v'_{max}, v'_{mid}, v'_{min} with (13) (for 3L) or (21) (for 4L)
4	Calculate v''_{max}, v''_{mid}, v''_{min} with (14)
5	Calculate v_{off} with (15) (for conventional SVPWM)
6	Calculate $v''_{X,\text{ref}}$ with (16)

TABLE II
EXECUTION TIME FOR THE CARRIER-BASED IMPLEMENTATION OF CONVENTIONAL SVPWM

	Approach in [20]	*Proposed Approach*
3L Converter	3.1 µs	0.8 µs
4L Converter	3.1 µs	0.9 µs

To prove the advantages in computation time of the proposed approach, it has been compared with the approach in [20] to carrier-based implement the conventional SVPWM strategy for both 3L and 4L converters. The computation of the reference signals is performed in a TMS320F28335 digital signal controller, programmed from a C code. The execution time is found by setting and resetting a GPIO pin at the beginning and end of the computation, respectively. Table II presents the resulting execution time with both approaches. The proposed approach presents a significantly lower execution time, mainly because it does not require the use of the modulo function.

III. DISCONTINUOUS CBPWM

The conventional SVPWM strategy applies both redundant switching states for equal amount of time. However, there are other nearest-three-vector SVPWM strategies, which use only one of the redundant switching states in a switching cycle. For example, in a 3L converter, if switching state 100 is not used for a reference vector in sector 1-subsector *b*, the applied sequence of switching states will be 211-210-200. This sequence clamps phase A to the positive dc-link terminal. Thus, phase A does not switch in the switching cycle. These PWM strategies are known as DPWM strategies. The DPWM strategies can also be carrier-based implemented by adding a proper CM offset to the original normalized phase-voltage reference signals.

For a 2L converter, to clamp the phase with the minimum voltage value to the negative dc-link terminal, the CM offset is given by

$$v_{\text{off}} = -1 - v_{\text{min}} \tag{22}$$

and to clamp the phase with the maximum voltage value to the positive dc-link terminal, the CM offset is given by

$$v_{\text{off}} = 1 - v_{\text{max}} \tag{23}$$

Similarly, for a multilevel converter, the reference signals corresponding to the small hexagon can be used to calculate the CM offset to implement a DPWM strategy. If the CM offset is given by

$$v_{\text{off}} = \frac{-1}{n-1} - v''_{\text{min}}, \tag{24}$$

the phase with the minimum updated reference signal does not switch in the switching cycle, and if the CM offset is given by

$$v_{\text{off}} = \frac{1}{n-1} - v''_{\text{max}}, \tag{25}$$

the phase with the maximum updated reference signal does not switch in the switching cycle.

For the 2L converter, there are six types of different DPWM reference signals that can be broadly classified into three groups: 120°-clamped, 60°-clamped, and 30°-clamped DPWM [25].

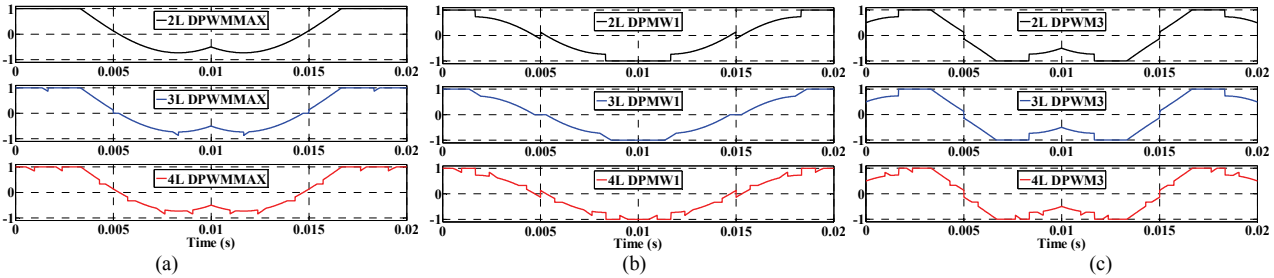

Fig. 4. Phase A reference signal in a 2L, 3L, and 4L converter at $m = 1$ for (a) DPWMMAX, (b) DPWM1, (c) DPWM3.

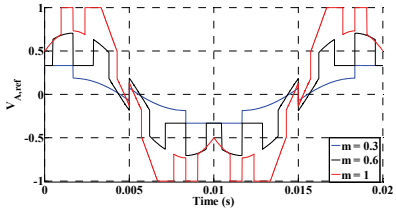

Fig. 5. Phase A reference signal for NDPWM1 in a 4L converter at $m = 0.3$, $m = 0.6$, and $m = 1$.

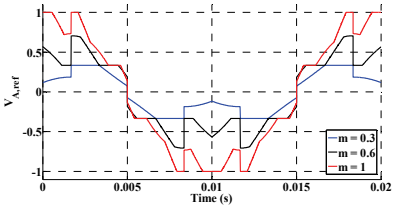

Fig. 6. Phase A reference signal for NDPWM3 in a 4L converter at $m = 0.3$, $m = 0.6$, and $m = 1$.

If the CM offset added to the reference signals is given by (24) for every switching cycle, the DPWM strategy is called 120°-clamped DPWMMIN. On the other hand, if the CM offset added to the reference signals is given by (25) for every switching cycle, the DPWM strategy is called 120°- clamped DPWMMAX. The phase A reference signal for 120°-clamped DPWMMAX is given in Fig. 4(a) in a 2L, 3L, and 4L converter at $m = 1$.

In 60°-clamped DPWM for a 2L converter, each phase is clamped for 60° twice in a fundamental cycle. Depending on the location of the clamping period, three types of 60°-clamped DPWM are identified in [25] which are designated as DPWM0, DPWM1, and DPWM2. For the sake of simplicity, only DPWM1 will be considered here. In a 2L converter, DPWM1 can be implemented by adding the following CM offset

$$v_{\text{off}} = \begin{cases} -1 - v_{\min}, & (v_{\text{mid}} > 0) \\ 1 - v_{\max}, & (v_{\text{mid}} < 0) \end{cases} \tag{26}$$

In 30°-clamped DPWM for a 2L converter (also known as DPMW3), each phase is clamped for 30° four times in a fundamental cycle. In a 2L converter, DPWM3 can be implemented by adding the following CM offset

$$v_{\text{off}} = \begin{cases} 1 - v_{\max}, & (v_{\text{mid}} > 0) \\ -1 - v_{\min}, & (v_{\text{mid}} < 0) \end{cases} \tag{27}$$

In a multilevel converter, according to the analysis presented in Section II, the CM offsets for DPWM1 and DPWM3 can be readily derived and are given by

$$v_{\text{off}} = \begin{cases} -\dfrac{1}{n-1} - v''_{\min}, & (v_{\text{mid}} > 0) \\ \dfrac{1}{n-1} - v''_{\max}, & (v_{\text{mid}} < 0) \end{cases} \tag{28}$$

and

$$v_{\text{off}} = \begin{cases} \dfrac{1}{n-1} - v''_{\max}, & (v_{\text{mid}} > 0) \\ -\dfrac{1}{n-1} - v''_{\min}, & (v_{\text{mid}} < 0) \end{cases}, \tag{29}$$

respectively. Figs. 4 (b) and (c) present phase A reference signal for DPWM1 and DPWM3 in a 2L, 3L, and 4L converter at $m = 1$. The CM offset selection depends on the value of v_{mid}. Another way to choose the CM offset can be based on v''_{mid}, and this yields the following CM offsets

$$v_{\text{off}} = \begin{cases} -\dfrac{1}{n-1} - v''_{\min}, & (v''_{\text{mid}} > 0) \\ \dfrac{1}{n-1} - v''_{\max}, & (v''_{\text{mid}} < 0) \end{cases} \tag{30}$$

and

$$v_{\text{off}} = \begin{cases} \dfrac{1}{n-1} - v''_{\max}, & (v''_{\text{mid}} > 0) \\ -\dfrac{1}{n-1} - v''_{\min}, & (v''_{\text{mid}} < 0) \end{cases}, \tag{31}$$

which define two novel DPWM strategies, designated as NDPWM1 and NDPWM3, respectively. In the 3L case and for $m < 1$, $v_{\text{mid}} > 0$ implies $v''_{\text{mid}} < 0$. Therefore, in this case DPWM1 is equal to NDPWM3, and DPWM3 is equal to NDPWM1. However, this does not hold in a 4L converter, where all four DPWM strategies are different. Thus, (30) and (31) generate new DPWM strategies. Fig. 5 and Fig. 6 present the phase A reference signal for the proposed DPWM strategies at $m = 0.3$, $m = 0.6$, and $m = 1$. While Fig. 4 present the same modulating signals given in [20] and [21], where the clamping period depends on the v_{mid} value, Figs. 5-6 present new DPWM strategies where the clamping period depends on the v''_{mid} value.

Fig. 7 presents a comparison of the harmonic distortion of the different 4L PWM strategies for the linear range of the modulation index ($m \in [0, 1.15]$). The normalized weighted total harmonic distortion (NWTHD) [20] is plotted as a function of the modulation index for a carrier frequency equal to 10 kHz. The NWTHD is calculated as

$$NWTHD(\%) = \frac{2\sqrt{2}}{\sqrt{3}} \frac{\sqrt{\sum_{h=2}^{\infty} \left(\frac{V_{h,LL}}{h} \right)^2}}{v_{dc}} .100 \qquad (32)$$

where $V_{h,LL}$ is the rms value of the hth harmonic of the line-line voltage. The conventional SVPWM strategy has the least NWTHD. However, among the DPWM strategies, NDPWM3 gives the least NWTHD. The NWTHD for DPWM1 and NDPWM1 are the same at low modulation index values because v_{mid} and v''_{mid} are equal in this modulation index range. The same behavior can be observed for DPWM3 and NDPWM3.

Overall, the main advantages of the proposed approach can be summarized as follows:

1. The proposed approach is based on simple geometric equations. Thus, it is easy to understand.
2. The proposed approach requires less computational effort than previous PWM modulation implementation approaches, because only if-then-else instructions and additions are used to calculate the CM offset.
3. Since the CM offset is derived from SVPWM theory, the proposed approach is general, allowing the implementation of all existing competitive PWM methods for any number of dc-link levels.
4. The proposed approach enables the proposal of new modulation strategies such as NDPWM1 and NDPWM3, which naturally arise from the proposed approach rationale.

IV. Simulation and Experimental Results

A MATLAB-Simulink model has been developed for the 4L converter. The dc-side of the converter is supplied by three independent 50 V voltage sources. The ac-side is connected to a balanced three-phase load with 16.5 Ω resistance in series with 10 mH inductance per phase. The carrier frequency is 10 kHz. Previous works in [20] and [21] have reported the ac-side waveforms with DPWM1 and DPWM3. Therefore, the results with NDPWM1 and NDPWM3 at two modulation index values are presented in Figs. 8-9.

A prototype of a four-level three-leg diode-clamped dc-ac converter with FDPF3860T (100 V, 20 A) metal-oxide semiconductor field-effect transistors (MOSFETs) has also been used to test the proposed modulation strategies. The modulator algorithm is implemented with dSpace processor board DS1006. A picture of the experimental setup is shown in Fig. 10. The converter is operated with the same dc-source, three-phase ac load, and carrier frequency employed in the simulations. Figs. 11-12 present the experimental results corresponding to the simulation results of Figs. 8-9. As can be observed, the experimental and simulation results are in good agreement. For instance, the duration for which the line-to-negative terminal voltage remains constant is the same in both cases. A frequency domain analysis of the experimental line-line voltage and line current waveforms has been performed applying the Fast Fourier Transform (FFT) algorithm. Fig. 13 and Fig. 14 present the corresponding frequency spectrum, for both NDPWM1 and NDPWM3, where the amplitude of the most relevant harmonics around the carrier frequency and twice the carrier frequency are depicted. The experimental line-line voltage NWTHD, calculated from the complete FFT analysis results, is presented in Table III. The experimental results from Table III are also in agreement with the simulation results from Fig. 7.

The voltages between adjacent input terminals at the dc-link should be balanced for proper operation. Several dc-link voltage balancing techniques have been studied in the literature. The PWM methods discussed in this paper do not have comprehensive dc-link voltage balancing capability and assume that the dc-link voltage balance is guaranteed by either additional external balancing circuits [28], [29], or by the availability of separate regulated voltage sources.

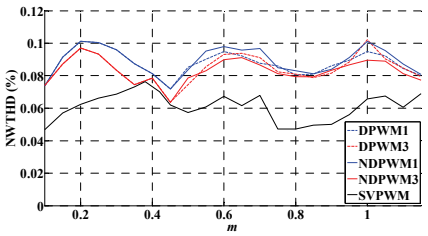

Fig. 7. Harmonic distortion of different PWM strategies for the 4L converter.

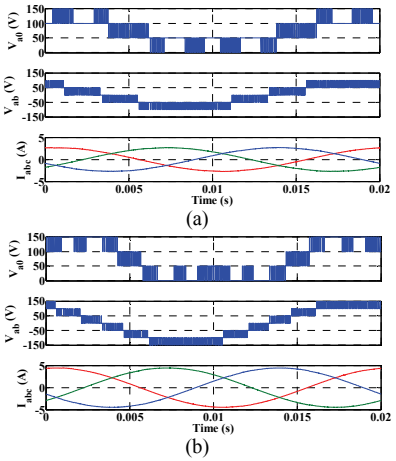

Fig. 8. Simulation results for the line-to-negative terminal of the dc supply voltage (v_{A0}), the line-line voltage (v_{AB}), and the phase currents for a 4L converter operated with NDPWM1. (a) $m = 0.6$. (b) $m = 1$.

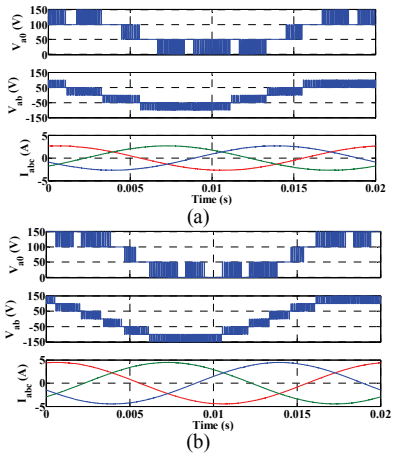

Fig. 9. Simulation results for the line-to-negative terminal of the dc supply voltage (v_{A0}), the line-line voltage (v_{AB}), and the phase currents for a 4L converter operated with NDPWM3. (a) m = 0.6. (b) m = 1.

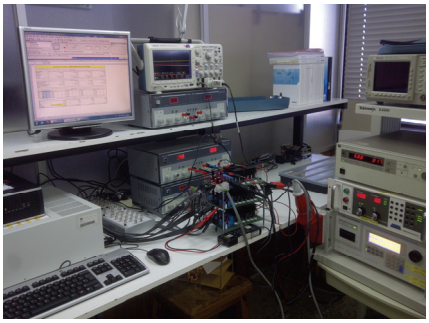

Fig. 10. Experimental setup.

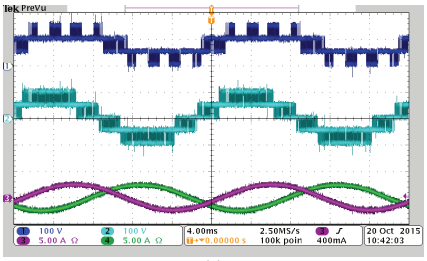

Fig. 11. Experimental results for the line-to-negative terminal of the dc supply voltage (v_{A0}), the line-line voltage (v_{AB}), and the phase currents for a 4L converter operated with NDPWM1 at (a) m = 0.6. (b) m = 1.

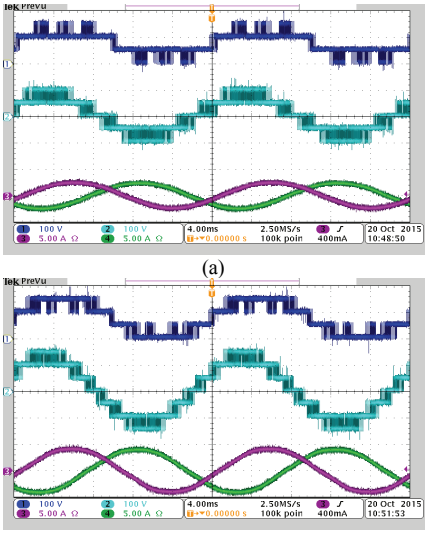

Fig. 12. Experimental results for the line-to-negative terminal of the dc supply voltage (v_{A0}), the line-line voltage (v_{AB}), and the phase currents for a 4L converter operated with NDPWM3 at (a) m = 0.6. (b) m = 1.

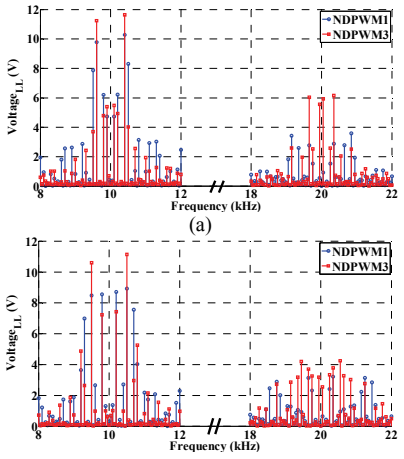

Fig. 13. FFT plot of the line-line voltage (v_{AB}) for NPWM1 and NDPWM3 at (a) m = 0.6 and (b) m = 1.

TABLE III
NWTHD FROM THE EXPERIMENTAL WAVEFORMS

	m	*NWTHD*
NDPWM1	0.6	0.13%
NDPWM1	1.0	0.12%
NDPWM3	0.6	0.125%
NDPWM3	1.0	0.126%

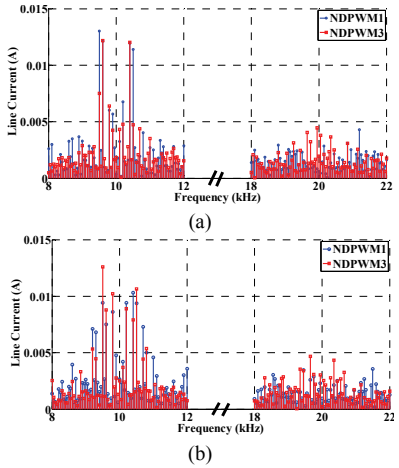

Fig. 14. FFT plot of the line current (i_A) for NPWM1 and NDPWM3 at (a) m = 0.6 and (b) m = 1.

V. Conclusion

A novel method to generate effective carrier-based PWM strategies for multilevel diode-clamped dc-ac converters has been presented. The method is based on the conversion of high performance space-vector-based PWM strategies into a carrier-based format in light of the correspondence between space vectors and modulating waveforms.

The proposed method allows the implementation of existing PWM strategies with reduced complexity and computation time. The implementation is demonstrated for three- and four-level converters, but the method can be extended to converters with higher levels.

In addition, the proposed method enables the development of new modulation strategies. To demonstrate this, two new DPWM strategies for a four-level converter have been proposed. From the comparison of the proposed DPWM strategies to other known DPWM strategies, it is found that one of the proposed DPWM strategies produces the least WTHD.

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