A Novel Approach to Accurately Determine the tq Parameter of Thyristors

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HAL Id: hal-01617496
https://hal.science/hal-01617496

Submitted on 18 Nov 2019

A Novel Approach to Accurately Determine the t_q Parameter of Thyristors

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Abstract—**The continued use of high-voltage thyristor devices in industry and their increased use in high-voltage dc transmission systems call for more attention to the properties of these devices. One of the important thyristor parameters is their turn-off time t_q, which can be a limiting factor when applying thyristors at elevated switching frequencies. Hence, the accurate measurement of t_q and its variation versus the operating conditions remains a crucial task for thyristor converters operating at elevated switching frequencies. In this paper, a proper test circuit for measuring this parameter with a high level of accuracy has been designed and built. Owing to the test circuit specificity, the variation effects of several electrical and physical constraints, such as the forward current, I_F, the reverse applied voltage, V_R, the operating temperature, T_o, and the ramp rate of the forward reapplied voltage, dV_D/dt, on the t_q parameter of Thyristors are also studied and analyzed based on the physics of semiconductor devices and associated simulations.**

Index Terms— **Finite element method (FEM), modeling, simulation, thyristors.**

I. INTRODUCTION

SILICON (Si) Thyristors continue to be largely used in high power applications [1]–[4], such as the High-voltage direct-current (HVDC) power systems. These HVDC power systems are exposed to a high risk of failures by their predisposition to lightning strikes or short circuits. Due to its robustness against surges induced by lightning strikes, thyristors are among the most suitable components to be used in HVDC power systems and line commutated converters [4]–[10]. However, one of the limiting factors for thyristors operating at elevated switching frequencies is their circuit-commutated turn-off time t_q, defined as the time from the instant of zero-current-crossing (at which the reverse recovery current begins to flow) until the instant when forward blocking voltage can be reapplied across the thyristor without turning it on. Knowledge of the turn-off time is mandatory in all hard switching power circuits as well as in circuits whose operating

frequency exceeds a few kHz. Immunity against parasitic triggering agents, such as a dV_D/dt greater than the critical value, that increase the junction temperature are other important features.

The accurate knowledge of t_q is very important when thyristors are used in phase-commutated converters and a.c. converters.

Some studies that focused on t_q have been published in the literature [11]–[14], but most of them did not give sufficient details about the measurement procedure of t_q. In addition, the t_q value is only provided on datasheets for some commercial Thyristors for some operating conditions [15]–[17], whereas in [18], t_q values are only given at room temperature and 125°C and no further information is given about other measurement conditions. Also, no details are given for the t_q measurement procedure of the commercial Thyristors in datasheets [15]–[18]. Therefore, in this paper, we intend to develop a novel approach to enable a measurement with a high level of accuracy for the turn-off time, t_q, versus the main operating conditions imposed by the external circuit of the Thyristor as well as to analyze the t_q parameter and its dependency on the main operating conditions using numerical device simulations. Section II describes the test circuit designed and built to accurately measure t_q. In this section, the measurement procedure algorithm is also discussed in detail. A physics-based study of this parameter (t_q) is the focus of this study. The critical levels of the hole density distribution and the hole current density distribution that enables the triggering of the Thyristor conduction process are obtained through the modeling and mixed-mode simulation of an adequate test circuit as described in section III. In section IV, a physical analysis of t_q through a numerical simulation is given. There is also focus on the behavior study of t_q as a function of the physical quantities imposed by the external circuit of Thyristor. In section IV, the t_q dependencies of the device under test (DUT) as a function of the main physical quantities, such as the average on-state current (I_F), the operating temperature (T_o), the reverse applied voltage (V_R), and the ramp rate of the forward reapplied voltage (dV_D/dt), imposed by the test circuit are also described, analyzed, and discussed based on the physics of the component. The paper concludes with section V.

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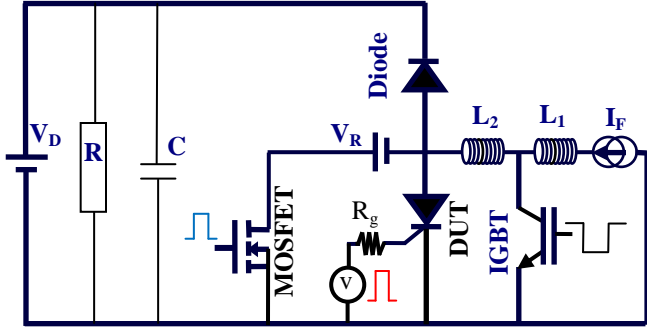
II. TEST SETUP FOR t_q MEASUREMENT

To accurately measure the t_q of Thyristors, a test setup has been designed and built. The circuit of the test setup is given in Fig. 1.

Fig. 1. Schematic of the experimental circuit for the Thyristor t_q measurement (V_D= 27 V, R= 10 kΩ, C= 1μF, L_1=54 mH includes an air-core (4 mH) plus an iron-core (50 mH) inductors. L_2~ 100 nH is a twist pair).

TABLE I

BASIC ABSOLUTE MAXIMUM RATINGS OF THE COMPONENTS AND MAIN SWITCHING CHARACTERISTICS OF THE DEVICES (RISE TIME, t_r, TURN-ON DELAY TIME, $t_{D(on)}$, FALL TIME, t_f, TURN-OFF DELAY TIME, $t_{D(OFF)}$ OF IGBT AND MOSFET AND REVERSE RECOVERY TIME, t_{rr} OF THE PIN DIODE)

Devices	Main Switching Characteristics (Typical) from datasheets				Basic Absolute Maximum Ratings
IGBT(FGL60N 100BNTD)	t_r 320 ns	$t_{D(ON)}$ 140 ns	$t_{D(OFF)}$ 630 ns	t_f 130 ns	1000 V, 60 A
MOSFET (IRF740)	t_r 25 ns	$t_{D(ON)}$ 15 ns	$t_{D(OFF)}$ 52 ns	t_f 25 ns	400 V, 10 A
PiN Diode (MUR8100)	t_{rr} 50 ns				1000 V, 8 A

In this section, the operation of the designed test setup is also described in detail.

The built test setup includes two dc-voltage sources and a dc-current source imposing the main conditions of the switching cell operation (V_R, I_F). An insulated gate bipolar transistor (IGBT) transistor, a PIN diode and a MOSFET transistor are also used as switches in the test circuit along with the DUT. The basic absolute maximum ratings and the main switching characteristics of these switches are given in Table I.

The turn-on and turn-off transient behavior of DUT are mainly controlled by the MOSFET transistor instead of using a second thyristor as published in the literature [14], [19], and [20]. To obtain a pertinent thyristor turn-off for the accurate measurements of t_q, a fast MOSFET transistor (IRF740) is chosen as a control switch. As the switching cell includes controlled switches, the characteristics of the driving circuit of the switch are important in terms of switching speed in order to control the dV_D/dt of the DUT. A driving circuit delivering three synchronized pulses has been designed. The three pulses are applied to the gate of the IGBT transistor, MOSFET transistor, and the DUT. The detailed control timing diagram is shown in Fig. 2.

The inductor, L_1, is a wide-bandwidth aircore inductor that ensures a constant current during the switching cell operation. A similar inductor of a smaller value, L_2, disconnects the IGBT of the switching cell during DUT transients.

To measure the t_q parameter of thyristors at a controlled temperature from an experimental point of view, it is necessary to limit the thyristor self-heating by using a very
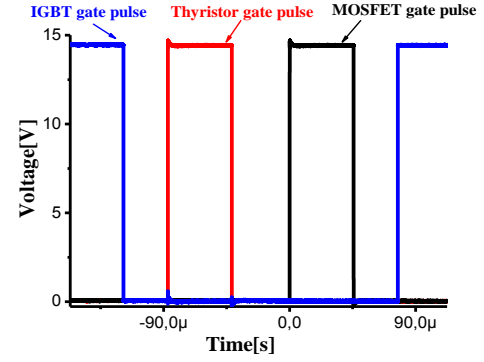

Fig. 2. Experimental control signal for IGBT, MOSFET and the Thyristor gate.

low recurrence operation. Indeed, due to its robustness, the IGBT transistor ensures the greatest part of the power dissipation that handles the I_F forward current most of the time but it has no role for the DUT switching. Therefore, the MOSFET transistor, DUT, and PIN diode components are relieved by the IGBT transistor. The IGBT is turned off during about 200 μs every 100 ms. Once the IGBT transistor is turned off, the PIN diode is turned on to ensure the continuity of the current. The PIN diode will then be in a freewheeling operation mode, and the DUT is forward biased by a V_D voltage plus the diode voltage drop. To stabilize the voltage supplied by the dc-voltage source, V_D, a ceramic and polypropylene capacitor, C, is added in parallel with the voltage generator; however, during the PIN diode conduction phase, the V_D voltage generator must consume energy when the capacitor is charged. Since the voltage source V_D is not bidirectional in current, certain issues may arise at high levels of current; to mitigate this problem, a parallel resistance R is placed across the voltage source.

A. The t_q measurement procedure

The t_q parameter of the DUT is measured repetitively in a three-stage cycle as shown in Fig.3.
First, a trigger pulse delivered by the driving circuit turns the DUT on, which is initially forward biased after having turned off the freewheeling diode. Thus, an I_F forward current is established through the thyristor and a forward voltage drop, V_{TM}, is obtained across its terminals. The second phase begins when a second pulse is applied to the MOSFET transistor gate, triggering its conduction mode during a time slot, T_{off}. This action connects the dc-voltage source, V_R, across the thyristor such that the sudden reverse bias cuts off its I_F forward current, and the total current flows through the MOSFET transistor. At the start of the thyristor reverse biasing, there is a fast-rising reverse current pulse that reaches a peak and decays, and the conduction mode of the DUT ceases temporarily. This reverse current is due to the recombination and evacuation of charges stored in the lightly doped region of the thyristor during its conduction phase. For the last step, a forward voltage is reapplied across the DUT with a ramp rate, dV_D/dt, controlled by adding capacitors in parallel to the MOSFET transistor. This phase is initiated when the MOSFET transistor is turned off.
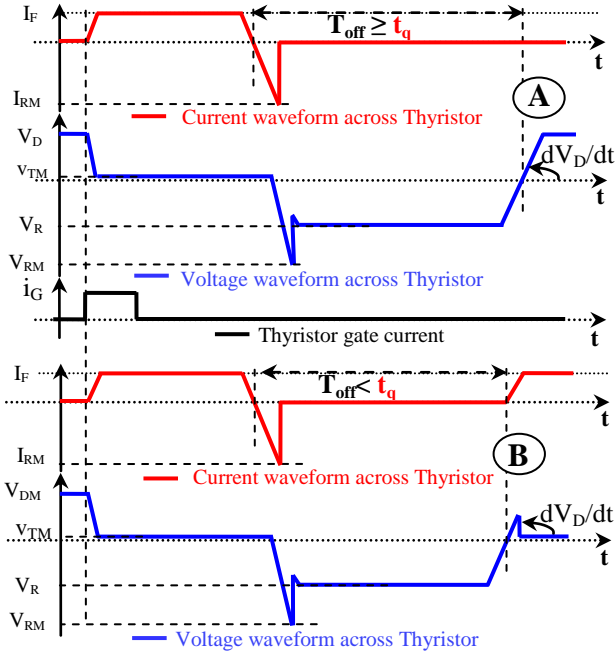
Fig. 3. Typical waveforms of current and voltage across the Thyristor during three transient phases for two possible behaviors (A and B).

Fig. 4. Measurement procedure algorithm

As shown in Fig. 3, two potential behaviors of the thyristor are distinguished. For the A and B behaviors, a lapse of time, T_{off}, is computed from the instant when the forward current crosses the zero value near the start of the reverse bias until the instant when the voltage across the thyristor becomes positive. For the B-behavior state, the thyristor conduction process is triggered when the forward reapplied voltage V_D across the thyristor goes positive; however, under the same operating conditions except for a larger T_{off}, the thyristor remains turned off, as shown for the A-behavior state. The turn-off time, t_q, is determined as the maximum time of T_{off} for which the first change is detected from B to the A behavior state by gradually increasing the T_{off} time. The main physical quantities imposed by the test circuit and affecting t_q are defined in Table II.

TABLE. II
DEFINITION OF THE MAIN PHYSICAL QUANTITIES IMPOSED BY THE TEST CIRCUIT AND AFFECTING t_q

Parameters	Definition
I_F	Thyristor forward current
T_o	Thyristor operating temperature
V_R	Reverse applied voltage across Thyristor during its turn-off transient behavior
dV_D/dt	Ramp rate of the forward reapplied voltage across Thyristor

B. t_q measurement

From an experimental point-of-view, a measurement procedure algorithm is developed to accurately measure the t_q parameter of each DUT, as illustrated in Fig. 4.

This measurement procedure includes three steps. In step #1, the DUT takes place in the test setup with the desired operating conditions (V_R, I_F, T_o, dV_D/dt) such that $dV_D/dt <$ (dV_D/dt)$_{critical}$. Step #2 involves the T_{off} initialization with a very small value for which the B behavior state is valid for the DUT corresponding to the triggering of its conduction mode during the reapplication of the forward voltage, V_D, across it.
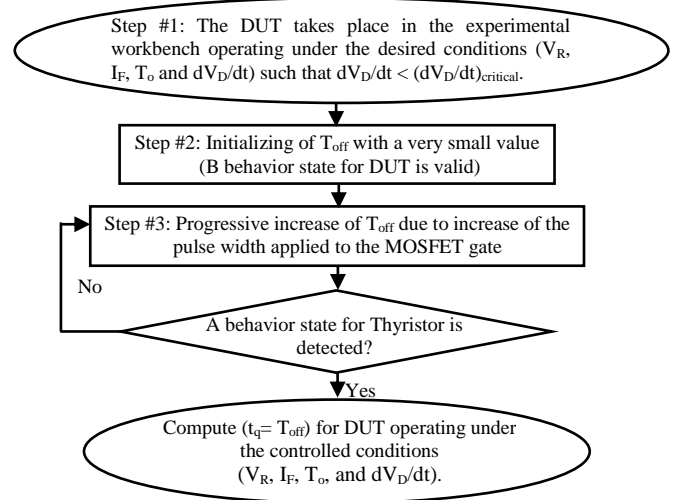
Step #3 involves a progressive increase of T_{off} automatically due to the increase of the pulse width applied to the MOSFET gate, and the behavior state of the component is checked each time. Once the A behavior state of the thyristor is obtained for the first time, the t_q value of the DUT is computed for the desired conditions of (V_R, I_F, T_o, dV_D/dt) fixed at the beginning of the measurement procedure algorithm. The experimental current and voltage waveforms across the thyristor (2N6508G) during its transient behavior for the two values of T_{off} ($T_{off} = t_q$ and T_{off} slightly lower than t_q) corresponding to the two behavior states are described in Fig. 5.

Under the operating conditions ($I_F = 2$ A, $V_R = 100$ V, $dV_D/dt = 980$ V/μs and $T_o = 27$ °C), and when the pulse width applied to the MOSFET gate is slightly increased, the thyristor behavior state A occurs for $T_{off} = t_q$ instead of the behavior state B. Therefore, the t_q parameter of the thyristor (2N6508G) is deduced when moving abruptly from the B behavior state to A for a change of 0.1μs for T_{off}. This leads to an accurate measurement of the t_q ($t_q = 46.0$ μs) of the thyristor (2N6508G) with a sensibility of 0.2%. From an experimental point of view, the current and voltage waveforms of the DUT are measured using two voltage probes and a current shunt. The designed and built test setup that measures t_q offers the possibility to independently control all rates and amplitudes of the most influential electrical quantities. Compared to other recent research studies in the literature [21], [22], the test setup presented in this paper is efficient because of the direct control of I_F, V_R, dV_D/dt, and T_o.

To control T_o of the DUT, the experimental circuit is equipped with a thermal management unit, TP041AH, where the temperature is monitored by a thermocouple and controlled by a microprocessor regulating the air stream temperature with high stability and accuracy. From an experimental point of view and while keeping three parameters among (I_F, V_R, dV_D/dt, and T_o) constant, the t_q behaviors versus the fourth parameter could thus be studied for this paper. In this section, the t_q measurement principle is described, and the test setup operation is discussed in detail. The device numerical simulation is of great importance for explanation and analysis of its behavior, as previously discussed in the literature for the
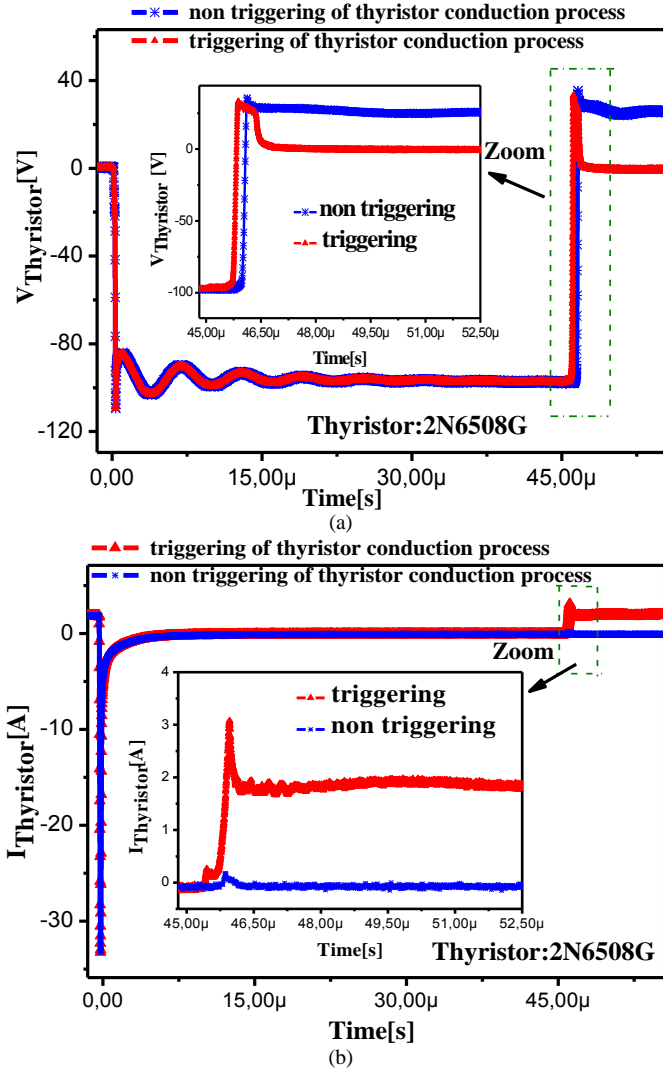
Fig. 5. Experimental A and B behavior states of DUT for (I_F = 2 A, V_R = 100 V, dV_D/dt = 980 V/µs and T_o = 27 °C) for two values of T_{off} ($T_{off} = t_q$ (non-triggering of Thyristor) and a T_{off} slightly lower than t_q (Thyristor triggering)). (a) Experimental voltage waveforms across DUT for the two values of T_{off}. (b) Experimental current waveforms across DUT for the two values of T_{off}.

thyristor turn-on [23]. To further study the physics behind the t_q parameter, it is important to use finite element methods (FEM) simulators to simulate the thyristor behavior when a voltage is reapplied across it as it is nearing its turn-off phase. Indeed, the behavior of carrier distributions inside the device structure of the component for the two values of T_{off} ($T_{off} = t_q$ and T_{off} slightly lower than t_q corresponding to the two behavior states, A and B) should be described and analyzed. In addition, to analyze and discuss the t_q behaviors as a function of the physical quantities imposed by the experimental test circuit, a simulation of a stored charge density behavior versus the main physical constraints is also necessary. The modeling of the test setup, including the accurate modeling of physical phenomena governing the DUT operation, particularly during the three phases previously described, will thus be addressed.

III. EXPERIMENTAL TEST CIRCUIT MODELING

To obtain accurate simulated results, the same methodology developed in [24] and [25] for the parasitic wiring model of
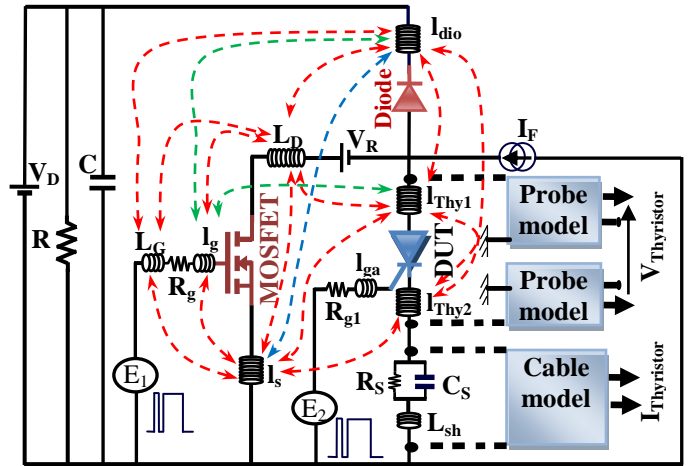

Fig. 6. Complete circuit model including a parasitic wiring model and probe models.

the test setup is considered using the partial element equivalent circuit method [26]. The complete circuit model, which takes into account the self and mutual inductances of the layout, shunt, probe, and cable models, is shown in Fig. 6. In this figure, the mutual effects between inductances of the circuit are represented by arrows. Since the turn-on and turn-off of the thyristor is mainly controlled by the MOSFET transistor, an advanced MOS2KP model developed in the literature [27] is considered in the test circuit modeling. As the experimental test circuit to be simulated includes several semiconductor devices, it is not clear whether the simulation of the complete experimental test circuit using the FEM could be supported due to simulation overhead costs; however, because it supports Mixed-Mode simulation, the experimental test circuit shown in Fig. 6 is implemented in the FEM simulator, DESSIS-ISE TCAD [28].

All of the components are simulated as equivalent circuit models except the thyristor device. For this DUT, the FEM model is used because on one hand, a high level of accuracy is required to obtain simulation results as close as possible to the experimental results. On the other hand, the behavior of the charge carrier distributions stored in the central region of the component during the reapplication of a forward voltage across it at the end of its turn-off phase is essential for the analysis of the physical phenomenon of the t_q parameter of the thyristor. To meet these requirements, three commercial thyristors are selected to be used as reference devices for the simulation results. The design parameters of these thyristors, illustrated in Table III, have been accurately extracted using the approach described in the literature [29]. The thyristor design parameters are defined in Fig. 7.

For the FEM modeling of the thyristor, the effective intrinsic density model established by Bennet Wilson [30] and the Philips unified mobility model proposed by Klassen et al. [31] are used. The temperature dependence is included for the lattice mobility [32], for the Shokley–Read–Hall lifetimes [33] and for the carrier intrinsic concentration [34]. The avalanche effects are also taken into account. The latter options are adequate for the simulation of power semiconductor devices. They are not discussed here since these issues are beyond the scope of this paper.

Thyristor	2N6508G	2N6397G	BT153
Maximum forward voltage	600 V	400 V	500 V
Nominal current	25 A	12 A	5 A
N_B (cm^{-3})	2.3×10^{14}	6×10^{14}	4×10^{14}
W_B (µm)	41	23	32
N_g (cm^{-3})	1.95×10^{17}	1.15×10^{17}	1.4×10^{17}
W_g (µm)	4.2	6	5
A (mm^2)	35	28	33.6
τ (µs)	9	5	8

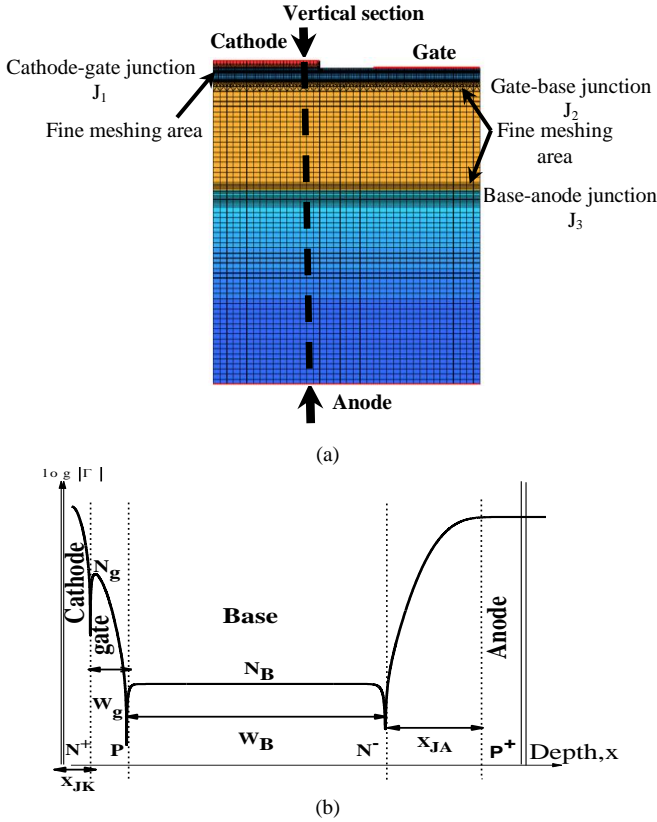| Parameters	Definition
I_S	Triggering current of the regenerative action necessary for the forward conduction mode of Thyristor
I_H	Thyristor holding current corresponding to the initiation point of the high level injection regime

(a)

(b)

Fig. 7. Simplified 2-D structure of the Thyristor. (a) 2-D structure of a Thyristor. (b) Thyristor doping profile from cathode to anode.

The architecture in Fig. 7 is implemented using the graphical tool, MDRAW-ISE TCAD [35]. A meshing tool produces the necessary data for DESSIS-ISE TCAD, such as the doping profile and the geometric structure of the component. A fine meshing is accomplished in J_1, J_2, and J_3 junctions, as shown in Fig. 7(a). The Thyristor is turned on if a sufficient amount of holes is injected by the driven circuit in its P-gate region, leading to the triggering of the regenerative action necessary to its forward conduction mode [36].

This threshold amount of injected holes corresponding to a critical current of holes in the P-gate region is reached when the Thyristor forward current is exactly equal to the triggering current, I_S, defined in Table IV. Once, this current level is reached, the charges stored in the lightly doped region of the Thyristor abruptly and considerably increase, thus reaching

the high level-injection regime, while the forward current becomes equal to I_H, which is defined in Table IV.

The current I_S is directly related to the t_q parameter of the component. The critical levels of the hole density and the hole current density distributions inside the Thyristor geometric structure corresponding to the triggering current I_S could be easily selected after having simulated the test circuit presented in Fig. 8(a) using DESSIS-ISE TCAD simulator. The I_H and I_S currents are shown in Fig. 8(b).

As shown by the control timing diagram of the voltage pulse, V_D and V_g in Fig. 8(a), the MOSFET is initially conducting, and the conduction process of the DUT is triggered by a fast ramp rate, dV_D/dt. The MOSFET will then be used as a controlled resistor. Indeed, by gradually reducing the voltage magnitude applied to the MOSFET gate, the current crossing the DUT decreases.

The simulated I-V characteristic of Fig. 8 shows the snap back region of the component. As presented in Fig. 8(b), the value of the device current I_S can be deduced. This current value is totally independent from the V_D value. This value is in good agreement with the experimental value. Using the experimental test circuit presented in Fig. 1, the regenerative action necessary for the forward conduction of the DUT is no longer maintained for any forward current $I_F < I_S$. For the I_S current, the hole density distribution and the hole current density distribution inside the geometric structure of the DUT are simulated and given in Fig. 8(c). These critical levels of the hole density and the hole current density distributions will be used later as reference levels enabling the triggering of the regenerative action necessary to the Thyristor conduction process.

IV. RESULTS AND DISCUSSION

A. Physics-based analysis of t_q

The t_q values of the commercial Thyristors under test obtained by simulation are almost identical to those given by the experiment as shown in Table V and as clearly illustrated for the Thyristor (2N6508G) in Figs. 9(a) and 9(a').

In datasheets of DUT, the dV_D/dt, I_F and V_R conditions are not specified that may explain the disagreement between the typical values of t_q from datasheets and the t_q values extracted by experiment and simulation. The hole density distributions and their current density distributions inside the geometrical structure of the Thyristor (2N6508G) for various instants during the reapplication of a forward voltage across it for two cases ($T_{off} = t_q$ and T_{off} slightly lower than t_q corresponding respectively to the A and B behavior states of the DUT) are simulated and given in Figs. 9(b), (b'), (c) and (c'). Once the
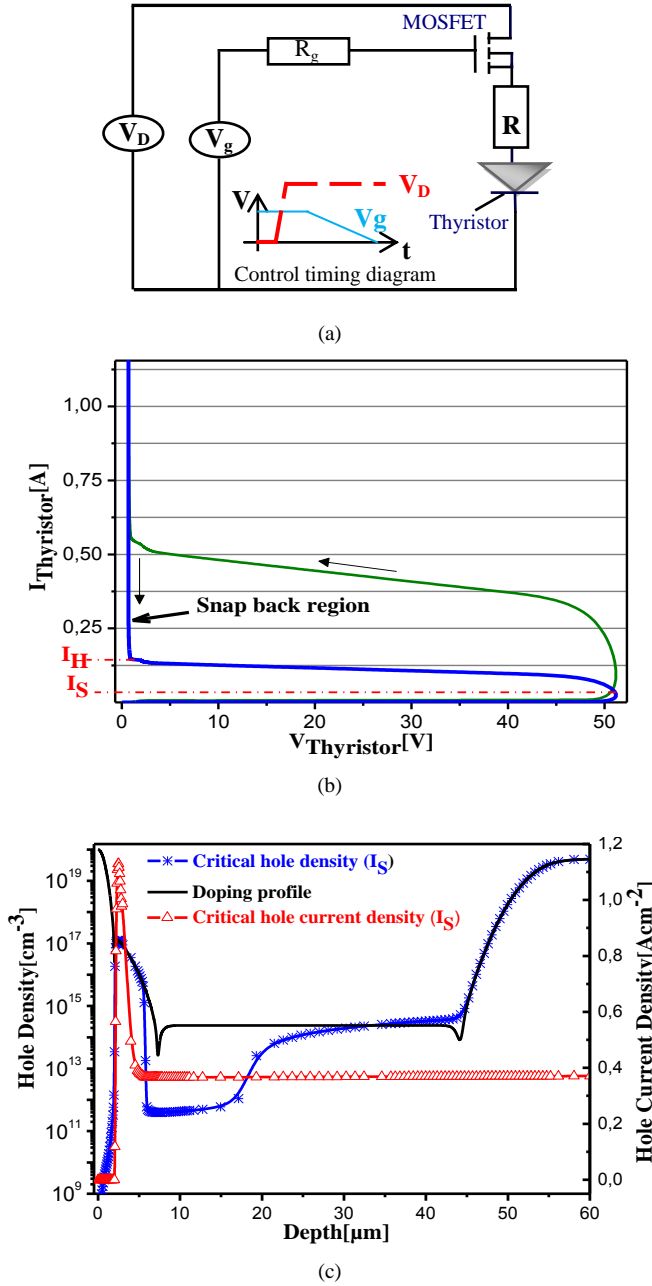
(a)

(b)

(c)

Fig. 8. Extraction of the critical hole density distribution and its critical current density distribution of the thyristor (2N6508G). (a) Simulated test circuit extracting I_H and I_S. (b) I-V characteristics. (c) Critical hole density distribution and its critical current density distribution of the Thyristor (2N6508G).

Table V

EXPERIMENTAL AND SIMULATED VALUES OF THE t_q PARAMETER FOR THREE COMMERCIAL THYRISTORS OPERATING UNDER THE FOLLOWING CONDITIONS (V_R = 100 V, T_o = 27 °C, dV_D/dt = 980 V/µs and I_F = 2 A) AND THEIR TYPICAL VALUES OF t_q FROM DATASHEETS (T_o = 27 °C)

Thyristors	Typical value of t_q(µs) from datasheets	t_q value (µs) experiment	t_q value (µs) simulation	Error between simulation and experiment (%)
2N6508G	15	46	45.65	0.7
BT153	15	40.1	39.7	1
2N6397G	15	30	29.6	1.3

thyristor is reverse biased by the voltage generator (V_R), an amount of charges stored in the Thyristor base region during its conduction mode is swept out; however, at instant t_1, the

time of the reapplication of the forward voltage across it, a residual amount of hole minority carriers still exists inside the component base region. Instant t_0 corresponds to the end of the steady state reverse blocking. From instant t_1, the voltage generator (V_D) begins to be reapplied across the DUT with a ramp rate, dV_D/dt, lower than the critical one. Therefore, the anode-base junction J_3 and the cathode-gate junction J_1 become forward biased, while the gate-base junction J_2 becomes reverse biased. Also, an amount of hole carriers injected from the anode to the base region is added to the residual amount of the holes inside the thyristor base region. From instant t_1 to t_2, the voltage across DUT increases to reach exactly at instant t_2, the forward reapplied voltage, V_D, thus increasing the hole density injected from the thyristor anode region as illustrated in Fig. 9.

The hole concentration gradient in the thyristor base region of the anode side is thus obtained From instant t_2 to t_4, the V_D voltage is supported by DUT and the stored holes obtained in the component base region diffuse towards the reverse biased junction J_2, where they are driven by the electric field extended through this junction into the thyristor P-gate region. For any instant greater than t_4, if the critical level of the hole density and the critical level of its current density flowing from the base to the gate region of the thyristor are reached, its conduction process is triggered leading to the establishment of a high-level injection regime in the central region of the device, as illustrated at instant t_6 in Figs. 9(a), (b) and (c). Otherwise, the thyristor remains in its off-state for any instant while keeping the forward reapplied voltage, V_D, across it as shown in Figs. 9 (a'), (b') and (c'). In this case, the hole density distribution and its current density distribution reach their maximum levels at instant t_5. These maximum levels are below the critical levels.

After having diffused along the thyristor epitaxial region, if a sufficient amount of holes arrives at the border of the space charge region extended through the reverse biased gate-base junction (J_2), it will be driven by the electric field extended across this junction into the thyristor P-gate region. Therefore, this necessary amount of holes will automatically replace the threshold amount of holes intended to be applied by the thyristor driven circuit for the triggering of its conduction process.

This necessary amount of holes injected from the base to the gate zone and automatically to the critical hole current density are reached exactly at the instant when $I = I_S$. From this moment, the hole carriers stored in the lightly doped region of the component considerably increase, leading to its high-level injection regime. The forward voltage drop, V_{TM}, and the forward current, I_F, are established through the thyristor.

It could be easily deduced that under the same operating conditions (I_F, V_R, dV_D/dt and T_o) for DUT, during the reapplication of a forward voltage across it, the possibility of triggering is greatly dependent on the remaining amount of holes inside the device base region just at instant t_1. That is why the lapse of time, T_{off}, should be long enough to avoid triggering the DUT by reducing the remaining amount of holes in the N-base region at instant t_1. Hence, the injected holes
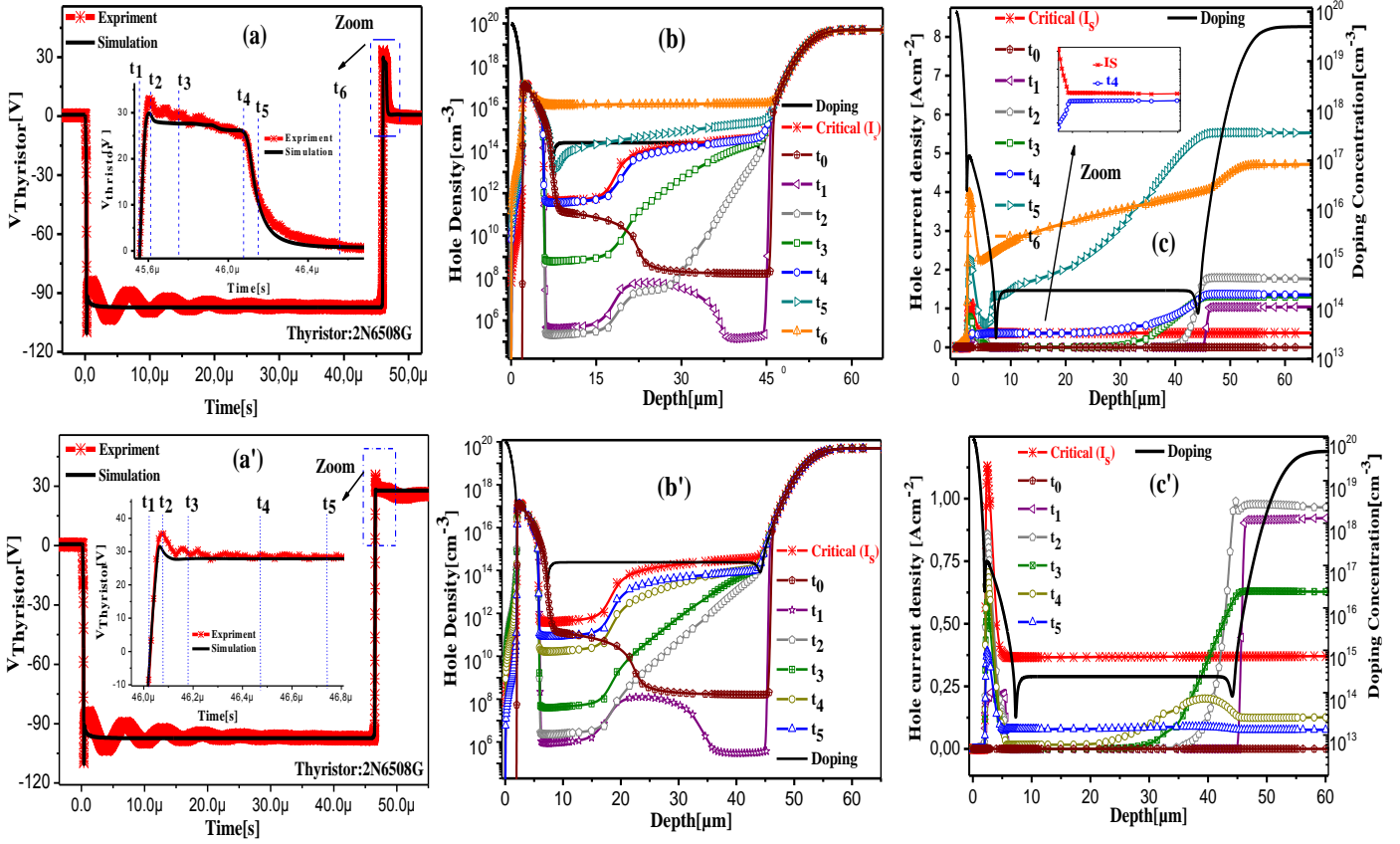
Fig. 9. Behavior of the Thyristor (2N6508G) during the reapplication of a forward voltage across it under (T_o = 27°C, V_R = 100V, dV_D/dt = 980V/μs and I_F = 2A) for two cases: (T_{off} slightly lower than t_q (a, b and c) and (T_{off} = t_q (a', b' and c')). (a, a') Comparison between experimental and simulated voltage waveforms across the Thyristor. (b, b') Hole density distributions for various instants during the reapplication of a forward voltage across the Thyristor. (c, c') Hole current density distributions for various instants during the reapplication of a forward voltage across the Thyristor

through the J_3 junction added to the residual ones in the base region and after diffusing along the component base zone do not reach a critical level and its current density do not reach a critical level for any instant during the reapplication of the forward voltage, as shown in Figs. 9(b') and 9(c'). Consequently, by varying T_{off}, the t_q value could be easily measured (t_q = T_{off}) exactly when the first change is detected from the B to A behavior state of DUT.

The remaining amount of stored holes in the N-base region of the thyristor just at instant t_1 for T_{off} = t_q and T_{off} slightly lower than t_q are shown in Fig. 10.

The t_q of the thyristor depends on the design parameters of the device as well as the parameters related to the component operating conditions imposed by the test circuit [37].

The t_q behavior study of the thyristor versus its design parameters is beyond the scope of this paper. The t_q behavior as a function of the physical quantities such I_F, V_R, dV_D/dt, and T_o, for the DUT are studied and analyzed in detail and discussed in a physical study using simulation results. A comparative study between the experimental and simulated results is performed

B. t_q versus dV_D/dt

A thyristor initially in its off-state, could be turned on without applying a current pulse on its gate when a forward voltage is
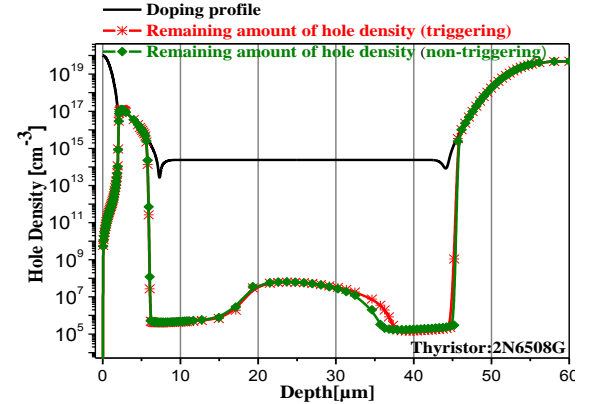

Fig. 10: Hole density distributions at instant t_1, operating under the following conditions (V_R = 100 V, T_o = 27 °C, dV_D/dt = 980 V/μs and I_F= 2 A) for T_{off}= t_q (non-triggering of the Thyristor conduction process) and T_{off} slightly lower than t_q (triggering of the Thyristor conduction process)

applied on its terminals with a ramp rate, dV_D/dt, higher than $(dV_D/dt)_{critical}$ [38]. Indeed, at the reapplication of the forward voltage across the thyristor, the anode-base and cathode-gate junctions become forward biased, while the gate-base junction becomes reverse biased. The triggering of the thyristor conduction process by dV_D/dt is mainly due to the injection of a considerable amount of holes through the anode-base junction J_3 in a short time inside the thyristor base region.
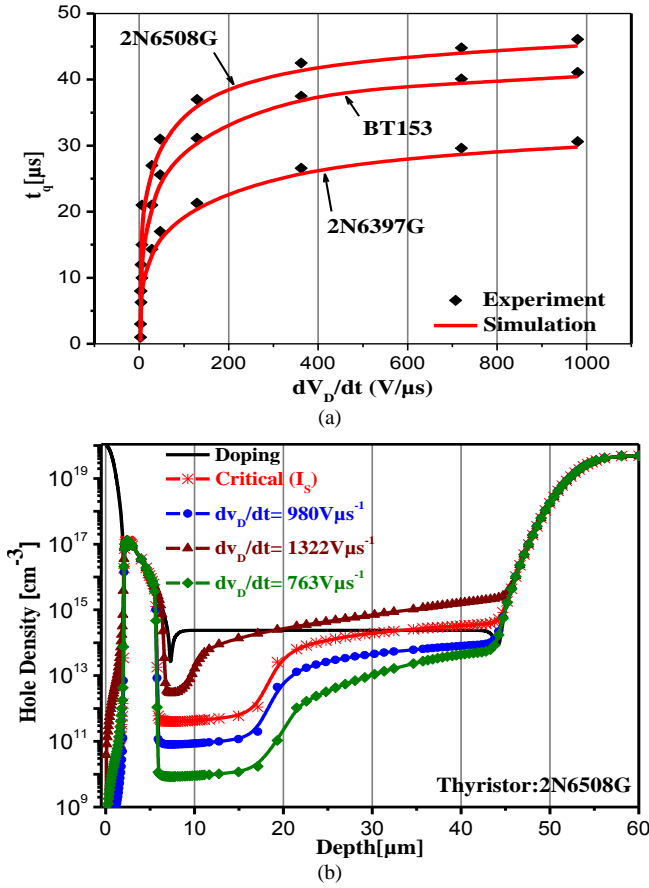
Fig.11. t_q versus dV_D/dt. (a) Experimental and simulated behavior of t_q of DUT as a function of dV_D/dt for (T_o = 27 °C, I_F = 2 A, V_R = 100 V). (b) Hole density distributions at instant t_5 versus dV_D/dt, across DUT (2N6508G) for (T_o = 27 °C, I_F = 2 A, V_R = 100 V and (T_{off} = t_q for dV_D/dt = 980 V/μs))

After diffusing along this lightly doped zone, this considerable amount of holes will be driven by the electric field extended through the gate-base junction J_2 in the P-gate region of the component, replacing the necessary amount of holes that were intended to be injected by the gate driven circuit responsible for the triggering of the regenerative action required for the thyristor conduction process. Therefore, this threshold amount of holes injected through the J_3 junction corresponds to a critical value of dV_D/dt. The effect of the dV_D/dt value (values lower than of the critical) on t_q is selected to be studied in this paper. By varying dV_D/dt under the operating conditions (I_F = 2 A, T_o = 27 °C and V_R = 100 V), the t_q behavior as a function of dV_D/dt for the DUT are measured with the experimental test setup and plotted in Fig. 11(a).

It can be observed that for each thyristor, the t_q value decreases with the reduction of dV_D/dt. It is also clear from this figure that the value of t_q falls considerably at the low values of dV_D/dt. Under the operating conditions (I_F = 2 A, T_o = 27 °C, dV_D/dt = 980 V/μs and V_R = 100 V and T_{off} = t_q), the simulated hole density distribution at instant t_5 for the Thyristor (2N6508G) is given in Fig. 11(b)

The hole density distribution is in its maximum position below the critical level. When dV_D/dt is increased while the same value of T_{off} is maintained, the levels of the hole density and its current density at instant t_5 become higher than those corresponding to the I_S current, leading to the triggering of the

thyristor conduction process. To avoid this change from the A to B behavior state of the component to measure the novel value of t_q, T_{off} should be increased to decrease the remaining amount of holes in the base region of the thyristor at the reapplication of the forward voltage across it. This residual amount reduction of the holes in the lightly doped region of the component will compensate the increase of holes injected in this region through the J_3-junction, due to the increasing of dV_D/dt. This physically explains the growth of t_q versus dV_D/dt in Fig. 11(a).

C. t_q versus I_F, T_o and V_R.

The behaviors of t_q as a function of I_F, T_o, and V_R for the DUT-are plotted in Fig. 12. it can be seen that the t_q parameter is directly proportional to I_F and T_o; however, it is inversely proportional to V_R.

When exactly T_{off} = t_q and for a slight increase of I_F or T_o, the hole density reaches the critical level, during the reapplication of the V_D voltage across the thyristors, triggering the regenerative action required by the conduction process of DUT, leading to a change from the A to B behavior state of thyristor.

As I_F or T_o increase, the hole density and its current density increase above the critical levels, approaching those corresponding to the high-level injection regime. Consequently, the conduction process of DUT will be triggered faster. Since the amount of charges stored in the thyristor base region during its conduction mode is an increasing function of I_F and T_o, the t_q measurement approach of the thyristor should be performed again by gradually increasing T_{off} to reduce the remaining amount of holes in the thyristor base region at instant t_1 to compensate its increase due to the increase of the stored charges during the thyristor conduction mode when I_F or T_o are increased. Thus, the residual holes in the base region added to the holes injected through the anode-base junction J_3 will no longer reach the critical level of hole density and the regenerative action necessary for the forward conduction mode cannot be triggered for T_{off} equal to the new value of t_q. This physically explains why t_q increases with I_F and T_o as illustrated in Figs. 12(a) and 12(b).

This analysis, which highlights the t_q behavior of thyristor as a function of I_F and T_o, is validated by the good agreement obtained between the experimental and simulated results for the DUT as shown in Figs. 12(a) and 12(b). The t_q behavior of thyristors as a function of I_F and T_o should be thus considered for thyristor converters operating at elevated switching frequencies and high temperatures.

When thyristors are turned off, the reverse applied voltage across them is mainly supported by the anode-base junction. An electric field will thus be established through this reverse-biased junction and will be primarily extended on the side of the lightly doped base region. This field will sweep the stored charges that have been injected into the base region of the component during its conduction phase, creating a depletion zone from free charges inside this region. As V_R increases during T_{off}, the charge evacuation process will be performed
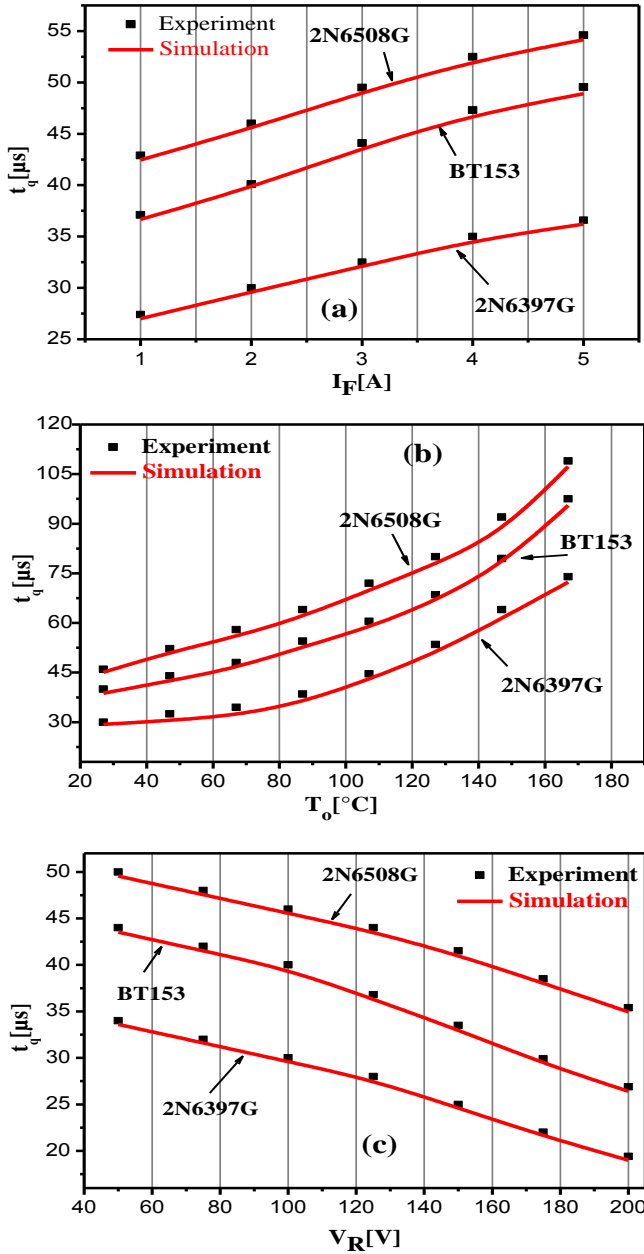
Fig. 13. Hole density distributions at instant t_6 versus V_R, for the Thyristor (2N6508G) under (T_o = 27 °C, I_F = 2 A, dV_D/dt= 980 V/µs and T_{off} slightly lower than t_q for V_R = 100 V)

The B behavior state is no longer valid for the component since its conduction process is no longer triggered. Therefore the measurement procedure should be performed again to measure the new value of t_q when V_R increases. Indeed, the lapse of time T_{off} should be decreased to increase the remaining amount of holes inside the geometrical structure of the thyristor at the reapplication of the forward voltage across it. This will automatically compensate for the reduction of the residual amount of holes due to the increase of V_R. The simulated behaviors of t_q as a function of V_R for the DUT are then compared to those given by the experimental test circuit. A good agreement is obtained between these results as shown in Fig. 12 (c). The physical explanation in this section fit well with the experimental portion. It could be deduced from this section that when the V_R voltage is increased, the thyristor's ability to regain its turn-off capabilities is diminished. This fact must be taken into account in designing of thyristor converters operating at elevated switching frequencies.

V. CONCLUSION

In this paper we have defined a measurement approach of the t_q parameter of thyristors. A test setup has been designed and built to accurately measure the t_q parameter of thyristors. Owing to the experimental circuit specificity, we have studied the t_q behaviors as a function of the electrical and physical quantities imposed by the test setup. All experimental results are analyzed with a high level of accuracy by simulation after having implemented the complete circuit model, including wiring and probe parasitics in the FEM simulator, DESSIS-ISE TCAD.

By using the complete model of the experimental test setup, including the accurate design parameters of three commercial thyristors selected as reference devices, we have analyzed the dependency of the thyristor parameter t_q on the quantities I_F, V_R, dV_D/dt, and T_o using a physics-based FEM model of commercially available thyristors.

The study is useful in developing multi-physics analytical models of Si thyristors often required to predict switching losses. It is thus intended to extend our study to a Si thyristor with higher breakdown voltage (kVs). The approach of the developed measurement procedure is devoted to Si

Fig. 12. t_q of DUT versus I_F, T_o and V_R. (a) Experimental and simulated t_q of DUT versus I_F, for (V_R = 100 V, T_o= 27 °C, dV_D/dt = 980 V/µs). (b) Experimental and simulated t_q of DUT versus T_o, for (V_R = 100 V, I_F = 2 A, dV_D/dt = 980 V/µs). (c) Experimental and simulated t_q of DUT versus V_R, for (T_o = 27 °C, I_F = 2 A, dV_D/dt = 980 V/µs).

faster, and the remaining amount of holes in the device base region at instant t_1 will be decreased.

For T_{off} slightly lower than the t_q of the thyristor (2N6508G) operating under the conditions (I_F = 2 A, T_o = 27 °C, dV_D/dt = 980 V/µs and V_R = 100 V), the hole density distribution corresponding to the high-level injection regime at instant t_6 is simulated in Fig. 13.

Under the same operating conditions but with various values of V_R, the distributions of hole density and its current density at instant t_6 are also selected. It can be observed that at instant t_6 and when V_R is increased from 100 V to 200 V, the hole density considerably falls below the critical level.
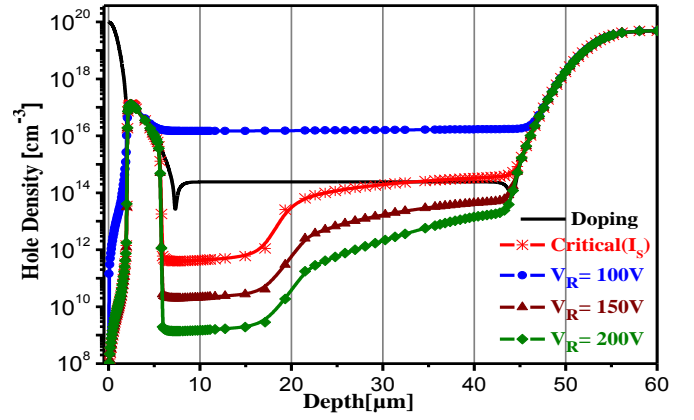
thyristors. Our future research task will be to extend the t_q measurement procedure to Silicon Carbide thyristors.

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