Direct Current Control for Grid Connected Diode-Clamped Inverters

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***Abstract*—The accurate control of the line current, robust and dynamic behavior even under distorted grids and other system faults are the most important requirements for grid connected inverters. Applying direct current control to multilevel inverters combines the advantages of both and is an enabling step towards improved inverter performance. Direct current controllers suffer from high complexity at increased level count, which is resolved using geometrical principles and simple analytical calculations for switching vector selection within the space vector diagram. The simplified, novel parametric controller concept is scalable to inverters with arbitrary level count, does not require any switching tables and the new fully symmetric setup guarantees equal switching frequencies among the three phases. The hypotheses are further confirmed on a real hardware test setup on the example of a 3-level NPC inverter hardware and a Xilinx development platform. Experimental results prove the expected behavior of the direct current control under various conditions, shows a general approach to balance the DC-link capacitors of diode-clamped inverters within the theoretical limits and demonstrates the benefits of using Field Programmable Gate Arrays (FPGA) as a controller platform.**

***Index Terms*—Current control, Field programmable gate arrays, Multilevel systems, Robust control**

I. Introduction

In literature, current control algorithms are divided into two main groups, namely indirect and direct controllers. Indirect methods separate current error compensation from modulation and exploit the advantages of open-loop modulators such as constant switching frequency, well-defined harmonic spectrum, optimal switching patterns and symmetrical DC-link utilization [1]. Direct methods attempt to directly modulate the current signal without calculating the output voltage. The most important advantages of the latter are the high dynamic range even with unknown loads and fast response. However, some of them have drawbacks primarily in steady-state behavior and with variable switching frequencies.

Today's real world applications mostly employ indirect current control techniques for their modulation method. Despite all their advantages, direct current controlled inverters are not the most common choice in industry applications. The advantages and disadvantages of those current control techniques have been widely discussed in the past and are presented in [1]–[3].

Different approaches of direct current control algorithms confirm the main advantages but also show the disadvantages. For example three phase hysteresis current controllers use three independent relays, one for each phase. When the line current exceeds the upper or lower limit of the current hysteresis band, the inverter leg is switched correspondingly to the negative or positive direction to reduce the specific current error. This control method shows excellent dynamic behavior and is capable of operating with asymmetrical loads. The main disadvantage is the considerably higher switching frequency as the relations between the three phases are totally neglected. The α-β hysteresis current controller reflects the dependency between the phases and transforms the three phase system into the α-β system using the Clarke-transformation [4]. This controller uses multi-stage relays to act on α and β errors. Changes to the output voltage of the inverter are triggered using those hysteresis bands. Several researchers have tried to overcome the main disadvantage of unequal switching frequencies among the three phases [5]. Predictive current control schemes calculate the estimated current trajectory [6]. Knowing the system parameters, the time until the tolerance band is touched can be calculated easily. This information could be used to lower the switching frequency of the inverter, by choosing the inverter output state which keeps the current error within the tolerance band for the longest time possible. By varying the tolerance band any average switching frequency can be set. The quality of this control method heavily depends on the accuracy of the load model parameters. Several researchers are proposing promising concepts classified in [7].

The research on multilevel inverters is growing rapidly since the so called neutral point clamped (NPC) inverter was introduced in 1981 [8]. After this development several multilevel inverter topologies were introduced all implementing the basic principle of multilevel converters to take the advantages of this topology. The main advantages compared to standard two-level inverters are presented in [9]–[11]:

- a more sinusoidal output waveform

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- a higher voltage capability
- lower switching losses

The main idea behind multilevel topologies is applying only small fractions of the DC voltage step-by-step to the load. The level count n of an inverter directly describes the total number of voltage steps available.

Space-vector based (SVM) modulation techniques are most commonly used for multilevel inverter applications [12]–[14]. A main drawback is the high complexity with an increasing number of voltage levels. An alternative and promising space vector based direct current control algorithm for two-level inverters can be adapted to three- or higher-level systems [15]. It controls the current by using four space vector voltages around the reference voltage v_{ref}. However, it also shows an increased complexity with high level numbers. Different approaches attempting to reduce the complexity of space vector based control are presented in [13], [16]–[18].

SVM algorithms are commonly implemented on digital signal processors (DSPs). Owing to the functional principle of those platforms, the control algorithm is processed sequentially which leads to longer calculation times. This behavior limits their usefulness with complex control algorithms and very fast direct current controllers. A new alternative to implementing control algorithms on DSPs is the use of field programmable gate arrays (FPGA), offering very fast calculation times and parallel computing capabilities [19].

This paper introduces a new FPGA based direct current control algorithm for grid connected inverters. Based on a three phase transformation [20], which is ideally suited for fixed point arithmetic, the algorithm controls the current quasi-continuously. A generic approach enables easy adaption to higher-level systems. The main advantages of the proposed concept are the geometric structure of the controller which achieves equality of the phase switching frequencies, the generic approach which gives the opportunity to freely decide the level count of the inverter and the optimization for fixed point arithmetic to run on an FPGA. Experimental results using a state-of-the-art three-level inverter and a real-time FPGA board prove the concept.

II. Basic principles

The proposed concept is verified using neutral point clamped inverters and a three phase transformation which is ideally suited for FPGA implementations.

A. Neutral point clamped inverter

A three-level NPC inverter is shown in Fig. 1. Compared to a standard two-level inverter, which provides $\pm\frac{V_{\mathrm{DC}}}{2}$ as output levels, the NPC inverter selects its output voltage amongst $\pm\frac{V_{\mathrm{DC}}}{2}$ and 0. Each leg of a three-level NPC inverter consists of four transistors and two clamping diodes. The functional principle works like all conventional inverters except that the two middle transistors and the clamping diodes offer the possibility to clamp the neutral point to the phase output. Diode clamped inverters also exist for higher level counts and are presented in [21], [22]. In general it can be said that an diode-clamped based three phase n-level inverter consists of

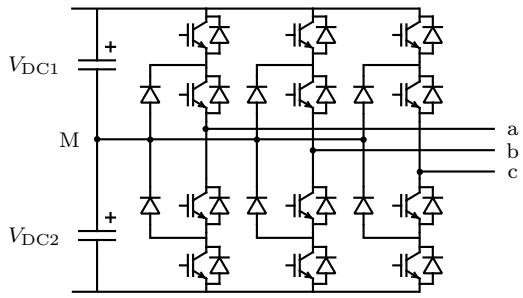

Fig. 1. Schematic of a three-level NPC inverter

$3\cdot 2\cdot(n-1)$ switches and $n-1$ DC capacitors charged with an equal fraction of the DC-link voltage. The number of required diodes can be calculated as $3\cdot(n-1)(n-2)$. A drawback of diode-clamped inverter is a possible unbalance between the DC-link capacitors. Several researchers propose promising schemes to overcome this disadvantage in [23], [24].

B. Transformation

The control algorithm is based on a special three phase transformation ideally suited for FPGA implementation to locate the sector of the reference voltage vector in the space vector plane [20]. The three phase voltages are described in a non-orthogonal a_*b_*-coordinate system which enables fast fixed point calculations as only integer values are used to describe the states. The transformation, as derived in [20], is given by

$$\underline{v}_{*\mathrm{ref}} = \underline{v}_{\mathrm{ref}}\{a_*, b_*\} = T\cdot\underline{v}_{\mathrm{ref}}\{a,b,c\}, \tag{1}$$

with the transformation matrix

$$T = \frac{2}{3}\begin{pmatrix} 1 & 0 & -1 \\ 0 & 1 & -1 \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix}. \tag{2}$$

Using this transformation matrix, the determination of the sector for control and the redundant states is achieved by the following three steps derived in [20]:

1) Determine adjacent voltage vectors: To select those four space vectors which are located closest to the reference voltage the following steps are performed (Fig. 2):

- Transform and normalize the reference voltage into the a_*b_* system using the above transformation.
- Determine the base vector of the translated unit cell by using the floor function

$$\underline{V}_{*\mathrm{base}} = \lfloor\underline{v}_{\mathrm{ref}}\{a_*, b_*\}\rfloor. \tag{3}$$

- Calculate the three remaining space vectors of the unit cell by simply adding a unit step along either the a_*-, b_*-or both axes.

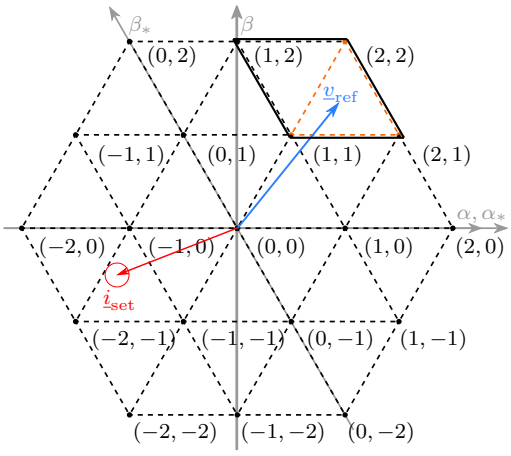

Fig. 2. Space vector diagram of a three-level inverter with (a_*, b_*) coordinates, unit cell and voltage triangle for control / set current with circular tolerance area

2) Determine the triangle for control: Since only three space vectors should be sufficient to modulate a reference voltage, one of the four surrounding space vectors of the unit cell can be eliminated. As the unit cell can be split into two triangles the one containing the reference voltage vector shall be selected. This triangle can simply be determined by calculating the dot product:

$$(\underline{v}_{*\mathrm{ref}} - \underline{V}_{*\mathrm{base}}) \cdot \begin{pmatrix} 1 \\ -1 \end{pmatrix} \geq 0 \quad \Rightarrow \quad \text{right triangle} \tag{4}$$

$$(\underline{v}_{*\mathrm{ref}} - \underline{V}_{*\mathrm{base}}) \cdot \begin{pmatrix} 1 \\ -1 \end{pmatrix} \leq 0 \quad \Rightarrow \quad \text{left triangle} \tag{5}$$

3) Determine redundant states: Depending on the multi-level inverter topology, the DC-link voltages may need to be balanced. One possible option would be taking advantage of redundant switching states. For a three-level system, $[1\ 0\ 0]$ produces the same inverter output voltage as $[0\ -1\ -1]$.

It is obvious that the redundant states can simply be determined by adding or subtracting $[1\ 1\ 1]$. This enables fast processing and easy calculation with fixed point systems. This is another advantage of the three phase transformation referenced above.

III. Proposed Direct Current Control Algorithm

The idea behind a current controlled inverter is keeping the current-error within a specified tolerance band respectively within a tolerance area in the a_*b_*-plane or in the well known $\alpha\beta$-plane. This tolerance area moves with the reference current and is located around the top of the reference current vector $\underline{i}_{\mathrm{ref}}$. Each time the current leaves the tolerance area a new space vector is selected corresponding to a voltage which reduces the current error.

A. Selection of current error reducing vector

Fig. 2 shows the space vector diagram of a three-level inverter with a reference voltage vector pointing to a specific triangle.

To control the reference current a circular tolerance area is chosen to trigger a switching event. When the current leaves the tolerance area the one inverter voltage vector leading the current error vector back towards zero is chosen. Knowing the magnitude and the phase of all involved vectors the correct inverter output voltage can simply be selected. Fig. 3 shows the geometric representation of the described problem with v_{ref} and its three neighboring space vectors. The origin of the coordinate system is defined to be at the top of the reference voltage $\underline{v}_{\mathrm{ref}}$.

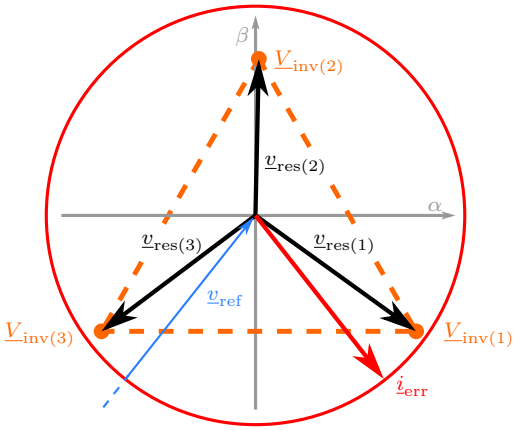

Fig. 3. Geometrical representation of all voltage and current vectors needed for current control

Using (6) the resulting voltages $\underline{v}_{\mathrm{res(k)}}$ can be determined. $\underline{v}_{\mathrm{res(k)}}$ is the voltage which directly impacts the current.

$$\underline{v}_{\mathrm{res(k)}} = \underline{V}_{\mathrm{inv(k)}} - \underline{v}_{\mathrm{ref}} = V_{\mathrm{res},k} e^{j\varphi_k}, k = 1, 2, 3 \tag{6}$$

where the magnitude V_{res} determines the rate of change of the current vector and φ the direction.

It is appropriate to plot the current error in Fig. 3 as well. The current error $\underline{i}_{\mathrm{err}}$ is defined by

$$\underline{i}_{\mathrm{err}} = \underline{i}_{\mathrm{set}} - \underline{i}_{\mathrm{ref}} = I_{\mathrm{err}} e^{j\psi}. \tag{7}$$

Calculating the complex dot product of the three voltages with the current error and choosing the minimum of those the controller selects the one output voltage that produces the component best opposing the current error. This can be achieved by finding the minimum out of the three dot products:

$$\min_k \Re \left\{ \underline{v}_{\mathrm{res(k)}} \cdot \bar{\underline{i}}_{\mathrm{err}} \right\} \tag{8}$$

The real component of (8) represents the dot product. It is minimal if the angle $\varphi_k - \psi$ is $180°$. Thus the minimum of the dot product yields directly to the one output voltage best opposing the current error.

B. DC-link balancing

Using the diode-clamped inverter topology with the DC-link mid point connected, an imbalance of the DC-link capacitor voltages can occur due to the choice of switching vectors. Since multiple switching vectors can produce the same output

voltage but with complementary effects on the DC-link capacitor voltage, a DC-link balancing algorithm can be applied. A balancing strategy which is also based on the minimum stored energy of the capacitors for a back-to-back five-level HVDC converter system was proposed in [25].

To demonstrate the easy adaptability to higher level converters an algorithm for an n-level diode-clamped inverter with $n-1$ DC-link capacitors will be derived. Fig. 4 shows the graphical illustration of the nomenclature used for the derivation of the DC-link balancing of n-level NPC inverters.

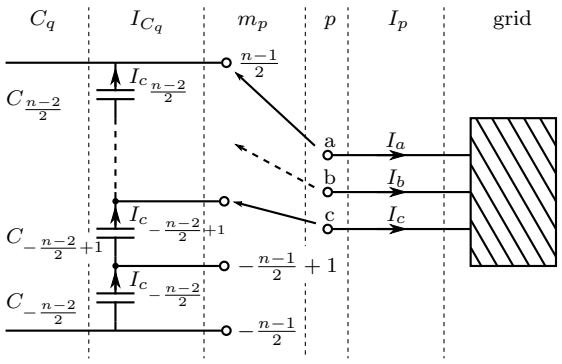

Fig. 4. Graphical illustration of the nomenclature of an n-level NPC inverter

We label the mth nominal output voltage on phase p as $V_{p,m}$:

$$V_{p,m} = \frac{mV_{\mathrm{dc}}}{n-1}, \tag{9}$$

where

$$\left\{ m \in \mathbb{Z} + \frac{n-1}{2} \middle| -\frac{n-1}{2} \le m \le \frac{n-1}{2} \right\}. \tag{10}$$

The current is defined as I_p (positive current flowing out of the inverter) on phase p.

Capacitors are labeled C_q where

$$\left\{ q \in \mathbb{Z} + \frac{n}{2} \middle| -\frac{n-2}{2} \le q \le \frac{n-2}{2} \right\}. \tag{11}$$

When the output is V_m, there are $\frac{n-1}{2} - m$ capacitors in series to the upper rail and $m - \frac{n-1}{2}$ capacitors in series to the lower rail.

Capacitor C_q supplies a current

$$\begin{aligned} I_{C,q} &= \sum_p I_p \begin{cases} \frac{1}{2} - \frac{m_p}{n-1} & \text{for } q < m_p \\ -\frac{1}{2} - \frac{m_p}{n-1} & \text{for } q > m_p \end{cases} && (12) \\ &= \sum_p I_p \left(\frac{1}{2} \operatorname{sgn}(m_p - q) - \frac{m_p}{n-1} \right) && (13) \end{aligned}$$

The DC voltage V_{dc} is split over the capacitors. Each capacitor carries a voltage $V_{C,q}$ such that $V_{\mathrm{dc}} = \sum_q V_{C,q}$. The variance of all the capacitor voltages is

$$\begin{aligned} \sigma^2(V_C) &= \frac{1}{n-1} \sum_q \left(V_{C,q} - \frac{V_{\mathrm{dc}}}{n-1} \right)^2 && (14) \\ &= \frac{1}{n-1} \sum_q V_{C,q}^2 - \left(\frac{V_{\mathrm{dc}}}{n-1} \right)^2. && (15) \end{aligned}$$

As the second term is constant, minimizing the variance is equivalent to minimizing the total stored energy in all capacitors

$$E_C = \frac{C}{2} \sum_q V_{C,q}^2. \tag{16}$$

The change of energy is given by

$$\frac{d}{dt} E_C = -\sum_q V_{C,q} I_{C,q}. \tag{17}$$

For a controller with bounded DC capacitor voltages, we require no change in energy on average over time

$$\langle \frac{d}{dt} E_C \rangle \le 0. \tag{18}$$

We therefore want to minimize $\frac{d}{dt} E_C$ at every timestep.

Combining (13) and (17)

$$\begin{aligned} \frac{d}{dt} E_C &= -\sum_{p,q} V_{C,q} I_p \left(\frac{1}{2} \operatorname{sgn}(m_p - q) - \frac{m_p}{n-1} \right) && (19) \\ &= -\frac{1}{2} \sum_{p,q} V_{C,q} I_p \operatorname{sgn}(m_p - q) + V_{\mathrm{dc}} \sum_p I_p \frac{m_p}{n-1}. && (20) \end{aligned}$$

In a system with disconnected neutral, the total current is zero, i.e. $\sum_p I_p = 0$.

As the capacitors are approximately balanced, we define

$$V_{C,q} = \frac{V_{\mathrm{dc}}}{n-1} + \Delta V_{C,q}. \tag{21}$$

Then

$$\begin{aligned} \frac{d}{dt} E_C =& \frac{V_{\mathrm{dc}}}{n-1} \left(-\frac{1}{2} \sum_{p,q} I_p \operatorname{sgn}(m_p - q) + \sum_p I_p m_p \right) \\ & - \frac{1}{2} \sum_{p,q} \Delta V_{C,q} I_p \operatorname{sgn}(m_p - q) && (22) \\ =& -\frac{1}{2} \sum_{p,q} \Delta V_{C,q} I_p \operatorname{sgn}(m_p - q). && (23) \end{aligned}$$

A simple algorithm to drive the capacitors towards the balanced state is therefore to calculate Expression (23) for each switching state that produces the output voltage selected by the current controller and to choose the inverter command that maximizes the rate of decrease of the asymmetry.

From [26], [27] it is known that DC-link balancing works well below a modulation index of $m \approx 0.55$. Above this point it depends on various conditions such as the AC-side power factor or the modulation scheme.

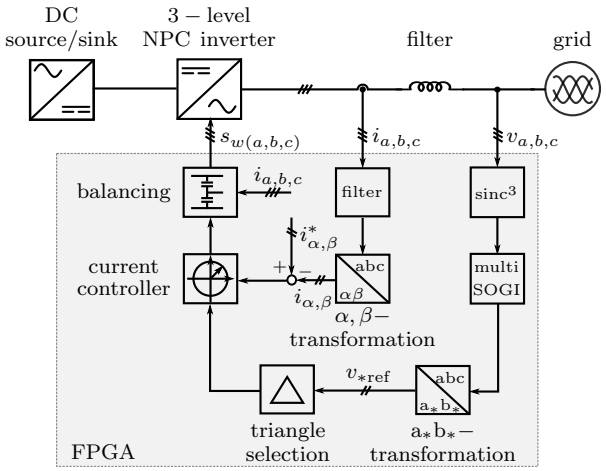

Fig. 5. Proposed control system

IV. Experimental results

Fig. 5 shows a configuration of the proposed system. A three-level NPC inverter is used to test the control algorithm under real conditions. The three phase voltages are measured, filtered, synchronized and transformed to the a_*b_* coordinate system to easily determine the space vectors for control using fixed point arithmetic on an FPGA. To filter the measurement and synchronize with the grid a sinc^3 filter in combination with the so called mSOGI was used [28], [29]. The three phase currents are transformed to the α-β coordinate system. These data are fed to the controller core and are used to determine the switching signals for the three-level inverter. The controller core consists of the current controller and the DC-link balancing algorithm. The output of the current controller gives the inverter voltage best opposing the current error according to (8). Given the commanded voltage, the DC-link balancing algorithm determines the switching signal that minimizes the deviation of the capacitors, if possible. If no redundant switching vector decreasing the deviation exists, the output of the current controller is directly passed through as the inverter switching state.

Fig. 6 shows the real test bench in our lab. The main components are labeled and described below.

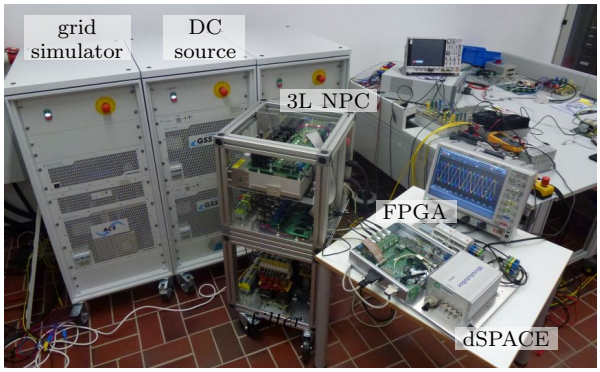

Fig. 6. Test bench for the proposed system

Experiments were carried out to verify the direct current control algorithm and the DC-link balancing algorithm. Fig. 7 shows the three phase current under normal conditions within the German grid. As the hysteresis band is relatively large the current ripple is considerable. The THD_i was calculated using (24) up to the 40^{th} order.

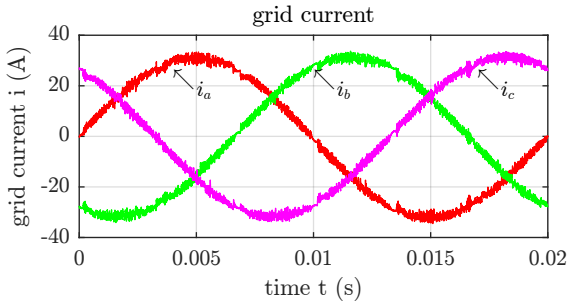

Fig. 7. Measured sinusoidal grid current ($\mathrm{THD}_i = 2.32\%$, $V_{\mathrm{AC}} = 400$ V, $V_{\mathrm{DC}} = 600$ V)

$$\mathrm{THD}_i = \frac{\sqrt{\sum_{h=2}^{40} I_h^2}}{I_1} \tag{24}$$

The main parameters for this measurements were 400 V AC and 600 V DC voltage with a filter inductance of 0.9 mH. The current set point was chosen to be 32 A in magnitude and the radius of the circular tolerance area was set to $|\vec{i}_{\mathrm{err}}|^2 = 1\ \mathrm{A}^2$ in order to achieve an average switching frequency of $f_s = 5\ \mathrm{kHz} \pm 300\ \mathrm{Hz}$. The controller is implemented on a high performance FPGA board with fast data processing ability and inputs for current ($\pm$300 A with 40 MHz) and voltage measurement ($\pm$900 V with 10 MHz). The inverter was a SEMIKRON three-phase NPC inverter with a maximum current capability of 100 A. The main system parameters are summarized in Table I.

TABLE I
Main system parameters

Paramter	Value
Grid voltage	400 V(50 Hz)
Filter inductance	0.9 mH
Rated current	100 $\mathrm{A_{rms}}$
DC-link voltage	600 V
DC-link capacitance	2 mF
Set current $\vec{i}_{\mathrm{set}}$	32 A
Tolerance $|\vec{i}_{\mathrm{err}}|^2$	1 A
resulting active power	$\approx$ 22 kW

A. DC-link balancing

Fig. 8 shows the DC-link voltage of the upper and the lower DC-link capacitor. For demonstration purposes, we added an offset to the upper capacitor measurement to force a 15 V difference between the two voltages. At the time $t = 0.02$ s we set the offset to zero to achieve balanced DC-link capacitor voltages. After 20 ms a balanced state is reached and the overall deviation decreases to a maximum amplitude

of $V_{\mathrm{dc1}} - V_{\mathrm{dc2}} \approx 3$ V. This shows that the direct current control algorithm can be combined with an effective DC-link balancing algorithm.

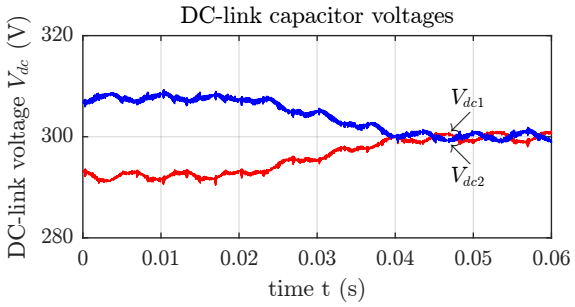

Fig. 8. Measured DC-link capacitor voltages (DC-link capacitance 2 mF)

B. Switching frequencies

Fig. 9 shows the switching frequencies of the phases under varied modulation index. The variation of the switching frequency over modulation index is caused by the functional principle of the direct current controller. As the voltage across the inductance and thus the slope of the current directly depend on the modulation index, the minimum switching frequencies are located at points where the output voltage of the inverter is close to a reference voltage.

It is known that α-β hysteresis controllers exhibit the disadvantage of unequal switching frequencies differing among the three phases by about 20% to 30%. From Fig. 9 it can be seen that the switching frequencies in the three phases do not differ from each other. This is achieved by building up the control scheme in a 3-fold rotationally symmetric system. In fact, the proposed control system maintains 6-fold rotational symmetry, of which 3-fold rotational symmetry is a subset. This measurement has proven that a circular tolerance band for the current error as well as switching vectors located around the reference voltage in a equilateral triangle lead to symmetric switching frequencies within the three phases.

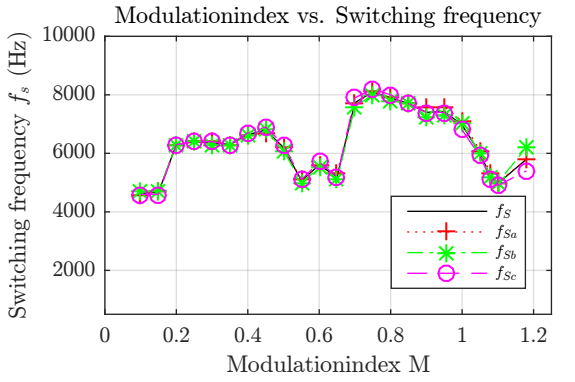

Fig. 9. Switching frequencies versus modulation index

C. Dynamic behaviour

Direct current controllers promise very good dynamic behavior even under load impedance variations. Fig. 10 shows the measured current error upon a current step. At $t = 0$ s the set current was changed from 16 A to -16 A resulting in an inversion of the power flow. It can be seen that the steady state is reached after 0.5 ms without any oscillations typically known from standard PI based indirect current controllers followed by PWM modulator.

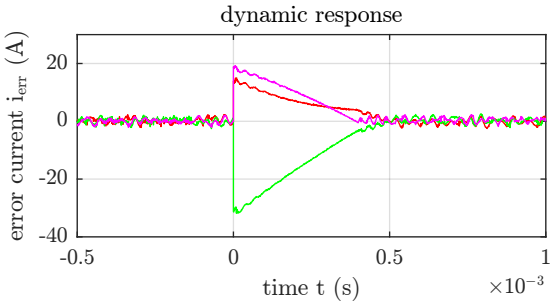

Fig. 10. Measured current error for step-change in set current ($\vec{i}_{\mathrm{set}} = 16\ A \rightarrow -16\ A$)

D. FPGA based control

FPGA based control promises a lot of benefits compared to standard implementations on DSPs as was explained in the introduction. Fig. 11 shows the timing diagram of the control scheme and the relevant components. When a trigger event occurs five tasks need to be carried out. Within the measurements a system clock of 40 MHz was used resulting in a step time of 25 ns. The step time leads to a total calculation time of 1700 ns which supports the statement that the limiting factor within the proposed system is the dead time of the inverter (2.6 μs). Increasing the complexity of the control system and the level count of the inverter would not cause a significant delay as the parallelization to perform the calculation could be used more extensively and the system clock can be scaled up to 300 MHz.

Regarding the computational resources for level counts above 3 the arithmetic effort of the direct current control part remains constant for any level count - only 3 hardware multipliers are needed for $n \rightarrow \infty$. For diode-clamped multilevel inverters the DC-link balancing consumes computational resources depending on the number of capacitors. The number of operations increase proportional to n, however these calculations can be performed in parallel. The FPGA architecture provides flexible possibilities and enough computational resources to handle the proposed algorithms within real-time.

E. Comparison with direct and indirect methods

In literature, several direct and indirect current controllers have been investigated, all having individual advantages and drawbacks. It is difficult to develop and implement a controller serving all demands in terms of complexity, dynamic speed, variation of switching frequency, stability and the application to multilevel systems. Table II compares existing direct and indirect current controllers in a qualitative manner.

To choose the optimal controller for a specific application, additional properties must be taken into account. For operation

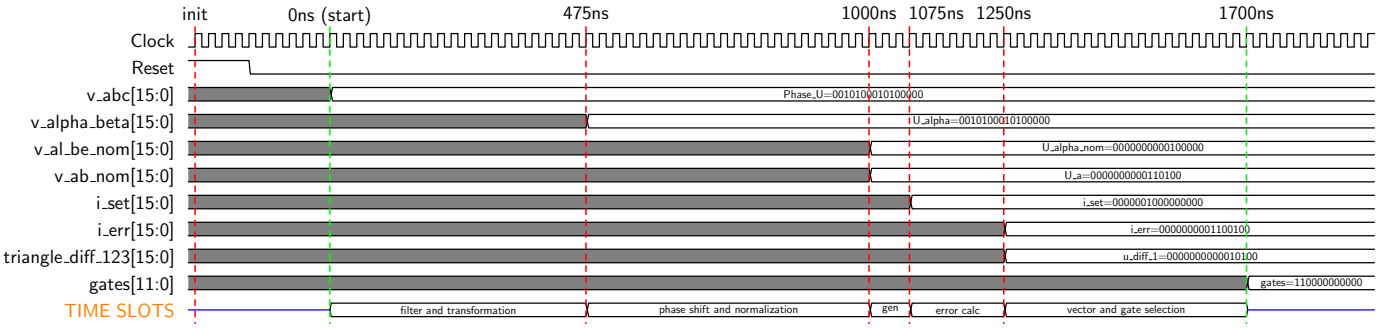

Fig. 11. Timing diagram of controller calculation cycle

TABLE II
COMPARISON OF DIRECT AND INDIRECT CURRENT CONTROLLERS

	PWM	Predictive Control	Direct Power Control	Proposed Current control
Complexity	medium	complex	simple	simple
Dynamic speed	slow	fast	very fast	very fast
Switching frequency	constant	constant	spread	spread
Stability	dependent	dependent	robust	robust
Multilevel adaptability	complex	complex	complex	less complex

in grid connected systems, robust controller types like the Direct Power control or the proposed current control do not need any PI current controller, and thus the reactive and active power can be directly controlled. The controllers' stability is stated as robust for variations within the grid/load impedance. With regard to multilevel systems the effort for adaption to the increased level count needs to be evaluated.

The complexity of adapting control methods to multilevel systems increases with the level count. Due to the low arithmetic complexity of the proposed current control the adaptability is judged to be less complex than existing solutions.

Individual characteristics like the fact that the proposed current controller involves multiplications to choose the correct space-vector, whereas existing direct methods mostly use table-based approaches, can be seen as advantage or disadvantage regarding to the requirements and circumstances within the application.

V. CONCLUSION

This paper presents a new direct current control algorithm. Compared to state of the art direct current control algorithms we have demonstrated some promising results in terms of controllability and complexity:

- The vector selection chooses the vector best opposing the current error.
- The algorithm is optimized for fixed point arithmetic and for easy implementation on FPGAs.
- Very short calculation times allow real-time operation ($t_{\mathrm{calc}} \leq t_{\mathrm{deadtime}}$).
- It is proved that we can overcome the disadvantage of asymmetric mean switching frequencies of the three phases by choosing a rotationally symmetric system (circular tolerance area, triangle for control).
- For adaption to multilevel systems the algorithm is optimized to easily change the inverter level count.
- There is no need to setup switching tables for all sectors within the space vector diagram.

Notwithstanding these advantages the proposed controller concept comes with some drawbacks:

- To choose the correct space-vector within a triangle the algorithm needs to determine the dot product. This involves multiplications whereas existing direct methods mostly use table-based approaches.
- In a diode-clamped topology the capacitor imbalance problem occurs. As described, the direct current controller or the hardware setup needs adaption to overcome this disadvantage.

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