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Principle and Control Design of Active Ground-Fault Arc Suppression Device for Full Compensation of Ground Current

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***Abstract*—Traditional ground-fault arc suppression devices mainly deal with capacitive component of ground current and have weak effect on the active and harmonic ones, which limits the arc suppression performance. The capacitive current detection needed in them suffers from low accuracy and robustness. The commonly-used large-capacity reactive component may bring about overvoltage because of possible resonance with the distributed phase-to-ground capacitance. To solve these problems, an active ground-fault arc suppression device is presented. It employs a topology based on single-phase inverter to inject current into the neutral without any large-capacity reactors, and thus avoids the aforementioned overvoltage. It compensates all the active, reactive and harmonic components of the ground current to reliably extinguish the ground-fault arcs. A dual-loop voltage control method is proposed to realize arc suppression without capacitive current detection. Its time-based feature also brings the benefit of fast response on ground-fault arc suppression. The principle of full current compensation is analyzed, together with the controller design method of the proposed device. Experiment on a prototype was carried out to validate the effectiveness of the device.**

***Index Terms*—Ground fault, arc suppression, full current compensation, voltage control.**

I. INTRODUCTION

POWER supply reliability is of great importance in distribution power systems [1]. Most of the reliability problems originate from single-phase-to-ground faults. The expansion of distribution networks enlarges the ground-fault current, which results to arc striking and consequently power supply apparatus outage. This makes the performance of arc suppression device (ASD) critical to the power system.

Traditional arc suppression coil (ASC) compensates the capacitive ground current by the principle of parallel resonance [2][3], encountering limited arc suppression performance as large harmonic contents can also maintain arcs at the ground point [4]. Besides, the possible overvoltage caused by the series resonance between ASC and inherent capacitance at the inception of ground fault may further result in cross-country faults and insulation failure [5]-[8]. Therefore, the ability of full ground-current compensation and dynamically adjusting the ASC inductance is emphasized in practice.

Several methods have been presented to avoid overvoltage and achieve dynamic adjustment of ASC inductance. *X. Zeng* [9] has presented a grounding method using a pre-adjusted Petersen coil paralleling with a reactor, which disconnects the coil in normal condition and connects it to the neutral at ground fault, to avoid overvoltage and extinguish fault arcs. This method avoids series resonance to some extent, but lacks of flexibility to the change of distributed parameters. *B. Chen* [10] has proposed two-stage magnetically controlled reactor to enhance the dynamic performance and mitigate the 3rd order harmonics caused by nonlinearity of saturated iron core. *C. Wang* [11] has proposed a three-phase five-column Peterson coil which is able to automatically trace the capacitive ground current with reduced harmonic injection. These devices are suitable to use in high voltage power systems. However, both of them are not able to compensate the active and harmonic components in ground current, thus have limited arc suppression performance.

The harmonics in ground current are mainly caused by the nonlinearity of the power transformers, mutual inductor, and nonlinear loads. Typical harmonic orders are 3rd (from transformers), 5th and 7th (from nonlinear loads e.g. rectifiers) [12][13]. The harmonic component of residual current may be several times greater than the fundamental one [4], resulting in unsatisfactory arc suppression performance while using the aforementioned methods. The active component in ground current is always neglected as its magnitude is relatively small (less than 5% of capacitive current) in normal condition, however, it may exceed 10% p.u. in overhead-line networks

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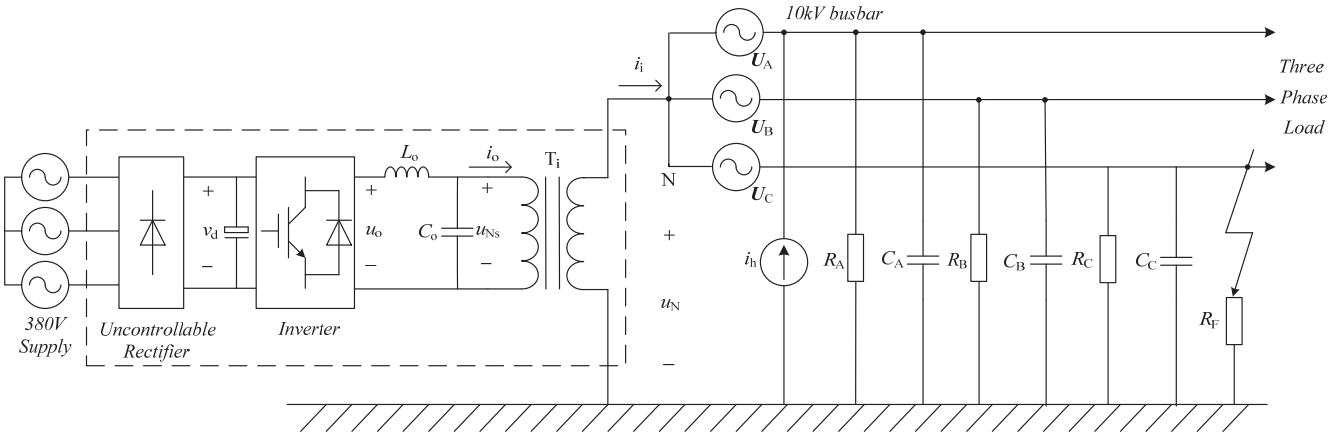

Fig. 1. Topology of the distribution network with the proposed arc suppression device.

due to insulation aging, bad weather or environmental deterioration. This current certainly enlarges the arc ignition duration and may even cause arc-extinguishing failure. Therefore, full compensation of ground current is essential to reliably quench ground-fault arcs.

Several active ways based on the technology of power electronics are proposed to meet this requirement. *K. Winter* [14] [15] has proposed a residual current compensation ground fault neutralizer (RCC-GFN) which is able to compensate harmonic ground current up to the 7th order. However, the response time (3 cycles) of this device is too long from the view of contemporary technology due to the adoption of gate-turn-off thyristor (GTO) based inverter with switching frequency of only 1.2 kHz. Moreover, the device is not designed to compensate the active component of ground current. *Y. Yang* [16] has proposed a principal-auxiliary ASC which is able to compensate the full ground current with the use of voltage source inverter connected to the auxiliary coil in parallel. This method has the advantages of full ground-current compensation and reasonable cost, but as it contains ASC in the principal side, series resonance may still happen and there is no measure mentioned to avoid it. *Q. Chen* [17] has proposed an ASC based on transformer with controlled load, which has the ability of full ground-current compensation and rapid response. However, this device suffers from low accuracy of the capacitive current detection and thus has limited arc-extinguishing performance.

All the aforementioned methods face the same problem, i.e., the capacitive current of the distribution network which is necessary for them is complicated to be precisely detected, owing to the complexity of operation modes [18][19]. *X. Lin* [20] has presented an online distributed capacitance measurement via twice measuring the voltage and current of ASC. This method can achieve real-time detection of capacitive current, however, the detection time undermines the overall performance of arc suppression. A harmonic current injection method is proposed by *X. Zeng* [21] to realize fast detection of capacitive current. However, the continuously injected harmonics for real-time measurement may deteriorate the power quality of the distribution system. Moreover, the detection of active and harmonic current are not mentioned in these methods, making them unfeasible for full ground-current compensation.

Recently, a hybrid flexible grounding system is proposed by *B. Chen* [22], which combines the magnetic control reactor (MCR) providing large-capacity reactive power and the active power compensator (APC) realizing full ground current compensation. Besides, the voltage control method used in this device does not need capacitive current detection, which decreases the response time and residual current level. However, the aforementioned series-resonance problem remains due to the use of MCR. Moreover, the control method adopts Fast Fourier Transformation (FFT) to calculate the magnitude of control parameters for real-time control. It significantly undermines the dynamic performance, making the system unsuitable for fast arc suppression.

This paper presents an active arc fault suppression device (ASD) which is able to achieve full ground-current compensation without the detection of capacitive current. The rest of this paper is organized as follows. In Section II, the principle of full ground-current compensation is presented. The voltage control and implementation method of active arc suppression is proposed in Section III, followed by control performance analysis and simple design guidelines of the controller parameters. Finally, experimental results are presented to verify the effectiveness of the ASD.

I. Full Ground Current Compensation Principle

A typical 10 kV distribution network with one feeder line and the proposed arc suppression device is shown in Fig. 1. U_X (X = A, B, or C) is the three-phase line-to-neutral voltage. R_X and C_X are the phase-to-ground leakage resistance and capacitance, respectively. The single-phase-to-ground fault is assumed to happen in phase C with a ground-fault resistance of R_F. The zero-sequence harmonic source is simplified to i_h in phase A. The proposed ASD connecting between the neutral and the earth is shown in the dashed box. It consists of a three-phase uncontrollable rectifier, a single-phase inverter with LC filter and an isolation transformer T_i. The rectifier and inverter are connected in parallel with a dc capacitor.

To simplify the analysis, the ASD is substituted for a controlled current source with the current of $\boldsymbol{I}_i$. It is assumed that the distributed phase-to-ground parameters are balanced, and the phase-to-ground resistance, capacitance and impedance are denoted by R_S, C_S and Z_S, respectively. It is also assumed that line-to-neutral voltages U_X are sinusoidal in fundamental frequency. The ground current, faulty phase voltage, neutral-to-ground voltage are $\boldsymbol{I}_F$, $\boldsymbol{U}_F$ and $\boldsymbol{U}_N$, respectively. Thus,

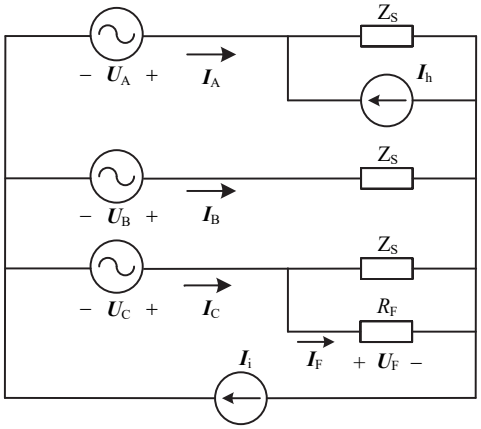

Fig. 2. Simplified system circuit.

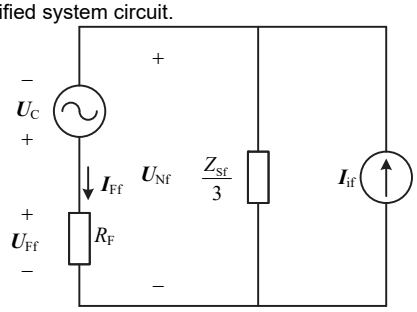

Fig. 3. System circuit in fundamental domain.

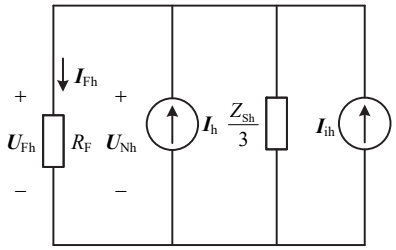

Fig. 4. System circuit in harmonic domain.

the simplified circuit of the system can be obtained in Fig. 2.

The system circuit is decomposed in fundamental and harmonic domain as shown in Fig. 3 and Fig. 4, respectively. The fundamental and harmonic components of the parameters in these figures are marked with the subscripts of '$_f$' and '$_h$', respectively. Thus, the fundamental and harmonic components of $\boldsymbol{I}_i$ can be expressed by

$$\boldsymbol{I}_{if} = \frac{3\boldsymbol{U}_{Nf}}{Z_{Sf}} + \boldsymbol{I}_{Ff} \tag{1}$$

$$\boldsymbol{I}_{ih} = \boldsymbol{I}_{Fh}\left(\frac{3R_F}{Z_{Sh}} + 1\right) - \boldsymbol{I}_h . \tag{2}$$

It should be noticed that the neutral-to-ground voltage and faulty phase voltage are equivalent in harmonic domain. The expression of $\boldsymbol{I}_i$ for compensating the ground current to zero can be obtained via setting $\boldsymbol{I}_F$ to zero and is shown as

$$\boldsymbol{I}_i = \frac{3\boldsymbol{U}_{Nf}}{Z_{Sf}} - \boldsymbol{I}_h = 3\boldsymbol{U}_{Nf}\left(\frac{1}{R_S} + j\omega C_S\right) - \boldsymbol{I}_h . \tag{3}$$

The current for full ground-current compensation is defined as the current injected to neutral which ensures the ground current to be zero under the conditions of ground impedance variation and zero-sequence harmonics existence. It consists of the active, reactive and harmonic component of the zero-sequence ground current. By substituting $\boldsymbol{U}_{Nf}$ for $-\boldsymbol{U}_C$, this current can be obtained as

$$\boldsymbol{I}_{ful\_com} = -3\boldsymbol{U}_C\left(\frac{1}{R_S} + j\omega C_S\right) - \boldsymbol{I}_h . \tag{4}$$

Obviously, if the injected current $\boldsymbol{I}_i$ is controlled to be equivalent to $\boldsymbol{I}_{ful\_com}$, the faulty phase voltage and ground current will be limited to zero, and thus the fault arc can be extinguished. It is notable that expression (3) is derived on the condition that $\boldsymbol{I}_F$ is equal to zero. This condition equals that U_F is equal to zero, which derives

$$\boldsymbol{U}_N = -\boldsymbol{U}_C . \tag{5}$$

That is to say, full ground-current compensation is the same as setting the neutral-to-ground voltage to the inverse of U_C. To make it more general, the line-to-neutral voltage of faulty phase may substitute for U_C. Therefore, full ground-current compensation can be guaranteed by controlling the neutral-to-ground voltage to the inverse of the line-to-neutral voltage of faulty phase. This brings the advantage that only these two voltages need to be detected instead of the complicated ground-current detection which is necessary in traditional arc suppression methods.

TABLE I
PARAMETERS FOR CASE STUDY

	Parameters	Values
Distribution network	Damping ratio d	0.08
	Leakage resistance R_S	15 kΩ
	Nominal distributed capacitance C_S	2.625 uF
	Nominal capacitive current	15 A
	Fundamental frequency f_0	50 Hz
	Line-to-neutral voltage E_X	10.5/√3 kV
	Ground fault resistance R_F	0.01 – 10 kΩ
Active arc suppression device	Isolation transformer ratio N	10.5/√3:0.3
	Isolation transformer capacity	100 kVA
	Isolation transformer leakage inductance (low voltage side)	0.01 mH
	Sample frequency f_s	20 kHz
	Filter inductance L_o	0.5 mH
	Filter inductor ESR r	0.2 Ω
	Filter capacitance C_o	10 uF
	Inverter gain G_{inv}	600
	dc voltage v_d	600 V

II. ACTIVE ARC SUPPRESSION METHOD

A. Model of distribution network

Typical parameters for case study are listed in TABLE I. The distribution network is a 10 kV power system with 15 A capacitive current. As the bolted ground fault rarely happens, the ground fault resistance is chosen to be 10 Ω to 10 kΩ in case study.

The power stage of the distribution network can be modelled in two aspects. One is in fundamental frequency, and it is treated as series connected voltage source $\boldsymbol{E}_0$ and impedance Z_{eq}. The other is in harmonic domain, where it is equivalent to the current source i_h. The resultant model is shown in Fig. 5, where N denotes the ratio of isolation transformer. For further analysis of the control method, the model is converted to low voltage side of the isolation transformer. From Thevenin's theorem, $\boldsymbol{E}_0$ and Z_{eq} can be expressed as

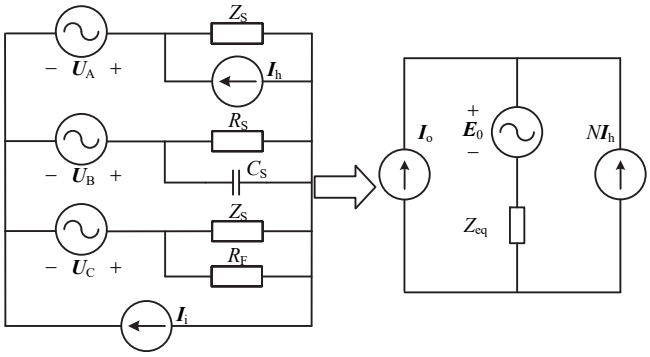

Fig. 5. Equivalent circuit of the distribution network.

$$\boldsymbol{E}_0 = -\frac{\boldsymbol{U}_C}{N}\frac{R_S}{3sR_FR_SC_S + 3R_F + R_S} \tag{6}$$

$$Z_{eq} = \frac{R_FR_S}{(3sR_FR_SC_S + 3R_F + R_S)N^2}. \tag{7}$$

The equivalent voltage source $\boldsymbol{E}_0$ is the asymmetric voltage caused by the asymmetry of the phase-to-ground parameters. The equivalent impedance Z_{eq} denotes the load of the proposed ASD, which is the zero-sequence impedance of the distribution network. Both of them not only depend on the distributed parameters of the network, but also the ground-fault resistance. The damping ratio of distribution networks normally has the value of 3% to 8% [9], which means the leakage resistance is far larger than the capacitive reactance. Thus, the resistance in (7) is negligible when high-resistance ground fault happens, which results a mainly capacitive load to the ASD. It is also notable that the ground-fault resistance is variable from bolted ground fault to high-resistance ground fault. The resistance also varies during the dynamic process of arc ignition.

B. Voltage control method

The control objective of the proposed ASD is to ensure that the neutral-to-ground voltage trace the inverse of the line-to-neutral voltage of faulty phase. With the model of the distribution network analyzed above, a typical dual-loop control method is presented in Fig. 6. Take notice that the leakage inductance of isolation transformer T_i is neglected as it is relatively small (less than 10% of the output inductance) in our case. It is also notable that the disturbance brought by the load change is added to the harmonic source NI_h.

The method includes a neutral-to-ground voltage outer loop and an output inductor current inner loop. As the load impedance may change rapidly, the dynamic performance is critical for the control method. Typical method to deal with load change is to use output capacitor current feedback (CCF) in the inner loop, which can be considered as a combination of filter inductor current feedback (ICF) with load current feedforward (LCF) [23]. It includes the load current disturbance in the inner loop, thus has better dynamic performance than ICF-based method, which excludes the load current from the inner loop, as shown in Fig. 7.

However, it is shown later that the capacitive load of the ASD makes the controller difficult to maintain good tracking performance. Therefore, the ICF is adopted in the inner loop. A feedforward of the filter capacitor voltage is introduced to

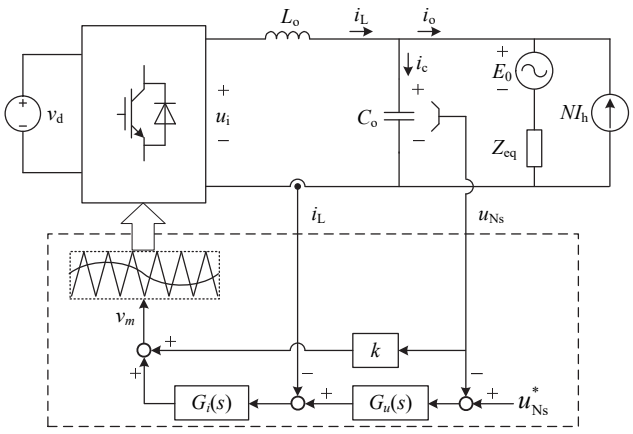

Fig. 6. Active arc suppression system with dual-loop control method.

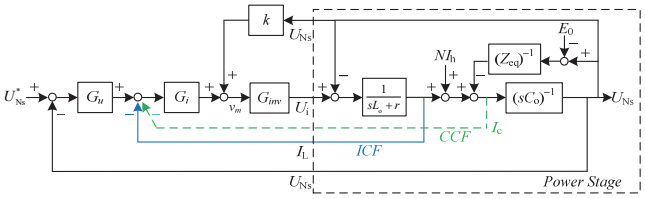

Fig. 7. Block diagram of the dual-loop control method with CCF and ICF.

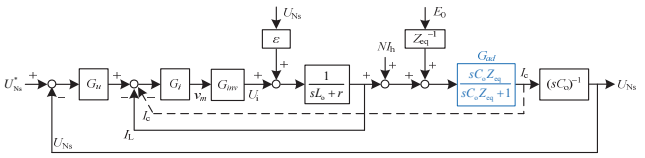

Fig. 8. Simplified block diagram of the dual-loop control methods.

enhance the steady state performance of the inner loop and decouple both control loops.

The block diagram of the dual-loop control method is shown in Fig. 7. The feedforward ratio of the output capacitor voltage is k, which is set to be the reciprocal of the nominal inverter gain G_{inv}. The inner loop can be simplified to Fig. 8 with the introduction of ε, which is a relatively tiny value as the actual value of inverter gain G_{inv} is close to the nominal one.

$$\varepsilon = kG_{inv} - 1 \tag{8}$$

Therefore, the influence of the output capacitor voltage to the inner current loop is diminished and reasonably negligible. Thus, the transfer function from the control signal v_m to output inductor current, which refers to the transfer function of ICF, is simplified to

$$G_{il} = \frac{I_L}{v_m} = \frac{G_{inv}}{sL_o + r}. \tag{9}$$

The asymmetric voltage and harmonic current are treated as the disturbance of the control system. Obviously, they are both in the inner loop when CCF is adopted. This brings an additional function G_{ad} to the forward path comparing to the ICF method, as shown in Fig. 8.

$$G_{ad} = \frac{sC_oZ_{eq}}{sC_oZ_{eq}+1} = \frac{sR_FR_SC_o}{sR_FR_S(C_o+3C_SN^2)+(3R_F+R_S)N^2} \tag{10}$$

The resultant CCF transfer function in the forward path can

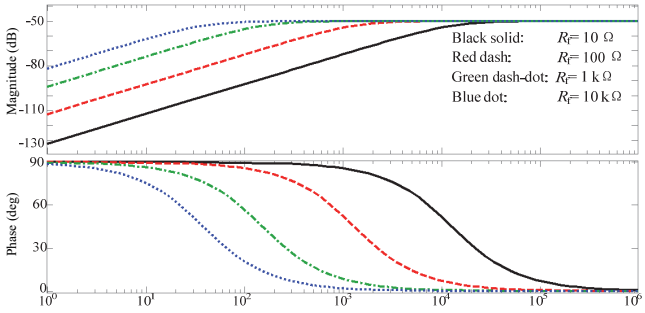

Fig. 9. Bode diagram of G_{ad} when R_F varies and C_S is nominal. (Frequency: rad/s)

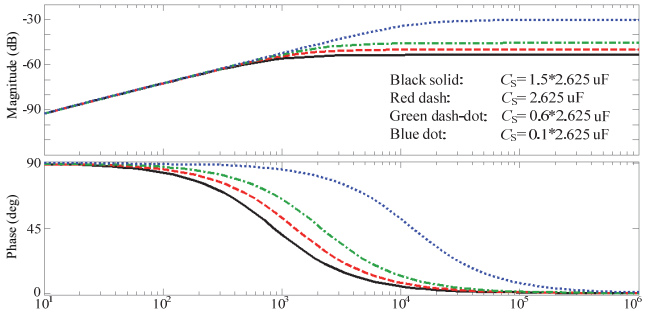

Fig. 10. Bode diagram of G_{ad} as C_S varies and R_F = 100 Ω. (Frequency: rad/s)

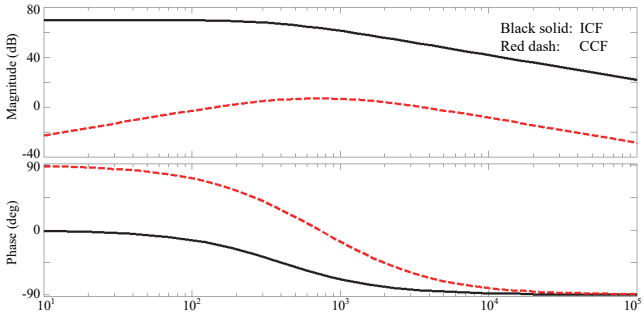

Fig. 11. Bode diagrams of open-loop ICF and CCF transfer function. (Frequency: rad/s)

thus be obtained.

$$G_{ic} = \frac{I_c}{v_m} = G_{il} G_{ad} \tag{11}$$

Obviously, G_{ad} is a first-order high pass filter with a small gain. The corner frequency and fundamental frequency gain depend on the ground-fault resistance and distributed capacitance. Fig. 9 shows the Bode diagram of G_{ad} when R_F varies. The corner frequency decreases as R_F increases, indicating lower fundamental gain in low-resistance grounding than high-resistance grounding. Fig. 10 shows the Bode diagram of G_{ad} as C_S varies. The high band gain decreases when C_S increases, indicating lower anti-interference ability with light load. Fig. 11 shows the Bode diagrams of open-loop ICF and CCF transfer function. Generally, because of the positive slope in low band and low gain in medium band, second-order integrator term and high gain should be adopted in the current controller to obtain reasonable bandwidth for the CCF method. This makes the controller parameters design complicated and brings about resonant point in current loop. Moreover, the −180° phase shift brought by the second-order integrator may

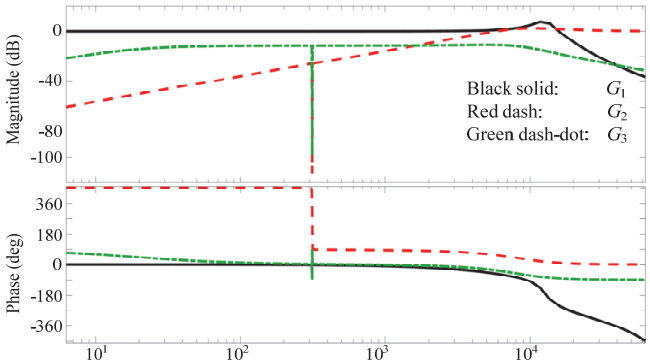

Fig. 12. Bode diagrams of G_1, G_2 and G_3. (Frequency: rad/s)

undermine the stability margin of the inner loop. On the contrary, the ICF method has flatter and larger magnitude in low band than the CCF, making it easy to obtain good steady state performance and stability margin. Thus, the ICF method is adopted in the inner loop.

A practical method to design the current controller is simply using a proportional controller. The proportional gain K_{in} can be easily set by the desired gain and phase margin of the inner loop. Take notice that K_{in} should not exceed $L_o f_s / G_{inv}$ as the discrete system stability demands. The transfer function of the inner loop is then obtained.

$$G_{in} = \frac{K_{in} G_{inv}}{sL_o + r + K_{in} G_{inv}} \tag{12}$$

The outer voltage loop of the controller is designed to achieve zero steady state error in fundamental frequency and enough damping to the ground-fault harmonic current and load transitions. The transfer function of U_{Ns} can be obtained from Fig. 8.

$$U_{Ns} = G_1 U_{Ns}^* + G_2 E_0 + G_3 N I_h = \frac{G_{ad}}{sC_o + G_u G_{in} G_{ad}} \left(G_u G_{in} U_{Ns}^* + \frac{E_0}{Z_{eq}} + N I_h \right) \tag{13}$$

Take notice that G_{ad}/Z_{eq} roughly equals sC_o, and G_{in} is unity in the bandwidth of outer loop, then G_2 can be derived to

$$G_2 = \frac{sC_o}{sC_o + G_u G_{in} G_{ad}}. \tag{14}$$

As $G_{ad}/(sC_o)$ results to a first-order low pass filter, it can be concluded that if G_u has infinite gain at fundamental frequency, G_2 will approach zero at the frequency, meaning that E_0 can be perfectly suppressed.

As the harmonic components of the ground-fault current are mainly in the 3rd, 5th, and 7th order, it seems simple to achieve harmonic damping by adding resonant controllers with corresponding resonant frequencies to the voltage controller [24]. Nevertheless, it makes the design of the controller complicated and increases the calculation burden to the processor. In fact, $G_{ad}/(sC_o)$ in the forward path provides some damping to the harmonics, simple PI plus Resonant controller can achieve good control performance.

$$G_u = K_p + \frac{K_i}{s} + \frac{2K_r s}{s^2 + \omega_0^2} \tag{15}$$

The resonant controller in G_u has the resonant frequency ω_0

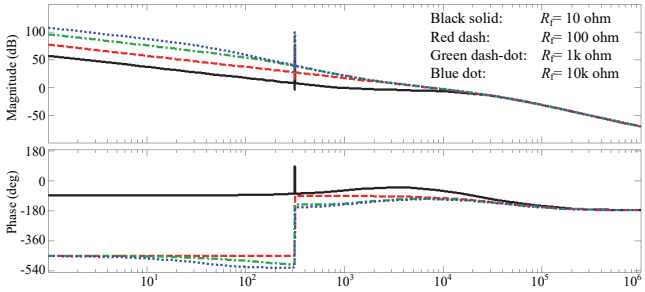

Fig. 13. Bode diagrams of voltage-loop forward path function under different ground fault resistances. (Frequency: rad/s)

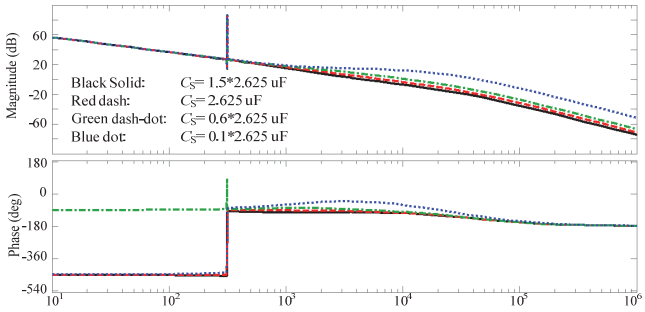

Fig. 14. Bode diagrams of voltage-loop forward path function under different distributed capacitances. (Frequency: rad/s)

in fundamental frequency. The turnover frequency K_i/K_p of PI controller in G_u can be chosen to cancel the coupling pole produced by $G_{ad}/(sC_o)$ for avoiding undesired peak in closed loop [25]. The other parameters in G_u can be designed by desired overall bandwidth and stability margin. As several literatures [23]-[29] have addressed the outer-loop control parameter design, this is not further elaborated. After careful choosing of the parameters, the Bode diagrams of the transfer functions in (13) are drawn in Fig. 12. The designed forward path transfer function has infinite gain in fundamental frequency, this not only achieves zero steady state error, but also provides enough suppression of E_0. Generally, as the main harmonic frequencies are within the bandwidth of the outer-loop controller, larger gain can provide greater damping to the harmonics [29]. However, the larger bandwidth undermines the suppression of high-order interference signals.

The forward path functions of voltage loop under different ground-fault resistances are shown in Fig. 13. The resistances mainly affect the low frequency band, where open-loop gain increases as the ground-fault resistance gets larger. Thus, better tracing performance in fundamental frequency together with better suppression of low frequency harmonic currents can be expected in high-resistance ground faults. The crossover frequency tends to slightly increase as the ground fault resistance gets larger, which means larger bandwidth and faster response in high-resistance ground fault. These features are beneficial as the actual ground-fault resistance is mostly high.

The forward path functions of voltage loop under different distributed capacitances are shown in Fig. 14. Different from the aforementioned conditions, the performance in high-frequency band is mainly affected by the distributed capacitance. The overall bandwidth and phase margin tend to decrease as the load become heavier. This means appropriate nominal capacitance level should be estimated as the distributed capacitance tends to increase with the expansion of

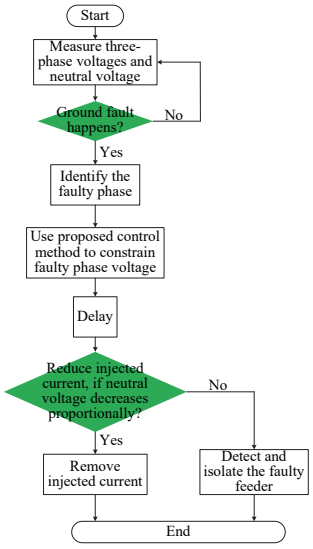

Fig.15. Implementation flowchart of the proposed ASD.

the distribution network.

C. Implementation

Two issues should be addressed while implementing the proposed ASD to a real distribution system. Firstly, the ASD mainly focuses on full compensation of grounding fault current. That is to say, it is assumed that the recognition of faulty state is fully and precisely accomplished. Secondly, different fault type leads to different post-fault measure. For instance, when instantaneous fault happens, current injection should be stopped after certain time as the fault disappears spontaneously; nevertheless, it should not be stopped until the faulty feeder is precisely identified when permanent fault happens as the fault arc is supposed to last.

The implementation flowchart of the proposed ASD is shown in Fig.15. Firstly, the single-phase-to-ground fault is detected and the faulty phase is identified. Then, a current is injected to the neutral point by the proposed ASD for constraining the faulty phase voltage. After certain delay, the injected current is reduced for fault type recognition. If the neutral voltage decreases proportionally, it indicates an instantaneous fault and the injected current would be removed. Otherwise, it indicates a permanent fault and faulty feeder detection method should be carried out. Finally, the faulty feeder should be isolated by disconnecting the corresponding breaker.

III. EXPERIMENTAL RESULTS

A 20 kVA prototype is developed in laboratory as shown in Fig. 16 with the parameters in TABLE II. It operates under the line voltage of 380 V. The nominal capacitive current is thus set to a larger value of 40 A for better performance presentation. The harmonic current source is denoted by a single-phase uncontrollable rectifier with L-type input filter and RC-type load which has a crest factor of 1.75 [23]. The control method and parameter design follows the guideline of Section II, Part B. The gain and phase margin of inner current loop are set to 6 dB and 47°, respectively. Taking into consideration the total delay of digital control ($1.5/f_s$), the inner-loop proportional ratio K_{in} can be obtained as shown in TABLE II. The overall bandwidth

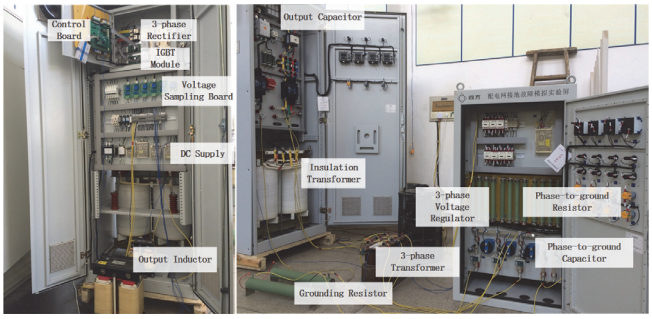

Fig. 16. Experimental system.

TABLE II
EXPERIMENTAL PARAMETERS

coefficients	Values
Nominal phase-to-ground resistance R_S	200 Ω
Nominal phase-to-ground capacitance C_S	200 uF
Nominal capacitive current	40 A
Line-to-neutral voltage E_X	220 V
Grounding fault resistance R_F	100 Ω, 10 kΩ
Isolation transformer ratio N	1:1
Isolation transformer capacity	20 kVA
Switching frequency f_{sw}	10 kHz
Filter inductance of nonlinear load	10 mH
Load capacitance of nonlinear load	2000 uF
Load resistance of nonlinear load	15 Ω
Inner-loop proportional ratio K_{in}	0.0265
Outer-loop proportional ratio K_p	4.1
Outer-loop Integral ratio K_i	73.4
Outer-loop Resonant ratio K_r	1

is set to be 17.2 krad/s with a gain margin of 3 dB and phase margin of 45°. The turnover frequency of PI controller in G_u is set under the nominal phase-to-ground parameters. Therefore, the parameters of outer-loop controller can be obtained.

As the load of ASD is mainly capacitive, a critical issue of experimentation is to constrain the surge current at the beginning of power switch action. Thus, a current limiter is added to the output of voltage controller to constrain the output current within the bearable extent. This limiter is set to ±100 A according to the capacity of prototype. As the theoretical analysis indicates that the distributed capacitance, ground-fault resistance and harmonic content of the ground current influence the compensation performance, the experiment mainly focuses on these parameters and is carried out in three groups.

The first group shows the inception of the ASD when a 10 kΩ ground fault in phase C and the nominal phase-to-ground capacitance have been set. Fig. 17 shows the dynamic waveforms of the neutral voltage, faulty phase voltage and injected current. Take notice that the neutral voltage error is almost the same as the inverse of faulty phase voltage, thus it is not shown here. Besides, as the fault resistance is very large, the ground current is hard to be measured, thus it is indirectly shown from the faulty phase voltage. The dynamic waveforms in Fig. 17 show that the neutral voltage changes from almost zero to line-to-neutral voltage after a short duration. This makes the faulty phase voltage approach zero accordingly. A slight overshoot can be observed from the faulty phase voltage, however, the instantaneous value reaches less than 15 V after 5 ms, indicating good dynamic performance. A step can be found in current waveform as the current limiter constrains the reference current within certain extent.

The second group shows the inception of distributed capacitance changes from nominal to 1.5 nominal value when

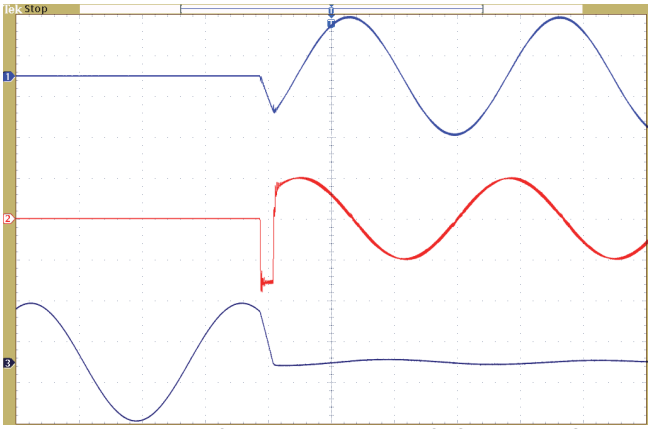

Fig. 17. Transient waveforms at the inception of ASD with 10 kΩ ground fault resistance and nominal capacitance (Ch. 1: neutral voltage 210 V/div, Ch. 2: injected current 60 A/div, Ch. 3: faulty phase voltage 210 V/div, t: 6 ms/div)

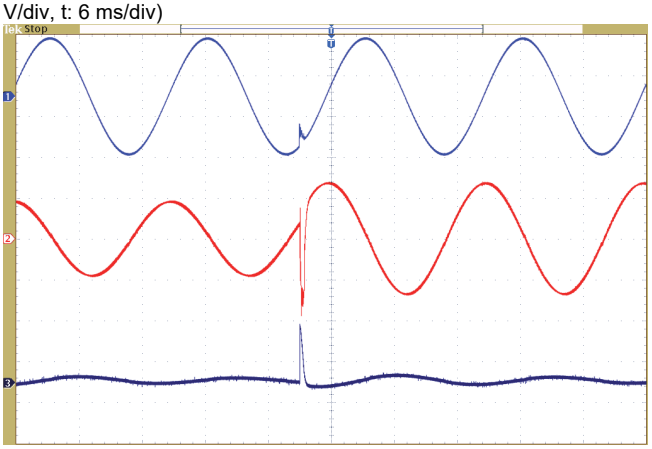

Fig. 18. Transient waveforms at the inception of capacitance change from nominal to 1.5 nominal value with 100 Ω ground fault resistance (Ch. 1: neutral voltage 210 V/div, Ch. 2: injected current 65 A/div, Ch.3: faulty phase voltage 70 V/div, t: 8 ms/div)

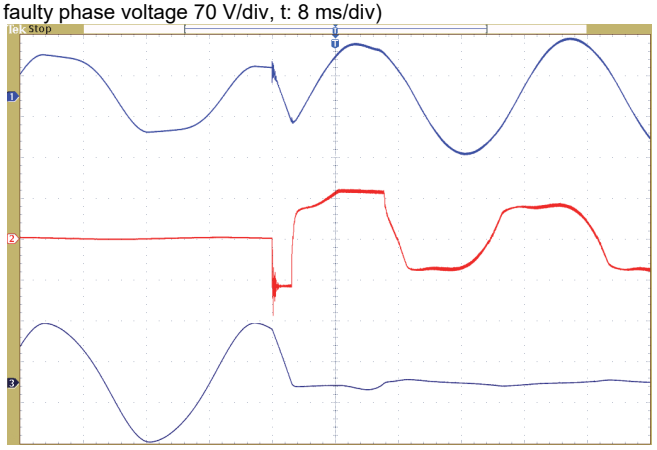

Fig. 19. Transient waveforms at the inception of ASD with 100 Ω ground fault resistance, nominal capacitance and nonlinear load (Ch. 1: neutral voltage 210 V/div, Ch. 2: injected current 80 A/div, Ch. 3: faulty phase voltage 320 V/div, t: 6 ms/div)

the ASD and a 100 Ω ground resistor have been set. It can be observed from Fig. 18 that the neutral voltage returns to the same track after a transient of about 2 ms. The faulty phase voltage gives a better presentation of the dynamic response. Overshoot up to 90 V can be observed in the voltage, while the resultant fault current remains small as the ground-fault resistance is relatively large. Larger voltage error after the

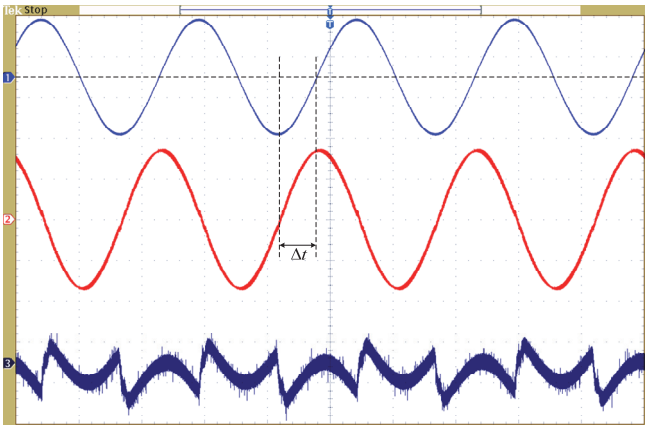

Fig. 20. Steady state waveforms when 100 Ω ground fault resistance, nominal capacitance have been set (Ch. 1: neutral voltage 210 V/div, Ch. 2: injected current 35 A/div, Ch. 3: faulty phase voltage 1.5 V/div, t: 8 ms/div)

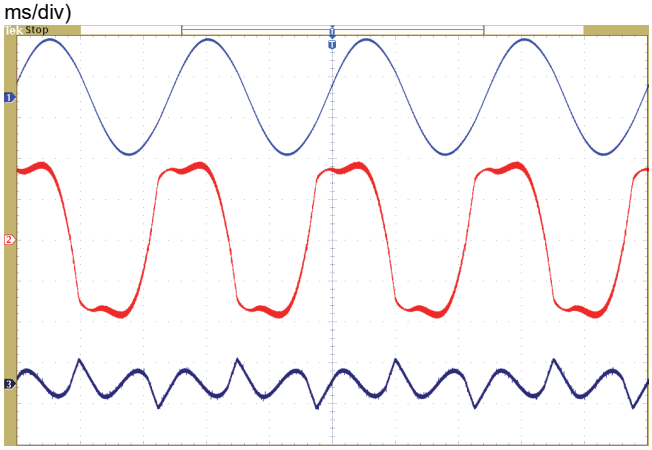

Fig. 21. Steady state waveforms when 100 Ω ground fault resistance, nominal capacitance and nonlinear load have been set (Ch. 1: neutral voltage 210 V/div, Ch. 2: injected current 35 A/div, Ch. 3: faulty phase voltage 10 V/div, t: 8 ms/div)

change of capacitance can be observed as the open-loop bandwidth decreases according to theoretical analysis.

The third group shows the inception of the ASD when nonlinear load, nominal capacitance and 100 Ω ground fault resistance have been set as shown in Fig. 19. Longer response time can be observed than the linear load case. This is because of the greater current surge brought by the harmonic voltage output of the ASD. Enlarging the limiter extent may quicken the response, however the resultant larger output current surge threaten the safety of power switches.

Comparing the dynamic waveforms with those presented in literature [22], it shows that the response time of the proposed ASD is greatly reduced from around 120 ms to less than 20 ms. This is mainly caused by the complicated control process and the FFT method used for reference current in the literature.

The steady state waveforms are shown in Fig. 20 and Fig. 21. The first figure shows the waveforms under linear load while the other one is under nonlinear load, both with nominal phase-to-ground capacitance and 100 Ω ground-fault resistance. From Fig. 20, slight switching frequency harmonics can be observed in the output current, together with good steady state performance in faulty phase voltage as it approaches zero. It can also be observed that the lag of the neutral voltage to the injected current (Δt) is around 4.8 ms or 86°. As the reference

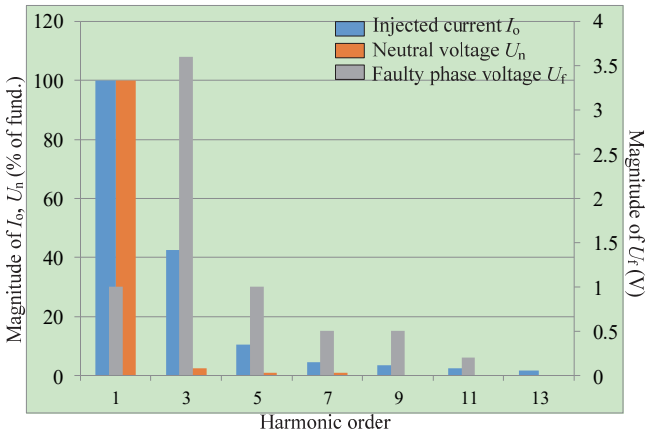

Fig. 22. Spectrum analysis of steady state waveforms in Fig. 21.

directions of the injected current and neutral voltage in Fig. 1 are non-associated, it results a power factor of 0.06 and a proportion of active power injection to the neutral, which roughly meets the relationship presented in (3). In Fig. 21, a neutral voltage with a smooth sinusoidal waveform can be observed. Spectrum analysis shown in Fig. 22 indicates its total harmonic distortion (THD) reaches 3.5%, comparing to 13.2% before the ASD is connected which can be observed from the first period of Fig. 19. The resultant faulty phase voltage is less than 5 V in RMS value, indicating good ground-current compensation performance in steady state.

IV. Conclusion

The active ground-fault arc suppression device can realize compensation of the active, reactive and harmonic currents, and is able to achieve better arc-extinguishing performance than traditional arc suppression coil. The voltages of the distribution networks are used to realize the full current compensation, achieving faster response and better robustness than the capacitive current based device. The experiment carried out on a prototype validates the effectiveness of the proposed device.

The advantages of the proposed method comparing to other active ground-fault arc suppression methods can be summarized in three aspects. Firstly, no reactive component is used and thus the resonance problem is avoided. Secondly, there is no need to conduct the capacitive current or phase-to-ground parameters detection, and thus the response time and compensation error are both decreased. Finally, the instantaneous value of neutral voltage is controlled directly instead of using the time-consuming FFT method, which further decreases the response time.

Drawbacks of this device include the high cost and low reliability of large-capacity use which is practical to the MV power system. This may be solved by the combination of the ASD and passive component e.g. ASC, MCR. However, the aforementioned resonant problem brought by this combination should be carefully handled.

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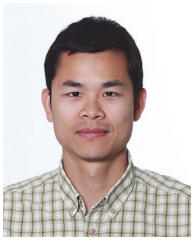

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