Low-Jitter GaN E-HEMT Gate Driver with High Common-Mode Voltage Transient Immunity

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***Abstract*—An improved gate driver is presented which significantly lowers the output noise of high-precision switch-mode (Class-D) power amplifiers by reducing signal jitter at the output of the power stage tenfold to values below 20 ps. Gate signal jitter in power electronic converters, which introduces wideband noise to the power output, originates mainly from the signal isolators that are required to provide the galvanically isolated gate driver control signals. A low-jitter gate control signal is produced by employing a digital flip-flop, which uses a low-jitter isolated clock, to re-synchronize the jittery gate control signal. By utilizing the clock-enable input of the flip-flop, the gate driver can be rendered immune to high-speed common-mode transients, which is important as the Class-D power amplifier demonstrator system employs fast-switching GaN E-HEMT transistors, where the 400 V switching transients exceed 300 kV µs^{-1}. The signal to noise ratio of a sinusoidal output signal is measured at 107 dB, which is an improvement of ≈20 dB as compared to the performance of a conventional gate driver.**

***Index Terms*—Low-jitter gate driver, common-mode transient immunity (CMTI), low noise switch-mode power amplifier, wide-bandgap gallium nitride power semiconductors, signal to noise ratio (SNR)**

I. Introduction

IMPORTANT industry applications, ranging from mechatronic wafer handling systems in integrated circuit manufacturing to X-ray computer tomography, require low-noise and low-distortion currents and/or voltages at power levels up to several kilowatts in order to, e.g., provide nanometer-range mechanical positioning or precise electron beam trajectories [1]–[3]. For positioning systems, the power amplifier output signal, which is usually a force or torque producing current, must be of low noise and low distortion in a limited frequency range from DC to ≈10 kHz, as undesired forces or torques at higher frequencies are sufficiently attenuated by the mechanical systems and do not lead to disturbing movements. The actuator current's signal to noise ratio (SNR) in this 10 kHz bandwidth should be ≈110 dB in order to meet industry requirements [4]. Such high SNR values are commonly reached using linear or hybrid power amplifiers [5], whereas state-of-the-art switch-mode systems usually only achieve SNR values in the range of $80 - 100$ dB [6]–[8]. However, switch-mode power converters are desired for such applications as they are more efficient, better scalable and can provide higher output powers than their hybrid or linear counterparts [5], [9]. Furthermore, digital control of such amplifiers is also preferred over analog control due to increased flexibility and robustness as well as quicker development and maintenance processes.

Signal jitter of the gate control signals in a switch-mode power converter, which is always present in digital systems, introduces considerable wideband noise to the converter's output by randomly varying the time instants of the signal transitions, which limits the achievable SNR. Accordingly, this paper describes an improved isolated gate driver capable of significantly reducing the jitter of the digital gate control signals and hence, the switched power waveforms. **Fig. 1** depicts the utilized hardware demonstrator featuring four half-bridges with gallium nitride (GaN) Enhancement-mode High-Electron-Mobility power Transistors (E-HEMT, *GaN Systems GS66508T*, 650 V, 30 A, 50 mΩ), equipped with the presented low-jitter gate drivers. Using this system, jitter and noise measurements are performed on two individually operating half-bridges with output powers up to 1 kW. One half-bridge features the low-jitter gate drivers and the other uses a regular gate driving method for comparison. A performance gain of up to 20 dB in the SNR of a sinusoidal half-bridge output is achieved with the improved gate driver, reaching 107 dB.

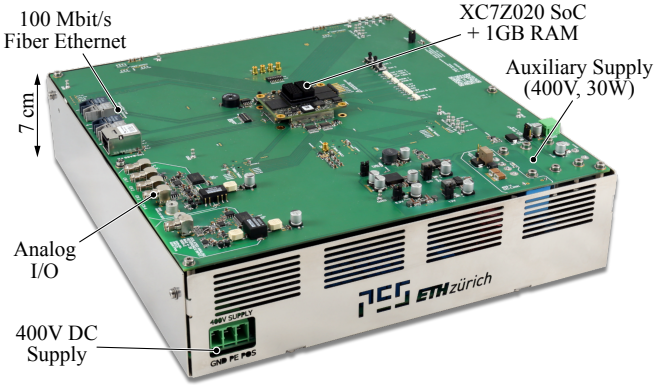

Fig. 1. High-precision power amplifier demonstrator comprising eight low-jitter gate drivers in four GaN half-bridges which can be interleaved in groups of two for single-phase DC/AC operation. The system features a 400 V DC input, 8 kVA peak output power and high-precision voltage/current sensors.

The utilized GaN transistors enable extremely fast switching transitions, low dead times and high switching frequencies

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while achieving low on-state resistances and low switching losses [10], [11], which lowers distortion in the power amplifier's output signal [12]. However, the fast switching transitions of a half-bridge switch-node voltage appear as a common-mode (CM) voltage transient across the isolation barrier of the signal isolator devices which transmit the gate control signal to the isolated gate drivers of high-side switches. These devices (i.e., optocouplers or digital signal isolators) are often rated for a CM transient of $< 100\,\mathrm{kV\,\mu s^{-1}}$, which is easily surpassed with modern GaN transistors, as the measurements in [10], [13] and this work show. Upon exceeding this rating, the signal isolators are prone to producing short-lived erroneous output signals that could lead to a faulty turn-on of a half-bridge transistor and hence to a potentially destructive short-circuit of the DC-link capacitors. Consequently, the presented low-jitter gate driver is rendered immune to faulty outputs from the signal isolators, which is necessary for reliably operating such fast-switching power converters. Initial considerations towards a low-jitter gate driver with a high CM immunity have been presented in [13]. This work introduces an additional circuit variety and further details of its operating principle. Moreover, measurements on a new demonstrator system are given and the performance of the proposed gate driver in a side-by-side comparison with a state-of-the-art solution is presented in order to directly demonstrate the advantages.

Section II introduces the set of problems caused by signal jitter in digitally controlled power electronics converters. **Section III** details the improved gate driver circuit and **Section IV** presents measurements and performance figures of the proposed driver in comparison to a regular gate control configuration. Ultimately, **Section V** summarizes the achieved results.

II. Signal Jitter in a Power Electronics Context

A pair of power-electronic switches acting complimentarily (e.g., arranged in a half-bridge configuration) is commonly controlled by a single binary (1-bit) signal encoding the state of the two switches. If this control signal originates from a digital processing system (as opposed to, e.g., an analog pulse-width modulator), the switches can be regarded as a digital to analog converter, as their switching action converts the binary control signal into a physical quantity. In this case, the idealized switch-node voltage is an (amplified) copy of the binary control signal, whereas the entire information carried by the binary control signal is embodied solely in the time-instants of its state transitions [14]. In power electronics, the encoding from information to a binary signal is often achieved using a pulse-width modulator (PWM) [15]. Due to non-idealities associated with power electronic switches such as non-zero switching times or on-state resistances, or clock frequency limitations in digital processing systems, among others, noise and distortion are added to the converter's output signal [12], [13]. These additional signal components are unwanted, as they are added during the digital to analog conversion and are not encoded by the original binary switch control signal. Accordingly, they reduce the SNR and increase the harmonic distortion of the converter's output.

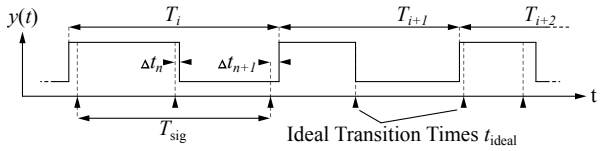

Fig. 2. A binary periodic signal $y(t)$ is subject to jitter and increased noise if its edges are shifted by Δt_n, which often follows a stochastic probability distribution, away from their ideal transition times.

This work investigates signal jitter, another undesired phenomenon which especially affects binary signals and limits the achievable SNR. In the time-domain, it can be regarded as a stochastically varying time delay in a signal's path. For a binary signal, this effect shifts the signal transitions away from their ideal time instants and thus alters its information content [16]–[18]. If the jitter is of stochastic nature, noise is usually added to the signal's spectrum, e.g., jitter following a normal probability distribution usually introduces white noise [19]. In common digital systems, the shifts in the signal transitions are usually in the sub-ns domain [20].

Fig. 2 shows a jittery periodic binary signal $y(t)$, which could be the gate control signal of a half-bridge's high-side switch or the (idealized) half-bridge switch-node voltage. The jitter expresses itself as the time-dependent deviations Δt_n of the signal's edge positions from their ideal instants t_{ideal}. Note that the jitter changes the signal's period T_{sig} such that each subsequent period has a slightly different duration T_i. Throughout this work, jitter is measured by acquiring the durations T_i of randomly selected periods. The RMS value of the jitter, given that N periods are recorded, and under the assumption of a Gaussian distribution, can then be given as:

$$T_{\mathrm{Jit,RMS}} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(T_i - T_{\mathrm{avg}})^2}, \tag{1}$$

with

$$T_{\mathrm{avg}} = \frac{1}{N}\sum_{i=1}^{N} T_i \;\approx T_{\mathrm{sig}}. \tag{2}$$

Note that $T_{\mathrm{Jit,RMS}}$ is the standard deviation of the randomly sampled periods T_i [16]. As the periods T_i follow a stochastic process, a sufficient number of samples N must be recorded in order to correctly assess the RMS value. Often, $1000 < N < 10000$ is sufficient [21].

As shown in [22], $T_{\mathrm{Jit,RMS}}$ can be used to derive the best achievable SNR (in a bandwidth f_{BW}) of a sinusoidal, pulse-width modulated signal:

$$\mathrm{SNR}_{\max} = 20\log_{10}\left(\frac{m}{4\sqrt{2}\cdot T_{\mathrm{Jit,RMS}}}\sqrt{\frac{T_{\mathrm{PWM}}}{f_{\mathrm{BW}}}}\right), \tag{3}$$

where T_{PWM} equals to the period T_{sig} of the modulated signal and m is the modulation index: $0 \leq m \leq 1$.

From (3) and [13], it is evident that even signal jitter values in the picosecond range, together with common power electronics PWM frequencies, can easily limit the achievable SNR to values below $100\,\mathrm{dB}$. Consequently, the origins and

magnitudes of jitter in power converters must, depending on the application, be carefully analyzed.

A digital signal often accumulates jitter as it passes through integrated circuits like DSPs, FPGAs, logic gates or signal buffers. However, these contributions are usually miniscule and only significant in high-speed data transmission systems [16]. Electromagnetic interference can also contribute to signal jitter, usually through crosstalk with closely located digital signals. In power converters, fast changing switch-node voltages can be a substantial source of jitter-inducing EM fields. Careful signal routing must be employed to minimize the influence from such sources [23]. However, the most prominent source of jitter in power converters are signal isolation circuits, such as commonly used optocouplers or non-optical digital signal isolators, which are used to transmit a digital signal across a galvanic isolation barrier. **Fig. 3** depicts a half-bridge switching leg which is a typical building block of power converters and consists of two power transistors, T_1 and T_2 and their respective gate driver circuits. In order to allow any control system reference potential between the potentials U_{POS} and U_{NEG} of the DC link rails, T_1 and T_2 require a galvanically isolated gate driver circuit, as the driver's reference potential (the transistor's source contact) is not identical to the control circuit's reference potential and may also change rapidly upon switching transitions of the half-bridge output $u_{\mathrm{Out}}(t)$.

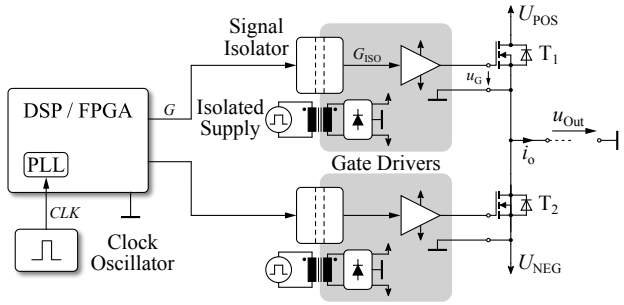

Fig. 3. Conventional half-bridge switch arrangement with two power transistors, their gate drivers and a digital gate signal source. The signal isolator contributes jitter to the isolated signal G_{ISO}.

Digital signal isolators feature shorter propagation delay times, stricter propagation delay tolerances and a higher CM transient withstand capability across their isolation barrier than optocouplers and are thus expected to perform better in low-distortion applications where the signal integrity is of importance [24], [25]. The usage of discrete signal isolation transformers is also discouraged as they cannot transmit DC signals, are also prone to malfunction when subject to fast-switching CM transients and tend to become bulky when operating at low frequencies. Furthermore, integrated half-bridge drivers have the disadvantages of a low CM transient withstand capability, are not galvanically isolated and are prone to latch-up [26], [27].

Digital signal isolators are based on either capacitive or inductive coupling across an isolation barrier. In order to be able to transmit a DC signal, the isolators use internal signal modulation schemes which seem to add significant amounts of jitter to the isolator's output signal [13], [24], [28]. Jitter data of signal isolators are rarely provided, but the authors have found no signal isolator with RMS jitter figures below several tens of picoseconds [29], which is still significantly higher than the jitter of the proposed low-jitter gate driver circuit, which is presented in the following.

III. Isolated Gate Driver with Reduced Jitter

There are several methods to reduce the jitter of a periodic digital clock signal, among them are jitter filters based on phase locked loops (PLLs) or controlled oscillators, which are usually employed in isolated analog to digital converters to produce the low-jitter sampling clock signal [20], [30], [31]. However, these methods are only applicable to periodic clock signals with a fixed duty cycle, which is not the case for modulated gate control signals.

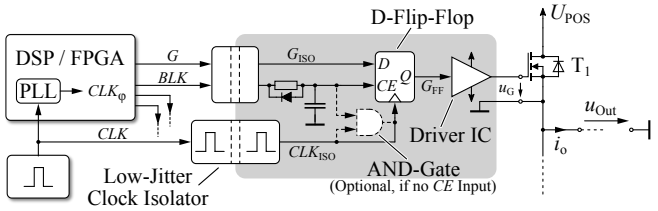

Fig. 4. Proposed gate driver which significantly reduces jitter and is immune to output voltage transitions with a high $\mathrm{d}u/\mathrm{d}t$. If the flip-flop does not provide a clock-enable input, a logic AND gate can be used to gate the flip-flop's clock signal. The isolated supply and the identical driver of the second transistor T_2 of the bridge leg are not shown.

Hence, this work proposes the circuit depicted in **Fig. 4** to eliminate the jitter introduced to the gate signal by the signal isolator and thus to provide a very low-jitter gate signal to the switching transistor. The circuit utilizes a basic concept proposed in [32], but improves it by not using an isolated clock generation device to reduce complexity. Furthermore, the circuit is rendered immune to fast CM voltage transients, i.e., it prevents a faulty turn-on or turn-off of the power transistor in case the signal isolator emits erroneous signals during switch-node voltage transients of high $\mathrm{d}u/\mathrm{d}t$.

The key component of this gate driver is a clock-edge triggered D-type flip-flop which is used to re-synchronize the jittery gate control signal G_{ISO} after the signal isolator onto a low-jitter clock signal CLK_{ISO}, which is synchronous to the system's global clock signal *CLK* and supplied to the isolated gate driver using a small signal transformer which is capable of operating with frequencies in excess of $100\,\mathrm{MHz}$. The clock isolation transformer is driven by a high-speed, low-voltage differential signal (LVDS) driver, and an LVDS receiver is used to recover CLK_{ISO} from the transformer's secondary [33]. As shown in [13], this technique adds $\approx 6\,\mathrm{ps}$ of RMS jitter to CLK_{ISO} as compared to the *CLK* signal, which is derived from an integrated low-jitter oscillator ($\approx 3.3\,\mathrm{ps}$ RMS jitter). As mentioned in **Sec.** II, this clock isolator cannot be used to transmit the gate control signal (only AC signals are possible and this isolator has an insufficient CM transient rejection). The functionality of the logic AND-gate and the flip-flop's clock-enable input in **Fig. 4** is explained in **Sec.** III-A.

Fig. 5 depicts the timing waveforms of the different signals used in the gate driver circuit. In order to fulfill the flip-flop's setup/hold timing and thus to prevent a potentially unstable flip-flop output, the clock used for the DSP/FPGA, CLK_φ, must potentially be shifted in phase relative to the isolated clock CLK_{ISO}, such that, ideally, a signal transition of G_{ISO} coincides with the falling edge of CLK_{ISO}. As G_{ISO} is a jittery signal, its worst-case signal transition instants must be used to assess the flip-flop timing. Discrete flip-flops typically have setup/hold times below $500\,\mathrm{ps}$ [34]. The required phase shift, which mainly depends on the propagation delay of the gate signal isolator $T_{\mathrm{pd,ISO}}$ and of the clock isolator, can be accomplished by, e.g., using on-chip digital clock managers of the gate signal generating FPGA [35]. If such an integrated phase-shifting feature is not available, an additional configurable delay line can be utilized. As multiple such gate drivers may be present in a power electronics converter, it is necessary that the signal propagation delays of the clock and gate control signals are matched between different gate drivers, such that the setup/hold timings are as similar as possible for all flip-flops in order to prevent timing violations. This may necessitate length matching of the signal traces and may restrict the worst-case device-to-device skew of the signal isolator's propagation delay. If the flip-flop's timing cannot be guaranteed by design, it is possible to place a second flip-flop after the first one in order to significantly reduce the possibility of an unstable flip-flop output [36]. The maximum frequency of the clock signal *CLK* at which the circuit can operate depends only on the limitations of the used devices like the flip-flop or LVDS drivers/receivers. Experiments show that $100\,\mathrm{MHz}$ poses no problems, whereas at $200\,\mathrm{MHz}$, the signal integrity of the LVDS receivers used in the clock isolation circuit decreases significantly, which prohibits a reliable operation of the flip-flop [37].

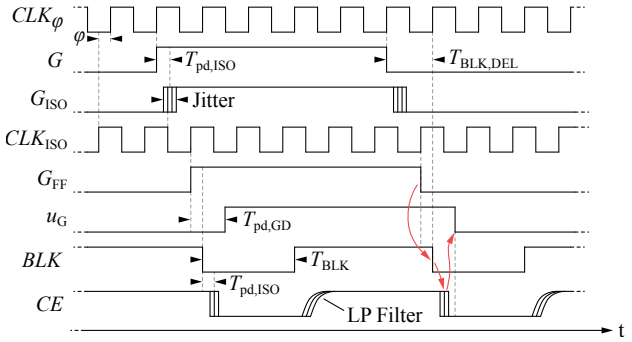

Fig. 5. Timing waveforms of the proposed circuit. CLK_φ is used by the digital control system. *BLK* and *CE* are used to render the system immune to bridge leg output transitions with a high $\mathrm{d}u/\mathrm{d}t$. $T_{\mathrm{pd,ISO}}$ and $T_{\mathrm{pd,GD}}$ are the propagation delays of the signal isolator and the gate driver IC. The required sequencing of G_{FF}, *BLK* and *CE* is indicated with arrows.

In the following, it is shown how the flip-flop's clock-enable input can be used to render the circuit immune to faulty outputs of the signal isolator during fast switching actions of the power transistors.

A. CM Transient Immunity

In typical power converter circuits, the switch-node voltage appears across the isolation barrier of the high-side transistor gate driver signal isolator, i.e., with reference to **Fig. 3**, the signal isolator of T_1, whose output side is connected to the source connection of T_1, is subjected to $u_{\mathrm{Out}}(t)$ across its isolation barrier. Unfavorably, signal isolators are rated only for a certain $\mathrm{d}u/\mathrm{d}t$ of their isolation barrier voltage (usually $50\,\mathrm{kV\,\mu s^{-1}}$ to $100\,\mathrm{kV\,\mu s^{-1}}$), without producing faulty output signals [25], [28], [38], [39]. These values are easily exceeded, at least during portions of the voltage transition of fast switching GaN or SiC power transistor half-bridge circuits ([10], [13]). The gate driver circuit of **Fig. 4** is designed to prevent the transmission of faulty control signals from the signal isolator through the flip-flop to the gate driver IC during switch-node transients and thus avoids an undesired and potentially destructive turn-on (or turn-off) of the associated power transistor.

The central concept is a second control signal (the blanking signal *BLK*) which is used to disable the flip-flop, i.e., it conserves its output G_{FF} regardless of a potentially faulty data input *D* (cf. **Fig. 4**). A passive RC low-pass filter in the blanking signal's path prevents temporary (nanosecond range) erroneous signals potentially emitted by the signal isolator during fast switch-node transients from re-enabling the flip-flop during the ongoing transient. In order to be able to quickly disable the flip-flop before a switch-node transient is initiated by the switching transistor, a signal diode is placed across the resistor of the low-pass filter.

In order to disable the flip-flop, its clock-enable (*CE*) input can be used or, if such an input is not available, a logic AND gate controlled by the *BLK* signal can disable the flip-flop's clock signal as illustrated with dotted lines in **Fig. 4**. The required control of the *BLK* signal is identical in both configurations.

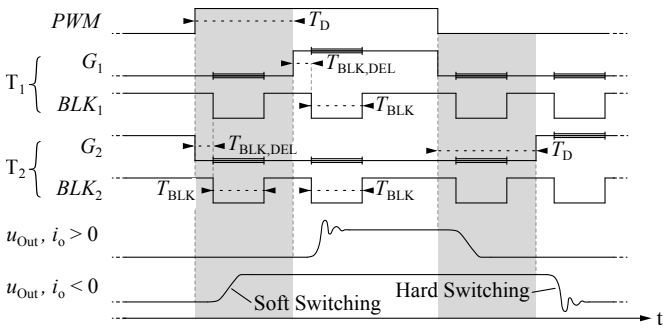

Fig. 6. Blanking signal control for the two half-bridge transistors T_1 and T_2, controlled by a binary PWM signal. The blanking delay time $T_{\mathrm{BLK,DEL}}$ ensures that the flip-flop can update its output. During the blanking time T_{BLK}, the switch-node voltage transition occurs and *BLK* is held low to disable the flip-flop. After the dead time T_{D}, the complimentary transistor is switched. The switch-node voltage $u_{\mathrm{Out}}(t)$ is drawn for both polarities of the half-bridge output current.

The waveforms of the *BLK* and *CE* signals is also illustrated in **Fig. 5**. Note that the required sequencing of the control signals G_{FF}, *BLK* and *CE* is indicated with red arrows. The flip-flop must be disabled (*CE* pulled low) before the gate

driver initiates the switch-node transition by changing the gate voltage u_{G}. Additionally, **Fig. 6** illustrates the blanking sequence and the required timing for both gate drivers of a half-bridge configuration. The blanking delay time $T_{\mathrm{BLK,DEL}}$ ensures that the flip-flop can update its output before it is disabled by pulling *BLK* low. As common gate drivers have a propagation delay in the range of $5\,\mathrm{ns}$ to $50\,\mathrm{ns}$, and the charging/discharging of the transistor's gate capacitance also takes some time, $T_{\mathrm{BLK,DEL}}$ is usually smaller than $\approx 30\,\mathrm{ns}$ in order to disable the flip-flop before the fast switching transition happens. The flip-flop is disabled during the blanking time T_{BLK}, in which the switch-node potential undergoes its transition. After the dead time T_{D} has elapsed, which is the amount of time required to prevent a simultaneous turn-on of both half-bridge transistors and a short-circuit of the DC link rails, the complimentary transistor's gate signal is toggled and another blanking cycle is initiated. Both gate drivers go through a blanking cycle if any of the two gate signals change, which is required as the polarity of the output current defines which gate signal (G_1 or G_2) finally initiates the switch-node transition. A state-machine in the gate signal generating FPGA can be used to control the timing of the gate and blanking signals.

This system limits the minimum dead time and minimum pulse widths, as time must be allotted for the blanking cycle ($T_{\mathrm{BLK,DEL}} + T_{\mathrm{BLK}}$) and the low-pass filter in the path of the *BLK* signal, during which the bridge leg's output state cannot be changed. In the demonstrator system, the timing values presented in sec. IV-A proved viable. Additionally, the flip-flop introduces a time delay of one digital clock period $1/f_{\mathrm{CLK}}$ to the gate signal's path. However, as the digital clock frequency is usually $>100\,\mathrm{MHz}$, this delay is negligible. Furthermore, the dielectric of the signal isolator could be subject to accelerated aging due to dielectric losses, which might reduce its lifetime or insulation capability [40].

The presented gate driver works with any kind of power electronics switch (e.g., silicon or silicon-carbide enhancement-mode MOSFETs or IGBTs), as the creation of the low-jitter signal is decoupled from the circuitry that is directly connected to the switch and provides the appropriate control signals for it.

IV. Measurements

The functionality of the enhanced gate driver has been initially verified in [13] with promising results, but the resulting SNR improvement under continuous output load has not been measured. In order to perform these measurements, a complete Class-D power amplifier has been built (cf. **Fig. 1** and **Fig. 7**). The system features four independent half-bridges, comprising eight top-cooled *GanSystems GS66508T* E-HEMT GaN transistors and their low-jitter, isolated gate drivers. The nominal DC-link voltage is $400\,\mathrm{V}$ and the rated peak output power is $8\,\mathrm{kVA}$. The system also features nine high-precision analog to digital converters (16-bit, 1 MSa/s and 18-bit, 5 MSa/s) together with a comprehensive data processing system in order to measure and control the required voltages and currents; furthermore, EMI filters are provided at the DC input and AC output.

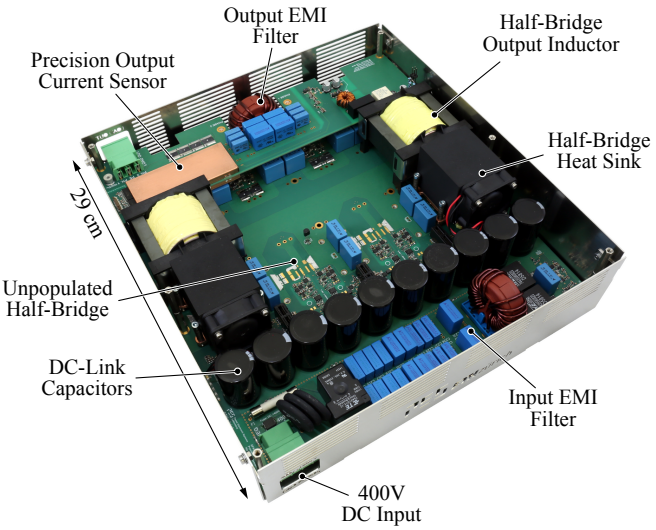

Fig. 7. Power amplifier demonstrator with the control-board removed. Two of the four half-bridges are populated, which employ top-cooled *GS66508T* GaN E-HEMT transistors. For this work, one half-bridge operates with a regular gate driver, while the other half-bridge uses the proposed low-jitter driver.

A. System Configuration

For the following analysis, two of the four available half-bridges (denoted as HB A and B) are utilized. The two gate drivers of HB A are reconfigured in such a way that the low-jitter feature is disabled; thus, they behave as regular gate driver circuits. Hereby, the blanking signal *BLK* is used to keep the gate driving IC's output permanently low during switch-node transitions, utilizing a second control input of the gate driver IC, which prevents a parasitic turn-on of the power transistor, and the jittery signal isolator output is directly routed to the gate driver IC [41]. Otherwise, the two half-bridges are operated identically. The system's configuration

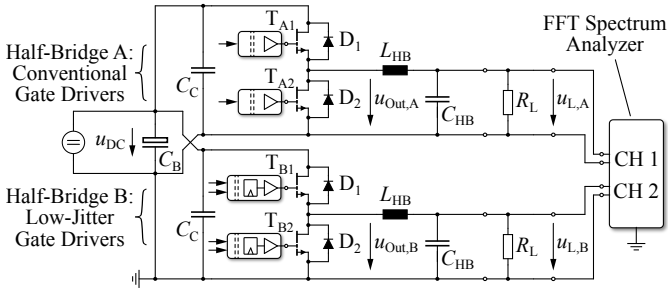

Fig. 8. Circuit configuration for the measurements. Half-bridge A features a conventional, jittery gate driver whereas the low-jitter gate driver is used in half-bridge B. A *Rohde&Schwarz UPV* high-precision FFT spectrum analyzer is used for measuring the SNR in the half-bridge output signals $u_{\mathrm{L,A}}$ and $u_{\mathrm{L,B}}$.

for the measurements is depicted in **Fig. 8**, and **Tab. I** lists important component values. The gate drivers apply a voltage of $+6\,\mathrm{V}$ between gate and source of the E-HEMT transistors in order to turn them on and a voltage of $-3.3\,\mathrm{V}$ to ensure a reliable turn-off. The digital clock frequency is set to $100\,\mathrm{MHz}$ and for the low-jitter gate drivers, the blanking delay time

$T_{\mathrm{BLK,DEL}}$ is set to 20 ns, the blanking time T_{BLK} to 30 ns and the dead time T_{D} to 70 ns.

To measure the SNR of the filtered half-bridge output voltages $u_{\mathrm{L,A}}$ and $u_{\mathrm{L,B}}$, a high-precision, two-channel spectrum analyzer (*Rohde&Schwarz UPV*) is used [42]. Furthermore, to reduce the quantization noise in the PWM signal, the optimized noise-coupled noise shaper presented in [13] is employed. This significantly reduces the quantization-induced half-bridge output noise in a band from DC to 10 kHz, rendering the noise contribution from the jittery gate signals observable. The digital PWM modulator is clocked with 100 MHz and has (configurable) counter resolutions of 9, 8 and 7 bit, which results in pulse repetition frequencies of 97.7 kHz, 195 kHz and 391 kHz [13]. As the two half-bridges are operated in an open-loop fashion (i.e., no voltages/currents are measured and no feedback is employed), a low-noise 400 V power supply is required as an open-loop switch-mode amplifier is characterized by a low power supply rejection [43], [44]. Otherwise, too much additional noise would be introduced to the half-bridge output voltages which would render the noise contributions from the gate drivers unobservable. For these experiments, a *HP 6035A* power supply is used (0-500 V, max. 5 A or 1 kW).

TABLE I
CONFIGURATION OF THE MEASUREMENT SETUP (CF. **FIG. 8**).

C_{B}	Bulk DC-Link Capacitors (Electrolytic)	1 mF
C_{C}	Half-Bridge Commutation Capacitors (Ceramic)	2 µF
L_{HB}	Half-Bridge Inductors (Ferrite, N87)	680 µH
C_{HB}	Half-Bridge Filter Capacitors (Film)	12 µF
R_{L}	Load Resistor	Variable

B. Jitter Measurements With Different Load Powers

The RMS jitter of randomly sampled periods (according to (1) and (2)) is measured directly at the switch-node voltage $u_{\mathrm{Out}}(t)$ at different converter operating conditions. For that purpose, both half-bridges are operating as independent DC/DC buck converters with a fixed duty cycle $d = 0.5$ and switching frequencies ranging from 100 kHz to 400 kHz. Consequently, $u_{\mathrm{L,x}} \approx u_{\mathrm{DC}}/2$, and R_{L} is used to define the DC load power of each half-bridge: $P_{\mathrm{HB}} = u_{\mathrm{L,x}}^2/R_{\mathrm{L}}$. **Fig. 9** illustrates a measurement of $u_{\mathrm{Out}}(t)$ of the two half-bridges at their hard-switching turn-on instant. This corroborates the necessity of a gate driver which is capable of reliably operating with high CM transient stresses across its isolation barrier.

Fig. 10 shows the rising edges of $u_{\mathrm{Out}}(t)$ of the two half-bridges after one period, measured for ≈5000-7000 periods, whereas the oscilloscope's screen persistence illustrates recurring transitions with red-shifted colors. The period durations T_i are recorded by the oscilloscope by measuring the elapsed time between two trigger instants (rising edges of $u_{\mathrm{Out}}(t)$), whereas the trigger level is set to $u_{\mathrm{DC}}/2$. The inherent jitter contribution of the oscilloscope itself is expected to be less than 5 ps [45]. This measurement reveals that the low-jitter gate driver reduces the peak-to-peak jitter by a factor of ≈14.

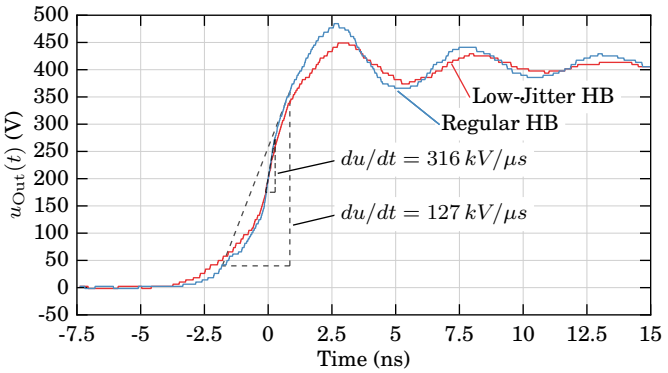

Fig. 9. Hard-switched turn-on transients of the two half-bridges recorded during steady-state operation with a switching frequency of 100 kHz. $u_{\mathrm{DC}} = 400$ V, $P_{\mathrm{HB}} = 1$ kW ($i_o = 5$ A).

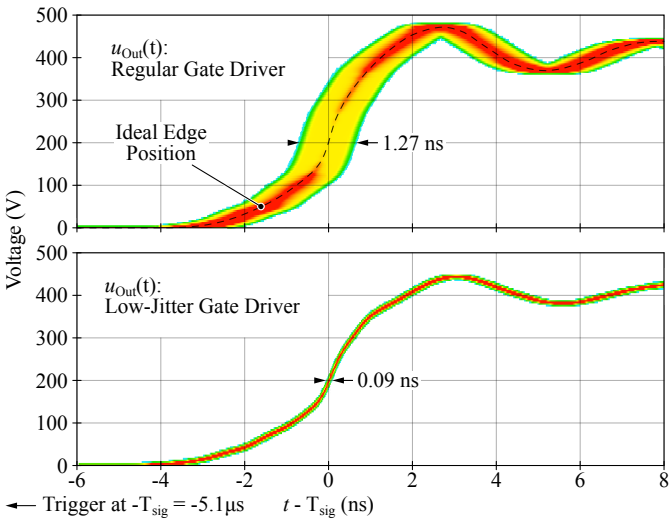

Fig. 10. Persistent oscilloscope waveforms of $u_{\mathrm{Out}}(t)$ recorded during DC/DC operation of the two half-bridges at 400 V, 195 kHz and 500 W each. The oscilloscope has a 1 GHz analog bandwidth and samples with 10 GHz (*R&S RTO1014*). Ca. 5k-7k transitions.

Additionally, each period's deviation from the ideal duration is plotted in a histogram in order to illustrate the underlying stochastic distribution, as shown in **Fig. 11** for a selection of different operating conditions of the two half-bridges. The jitter (of both half-bridges) is very independent of the converter's operating condition such as DC-link voltage, switching frequency or output load, which enables the usage of the low-jitter driver in different applications without the necessity of circuit changes. Furthermore, the distribution of the regular gate driver's jitter resembles a triangular distribution, whereas the remaining jitter of the improved driver can be approximated with a normal distribution ($\mu = 0, \sigma = 18$ ps).

Using this method, RMS jitter values of u_{Out} from both half-bridges have been recorded for different operating conditions. **Tab. II** lists the measurement results, which show the significant jitter reduction achieved by the low-jitter gate driver. Furthermore, the jitter values remain consistent over a wide range of operating conditions. The RMS jitter recorded at a switching frequency of 391 kHz is elevated (30.3 ps) compared to the other values (≈15-20 ps), which is attributed

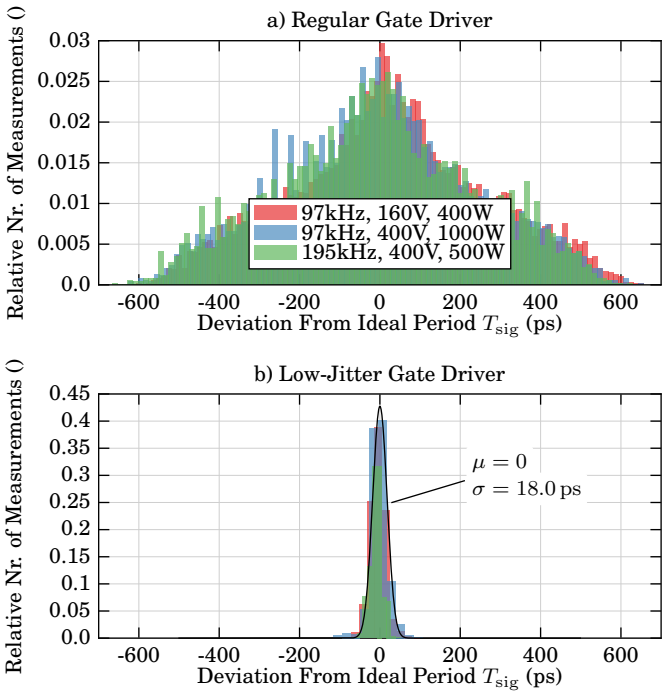

Fig. 11. Histograms of $(T_{\mathrm{sig}} - T_{\mathrm{avg}})$ of the two half-bridges operating as DC/DC buck converters with different pulse frequencies and output loads. The legend is valid for both plots. Each histogram incorporates ≈5k-7k measurements. (a): Conventional gate driver, 100 bins. (b): Low-jitter gate driver, 10 bins.

TABLE II
RMS JITTER MEASURED DURING DC/DC BUCK CONVERSION IN $u_{\mathrm{Out}}(t)$ OF THE HB WITH THE REGULAR GATE DRIVERS (HB A) AND THE LOW-JITTER DRIVERS (HB B) AT DIFFERENT OPERATING POINTS.

u_{DC} (V)	f_{PWM} (kHz)	P_{HB} (W)	$T_{\mathrm{Jit,RMS,A}}$ (ps)	$T_{\mathrm{Jit,RMS,B}}$ (ps)
160	97.7	100	235.1	18.2
160	97.7	400	236.3	17.9
160	195	400	239.2	15.1
160	391	400	235.8	30.3
400	97.7	100	230.8	19.0
400	97.7	1000	237.0	19.7
400	195	500	238.4	13.5

to thermal effects in the gate driving circuit, as its power dissipation increases and the integrated circuits (flip-flop, AND gate, gate driver IC) are introducing more jitter. Nonetheless, the low-jitter gate driver reduces the RMS jitter on average across the different measurements by a factor of ≈ 12.

In the following, the SNR of a sine-modulated half-bridge output is measured, which coincides with these static jitter measurements according to (3).

C. SNR Measurements

Similar to the previous section, the two half-bridges are operated independently as buck converters, but now, the duty cycle is modulated according to

$$d = m_{\mathrm{DC}} + m\sin(2\pi f_{\mathrm{F}} t), \tag{4}$$

which creates a sinusoidal output voltage with a DC offset. The selection of $m_{\mathrm{DC}} = 0.5$ and $m = 0.42$ leads to a minimum duty cycle of 0.08 and a maximum duty cycle of 0.92. This is done as the noise shapers have been optimized for stable operation up to $d = 0.95$, which leaves some safety margin (cf. [13]). The fundamental frequency f_{F} has been set to 33 Hz as there is no integer ratio to the 50 Hz mains frequency, whose components might be visible in spectral plots due to the open-loop operation and the non-ideal power supply. Note that the selection of the fundamental frequency does not influence the SNR, as (3) shows and measurements confirm. For the sake of brevity, all measurements are shown with $f_{\mathrm{F}} = 33$ Hz.

Again, the converter is operated at different output power levels according to

$$P_{\mathrm{HB,AVG}} = \frac{1}{T}\int_0^T \frac{u_{\mathrm{L,x}}(t)^2}{R_{\mathrm{L}}} dt, \tag{5}$$

and

$$P_{\mathrm{HB,Pk}} = \frac{(u_{\mathrm{DC}}(m_{\mathrm{DC}} + m))^2}{R_{\mathrm{L}}}, \tag{6}$$

while the reactive power resulting from the output filter capacitor C_{HB} is neglected. The *Rohde&Schwarz UPV* spectrum analyzer is directly connected to the filtered half-bridge output voltage $u_{\mathrm{L,x}}$. As this unit accepts an input voltage ≤160 V, the DC-link voltage is set to $u_{\mathrm{DC}} = 160$ V for these measurements. **Fig. 12** shows the spectra of the two half-bridges at $P_{\mathrm{HB,AVG}} = 400$ W, at a switching frequency of 195 kHz. The noise floor of the low-jitter half-bridge is significantly

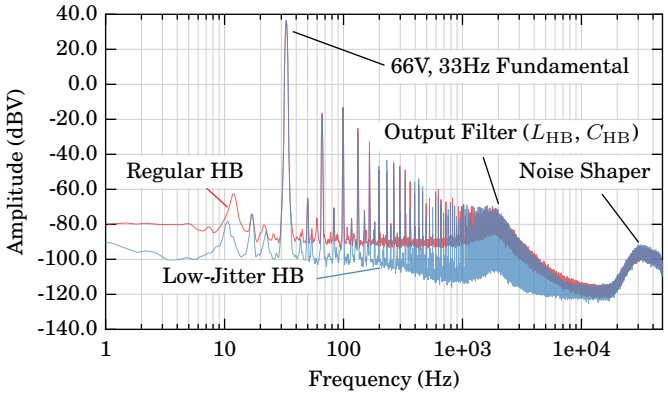

Fig. 12. Spectra (AC coupled) of the two filtered half-bridge output voltages $u_{\mathrm{L,x}}(t)$. PWM switching frequency is 195 kHz, $u_{\mathrm{DC}} = 160$ V and $P_{\mathrm{HB,AVG}} = 400$ W. The SNR of the regular HB output is 88.3 dB, whereas the low-jitter half-bridge achieves 105.9 dB.

lower. The frequency components at harmonic frequencies $f_{\mathrm{H,n}} = nf_{\mathrm{F}}$ of the fundamental are due to the dead time in the half-bridges, non-zero transistor on-state resistances and non-zero switching times, among others, as described in [12]. However, as the SNR is considered in this analysis, the harmonic spectral components are of no concern, as they are neglected when calculating the noise power [13]. The SNR is measured for different operating conditions of the converter, which **Tab. III** summarizes. As the DC power supply injects some noise and spectral spurs up to ≈300 Hz, which adds to the half-bridge output noise, the SNR is evaluated in a frequency band ranging from 300 Hz to 10 kHz. In **Fig. 12**,

this supply-related noise contribution is visible between the harmonics of the 33 Hz fundamental. It shows that the SNR values are, as expected from the static jitter measurements presented earlier, not significantly dependent on the load power.

TABLE III
SNR MEASUREMENTS FOR THE TWO HALF-BRIDGES AT DIFFERENT OPERATING CONDITIONS. $u_{\mathrm{DC}} = 160\,\mathrm{V}$. THE SNR IS EVALUATED IN A FREQUENCY BAND FROM 300 Hz TO 10 kHz.

f_{PWM} (kHz)	$P_{\mathrm{HB,AVG}}$ (W)	$P_{\mathrm{HB,Pk}}$ (W)	$\mathrm{SNR_{HB\,A}}$ (dB)	$\mathrm{SNR_{HB\,B}}$ (dB)
97.7	100	250	87.6	98.8
97.7	400	1000	89.5	99.6
195	100	250	86.1	107.1
195	400	1000	88.3	105.9
391	100	250	84.5	95.4
391	400	1000	84.9	90.5

Correspondingly, **Tab. IV** summarizes the measured RMS jitter and SNR values as averaged values (arithmetic mean) from different operating conditions in order to compare them to the theoretically best achievable SNR according to (3), with $f_{\mathrm{BW}} = 9700\,\mathrm{Hz}$ and $m = 0.84$, as this corresponds to the configuration of the SNR measurement. The measured jitter values follow the theoretical prediction accurately for the conventional gate driver with the jittery switch-node signal, despite its triangular-shaped distribution (cf. **Fig. 11**; (3) assumes a normal distribution). As the low-jitter half-bridge achieves significantly better SNR figures, it can be concluded that the SNR of the conventional half-bridge output is in fact limited by the jitter of the signal isolator. With regards to the low-jitter half-bridge, the predicted performance can be only measured with a switching frequency of $195\,\mathrm{kHz}$, as this noise shaper's configuration achieves the lowest noise, as indicated in Fig. 16 of [13]. The other two noise shaper configurations do not achieve a sufficiently low noise figure and introduce more wideband quantization noise to the output, which is added to the jitter-induced noise, thus lowering the SNR figure below the predicted value. The good coincidence of predicted and measured SNR of the low-jitter driver for $f_{\mathrm{PWM}} = 195\,\mathrm{kHz}$ indicates that the remaining jitter is the dominant source of output noise.

V. CONCLUSION

A gate driver circuit is proposed which enables very low-noise switch-mode power amplifier output signals. In mechatronic positioning systems operating with accuracies in the nanometer range, e.g., in integrated semiconductor manufacturing, such precision amplifiers face the challenging task of providing actuator currents of high signal to noise ratio (SNR$\approx$110 dB) at power levels up to several kVA. Regular gate driving methods are subject to jitter introduced to the gate control signal by the signal isolator which is required to control the high-side driver in a half-bridge switching leg. This signal jitter introduces wideband noise and lowers the achievable SNR in the DC/AC converter's output signal. RMS jitter values $>200\,\mathrm{ps}$ are common with conventional gate drivers and reduce the best achievable SNR at the converter output to levels $<90\,\mathrm{dB}$. Consequently, the proposed gate driver is capable of reducing the jitter in the gate control signal to values $<20\,\mathrm{ps}$, which increases the achievable SNR to $107\,\mathrm{dB}$, as measurements confirm. The gate driver is evaluated at various DC-link voltages up to $400\,\mathrm{V}$, PWM switching frequencies from $100\,\mathrm{kHz}$ to $400\,\mathrm{kHz}$ and output powers up to $1000\,\mathrm{W}$ (limited by the utilized supply), without observing deviations from its jitter reduction performance. The gate driver circuit is also rendered immune to fast common-mode transients across its isolation barrier, which is necessary due to the fast switching action of the GaN transistors, exceeding $300\,\mathrm{kV\,\mu s^{-1}}$ in the switched $400\,\mathrm{V}$ half-bridge output. The presented gate driver circuit is of little complexity which would allow an easy inclusion into integrated gate drivers, enabling low-noise and reliable converter operation at extremely high switching speeds, which would benefit future applications involving wide-bandgap semiconductors.

TABLE IV
AVERAGED JITTER VALUES FROM DIFFERENT CONVERTER LOADS, BEST POSSIBLE SNR ACCORDING TO (3), EVALUATED IN A BANDWIDTH FROM 300 Hz TO 10 kHz, AND THE AVERAGED MEASURED SNR, ALSO AVERAGED FROM DIFFERENT CONVERTER OPERATING POINTS.

f_{PWM} (kHz)	$T_{\mathrm{Jit,RMS,A}}$ (Averaged, ps)	$\mathrm{SNR_{Max,Calc.}}$ (dB)	$\mathrm{SNR_{Meas,HB\,A}}$ (Averaged, dB)
97.7	235.2	86.2	88.6
195	238.8	83.1	87.2
391	235.8	83.2	84.7
f_{PWM} (kHz)	$T_{\mathrm{Jit,RMS,B}}$ (Averaged, ps)	$\mathrm{SNR_{Max,Calc.}}$ (dB)	$\mathrm{SNR_{Meas,HB\,B}}$ (Averaged, dB)
97.7	18.7	108.2	99.2
195	14.3	107.6	106.5
391	30.3	101.0	93.0

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