Universal Fractional-order Design of Linear Phase Lead Compensation Multirate Repetitive Control for PWM Inverters

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***Abstract*—Repetitive control (RC) with linear phase lead compensation provides a simple but very effective control solution for any periodic signal with a known period. Multirate repetitive control (MRC) with a downsampling rate can reduce the need of memory size and computational cost, and then leads to a more feasible design of the plug-in repetitive control systems in practical applications. However, with fixed sampling rate, both MRC and its linear phase lead compensator are sensitive to the ratio of the sampling frequency to the frequency of interested periodic signals: (1) MRC might fails to exactly compensate the periodic signal in the case of a fractional ratio; (2) linear phase lead compensation might fail to enable MRC to achieve satisfactory performance in the case of a low ratio. In this paper, a universal fractional-order design of linear phase lead compensation MRC is proposed to tackle periodic signals with high accuracy, fast dynamic response, good robustness, and cost-effective implementation regardless of the frequency ratio, which offers a unified framework for housing various RC schemes in extensive engineering application. An application example of programmable AC power supply is explored to comprehensively testify the effectiveness of the proposed control scheme.**

***Index Terms*—repetitive control, DC/AC inverter, multirate repetitive control, phase lead compensation, Lagrange interpolation polynomial, programmable AC power supply**

I. Introduction

CONSTANT voltage constant frequency pulse-width modulated (PWM) voltage source inverters are widely applied as a significant element in nowadays power conversion application, e.g. uninterrupted power supply system [1], [2], grid-connected photovoltaic power source [3], [4], etc. Repetitive control, which is based on internal model principle, is an effective way to improve inverter performance with low total harmonic distortion (THD), fast transient response, and low steady state error [5]–[7].

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To reduce CPU processing load, multirate repetitive control was introduced in [8]. In MRC scheme, the converter samples with a high sampling rate, while RC processes the data with a reduced low rate. Previous work shows that MRC is able to maintain the convergence speed, tracking error and THD as good as conventional RC (CRC). Note that CRC is a special case of multirate RC with $m = 1$. Therefore, multirate RC offers a more general RC scheme in applications.

To compensate the phase lag of overall system, phase lead compensator is usually incorporated in RC scheme. Linear phase lead compensation, as a practical and efficient design method, prominently improves RC performance on convergence speed, tracking accuracy, and system stability [9], [10].

However, MRC with linear phase lead compensation usually confronts severe frequency robustness problems in practices:

1) MRC is sensitive to the ratio of the sampling frequency to the reference signal fundamental frequency. In MRC, the period delay unit $z_m^{-N_m}$ needs to provide a time delay of one reference signal period, where $z_m = z^m$ indicates MRC sampling rate is m times slower than the system sampling frequency f_s, and N_m is the ratio of the MRC sampling frequency f_s/m to the reference signal frequency f_r, i.e. $N_m = f_s/f_r/m$. In previous design [8], RC requires N_m to be an integer, which however cannot be always true in many applications. The fraction N_m can be caused by either a fractional f_s/f_r [11] (e.g. for a 60 Hz voltage reference signal under a 10 kHz MRC (m=1) sampling frequency, N_m will be 166.67) or downsampling ratio m. (e.g. for a 60 Hz voltage reference signal under a 12 kHz MRC sampling frequency, when downsampling ratio $m = 3$, N_m will be $f_s/f_r/3 = 66.67$).
2) The grid frequency is not a constant and has frequency fluctuations [12], [13]. For example, the grid frequency could vary between 59 Hz to 61 Hz. When the sampling frequency is 12 kHz, N_m of MRC (m=1) for grid-connected application will vary between 196.72 and 203.39. Inaccurate period delay will shift high gains away from the actual frequencies of interest, which will deteriorate the performance in terms of tracking accuracy and robustness.
3) Low delay periods N_m in MRC leads to a low resolution for linear phase lead compensation. The linear phase lead compensator z_m^{γ}, where γ is phase lead step, provides a phase lead $\theta = \gamma \times m \times (\omega/\omega_N) \times 180^\circ$ at frequency ω, where $\omega_N = \pi f_s$ represents the Nyquist frequency.

For RC, it is of interest to study the compensation at the fundamental frequency of the input signal $\omega_r = 2\pi f_r$ and its harmonies. Therefore, the resolution of linear compensation will be $m \times (\omega_r/\omega_N) \times 180^\circ$ at the fundamental frequency. Thus, the phase lead compensation resolution of linear phase compensator z_m^γ is $m \times (\omega_r/\omega_N) \times 180^\circ$. Obviously, large multirate m, high fundamental frequency ω_r, or low Nyquist frequency ω_N caused by low sampling frequency will lead to lower phase compensation resolution, e.g. 400 Hz on-broad AC power supplies on ship [14], low switching frequency wind power system [15]. Imprecise phase lead degrades MRC control performance or even makes the system unstable.

Addressing above issues, a finite impulse response (FIR) based fractional delay is proposed for CRC [16], parallel structure RC [11], and selective harmonic RC [17], which enables frequency adaptation to the reference signal variations. Lagrange-interpolation-based fractional delay based RC is applied in various applications, for instance, programmable AC power source [18], grid-connected power converter [13], and shunt active power filters [19]. And the scheme of Lagrange interpolation-based fractional delay is further improved with the Farrow structure to decrease computation load in [7]. However, being a general RC design, MRC still faces the frequency robustness issues of low phase compensation resolution and fractional sampling interval. Generally speaking, frequency adaptive phase lead compensation MRC is still needed to offer a universal RC design in practical applications.

To provide a comprehensive solution to above problems, a universal fractional-order design of linear phase lead compensation MRC is proposed in this paper. In the proposed universal design, both MRC delay period N_m and phase lead step γ are fractional. The proposed universal fractional-order RC, which includes a fractional-order MRC and a fractional-order linear phase compensation, provides a general frequency adaptive RC solution. It is able to achieve accurate phase lead compensation, consume less computation, and allow flexible sampling frequency and time varying reference frequency. Comprehensive analysis and synthesis method for the proposed control system are given. Experimental verification of the proposed control scheme on a programmable AC power supply is carried out to demonstrate the effectiveness of the proposed solution under various application scenarios.

The rest of this paper is organized as follows: Section II introduces MRC and its linear phase lead compensation; Section III provides the fractional-order design for linear phase lead compensation MRC in details. Section IV presents experimental results of the proposed fractional-order linear phase compensation MRC with scenarios of frequency fluctuations (reference frequency varies at 59 Hz, 60 Hz, and 61 Hz) and shipboard high frequency reference signal (400 Hz). The conclusion is summarized in the Section V.

II. Linear phase lead compensation MRC

A. MRC

MRC is able to reduce computation and keep the system with a high sampling frequency [8]. For multirate RC, the converter system has sampling time of T_s and MRC processes the data with a sampling time of T_m, which is m times of T_s. Then, we denote:

$$T_m = mT_s; z_m = e^{sT_m} = e^{msT} = z^m. \tag{1}$$

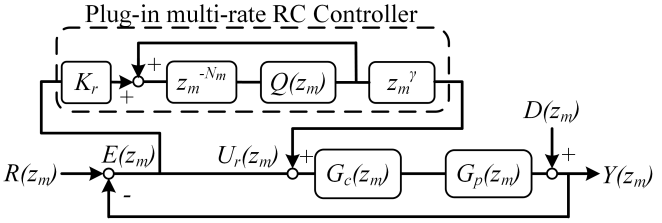

Fig. 1. Equivalent single sampling rate RC

To analyse the system with two different sampling rates, MRC is presented by an equivalent plug-in RC structure [20] shown in Fig. 1, through transforming the entire system with the same sampling rate f_s/m, where $R(z_m)$ is the reference input, $G_c(z_m)$ is the conventional controller, $G_p(z_m)$ is the plant model, $D(z_m)$ is the disturbance, $Y(z_m)$ is the system output. Plug-in MRC controller is a feed-forward controller consisting of MRC gain K_r, robustness filter $Q(z_m)$, stability filter $G_f(z_m)$, and period delay $z_m^{-N_m}$ in which N_m equals to the ratio of MRC sampling frequency f_s/m to the fundamental frequency f_r of reference signal $R(z_m)$, i.e. $N_m = f_s/f_r/m$. Note that due to factor of m, N_m is more likely to be a fraction.

The MRC transfer function G_{MRC} in Fig. 1 is:

$$G_{MRC}(z_m) = \frac{U_r(z_m)}{E(z_m)} = K_r \frac{z_m^{-N_m} Q(z_m)}{1 - z_m^{-N_m} Q(z_m)} G_f(z_m) \tag{2}$$

where $E(z_m) = R(z_m) - Y(z_m)$ is the system tracking error. Note that when $m = 1$, the MRC reduces to a conventional RC. It is worth mentioning that m can be an integer or a fraction. When m is a fraction, the signal is up-sampled first and then down-sampled to get a fractional ratio. For simple analysis, we only consider m as an integer in this paper and the results we obtained can be applied for fractional m. Note also that, theoretically, the system can be upsampled by setting $m < 1$, so more sampling points will be obtained in RC. However, it is neither efficient nor cost-effective in real applications because the requirement of computation time and resources will increase. Therefore, only downsampling MRC approach with $m \geqslant 1$ is investigated in our study.

In the frequency domain, MRC transfer function in Eq. (2) has infinity magnitude gain at the fundamental and all harmonic frequencies of the reference signal when $Q(z_m) = 1$. Therefore, MRC can achieve zero steady-state error tracking of periodic signals. Previous work shows that MRC is able to maintain the convergence speed and THD as good as conventional RC does [8]. It is clear that CRC is a special case of MRC when $m = 1$. Thus, MRC is a more flexible RC design approach.

When the ratio $N_m = f_s/f_r/m$ is not an integer, conventional MRC design chooses the closest integer $\lfloor N_m \rceil$. The delay error in a period ΔN_m is defined as $\Delta N_m = \lfloor N_m \rceil - N_m$.

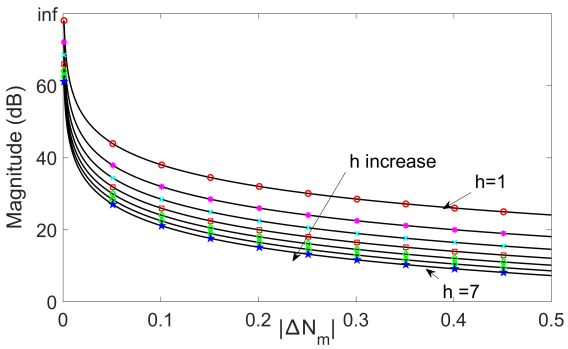

Fig. 2. Sensitivity of MRC magnitude plot to delay period error

Using Euler's identity, the magnitude response of MRC at harmonics frequencies $\omega = 2\pi h f_r$, with h being the harmonic order, can be obtain as:

$$|G_{MRC}(z_m)| = \left| K_r \frac{z_m^{-\lfloor N_m \rceil} Q(z_m)}{1 - z_m^{-\lfloor N_m \rceil} Q(z_m)} \right| \xrightarrow[z_m = e^{-j\omega T_m}]{|Q(z_m)|=1} \frac{K_r}{\sqrt{2 - 2cos[2\pi h(1 + f_r \Delta N_m)]}} \tag{3}$$

where phase lead compensation $G_f(z_m)$ has been ignored because of unit magnitude for linear phase lead compensation. To study the sensitivity and robustness of MRC to delay error ΔN_m, Fig. 2 shows the magnitude plot at reference fundamental and harmonic frequencies when ΔN_m changes from 0 to 0.5, where 0.5 is the maximum delay error ΔN_m. It illustrates that inaccurate delay period in MRC will result in delay error and cause remarkable gain drop. As a result, the capability of MRC in tracking reference signal or rejecting disturbance signal is significantly degraded. Obviously, this analysis shows that conventional MRC design [8] is sensitive and not robust to delay error, which can be caused by f_s/f_r itself [7], downsampling ratio m, and reference frequency fluctuation. This puts a great challenge to conventional MRC with a fixed time delay period $\lfloor N_m \rceil$.

B. Linear Phase Lead Compensation for MRC

The phase lead compensator $G_f(z_m)$ in Fig. 1 improves the system stability by providing phase lead to cancel out the phase lag of the closed-loop system $G(z_m)$ [21]. Theoretically, it can be implemented as the inverse of the system model $G(z_m)$ [22]. In practice, it is difficult to obtain the inverse of the closed-loop system accurately due to various model uncertainties.

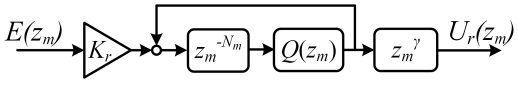

Fig. 3. Linear phase lead compensation for MRC

A simple and flexible phase lead compensation scheme is linear phase compensation design given by z_m^{γ}. Fig. 3 presents the MRC scheme with a typical linear phase lead compensation [23]. By adding a leading filter z_m^{γ}, it produces a phase lead $\theta = \gamma \times m \times (\omega/\omega_N) \times 180^\circ$ at frequency ω for the RC output. In previous design, γ is an integer, which could lead to an inaccurate phase compensation and result in performance degradation. It is desirable to develop an accurate linear phase lead compensation for MRC.

III. Fractional-order Design of Linear Phase Lead Compensation MRC

As integral-order phase lead compensation MRC is low-resolution and sensitive to both reference frequency variation and the ratio of the sampling frequency to the reference signal fundamental frequency, fractional-order design of linear phase lead compensation MRC is introduced in detail to solve the issue in this section.

A. Fractional-order Multirate RC

When sampling frequency f_s is not an integral multiple of $f_r \times m$, typical MRC is often designed based on an integral that is the closest integral to N_m. This will result in a severe performance degradation for tracking of periodic reference signal or rejecting of period disturbance signal [18], [19]. Therefore, it is necessary to design MRC with exact N_m.

This paper proposes a fractional-order multirate RC (FOMRC) scheme as shown in Fig. 4, in which $z_m^{-N_m}$ in Figs. 1 and 3 is realized by the integral part $z_m^{-N_i}$ and an approximation of fractional part. The new scheme is a universal solution as it also includes a fractional order phase lead compensation to provide accurate phase compensation, which will be discussed in the following part.

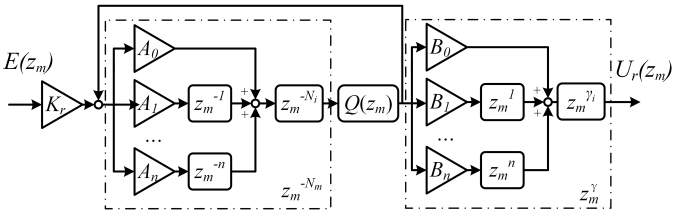

Fig. 4. Structure of the fractional-order MRC (FOMRC) with fractional-order phase lead (FOPL) compensation

In Fig. 4, a nth-order polynomial is designed to approximate the fractional delay $z_m^{-N_m}$ for MRC:

$$z_m^{-N_m} \approx z_m^{-Ni} \times \sum_{k=0}^{n} A_k z_m^{-k} \tag{4}$$

where N_i is the closest integer of $(N_m - n/2)$, and the fractional part of N_m is approximated by $\sum_{k=0}^{n} A_k z_m^{-k}$.

B. Fractional-order Linear Phase Lead Compensation

For accurate phase compensation, a fractional order phase lead (FOPL) compensation $G_f(z_m) = z_m^{\gamma}$ is proposed, where $\gamma \in \mathbb{R}^+$ is designed as a real number, as shown in Fig. 4. The FOPL can be approximated by a nth-order polynomial:

$$z_m^{\gamma} \approx z_m^{\gamma_i} + \sum_{k=0}^{n} B_k z_m^{k} \tag{5}$$

where γ_i is the nearest integer of $(\gamma - n/2)$.

With Eq. (5), the FOPL filter produces a linear phase lead:

$$\theta_f = \gamma \times m\frac{\omega_r}{\omega_N}180^\circ \tag{6}$$

for input signal frequency ω_r, where γ is a real number. Therefore, the FOPL filter can produce higher compensation resolution and accuracy than integral-order filter.

C. Fraction-order Approximation

The fractional approximation item $\sum_{k=0}^{n} A_k z_m^k$ in (4) and (5) is achieved by Lagrange interpolation polynomial. The Lagrange coefficients A_k can be calculated as:

$$A_k = \prod_{i=0, i\neq k}^{n} \frac{\gamma - i}{k - i}. \tag{7}$$

Higher order approximation can provide higher accuracy in magnitude. However, higher order approximation needs more computation and a more complicated design. With the tradeoff of approximation accuracy and design complexity, a $3rd$-order FOPL is often selected in practical applications.

D. Stability of FOMRC with FOPL

For MRC system shown in Fig. 1, $z_m^{-N_m}$ approaches 1 at f_r and its harmonics. With the assumption that $Q(z_m) = 1$, the tracking error is:

$$\lim_{\omega \to \omega_h} |E(z_m)| = 0 \tag{8}$$

where ω_h is the reference signal harmonic frequency.

The overall system holds the stability conditions: first, the closed-loop system $G(z_m) = G_c(z_m)G_s(z_m)/[1 + G_c(z_m)G_s(z_m)]$ is stable [24]; second, the following condition holds:

$$| Q(z_m)(1 - K_r G_f(z_m)G(z_m)) | < 1 \tag{9}$$

With the fractional-order linear phase lead filter $G_f(z_m)$, Eq. (9) can be rewritten as:

$$| 1 - K_r z_m^{\gamma} G(z_m) | < \frac{1}{\|Q(z_m)\|} \tag{10}$$

Substitute $z_m = e^{j\omega T_m}$, where T_m is MRC sampling time, the equivalent closed-loop transfer function can be expressed as $G(e^{j\omega T_m}) = N_g(e^{j\omega T_m})exp(j\theta_g(e^{j\omega T_m}))$, with $N_g(e^{j\omega T_m})$ and $\theta_g(e^{j\omega T_m})$ being its magnitude and phase characteristics. The robustness filter $Q(z_m)$, with the form as $Q(z_m) = az_m + (1 - 2a) + az_m^{-1}$, can be expressed as $Q(e^{j\omega T_m}) = N_q(e^{j\omega T_m})$, with $N_q(e^{j\omega T_m})$ being its magnitude characteristics. Note that $Q(z_m)$ is a zero phase low pass filter, so its phase characteristic is always 0. Then (10) becomes:

$$| 1 - K_r N_g(e^{j\omega T_m}) e^{j[\theta_g(e^{j\omega}) + \gamma\omega]T_m)} | < \frac{1}{N_q(e^{j\omega T_m})} \tag{11}$$

Since K_r and $N_g(e^{j\omega T_m})$ are both positive, we can get:

$$\begin{aligned} 0 < K_r < & \frac{1 - N_q^2(e^{j\omega T_m})}{N_q^2(e^{j\omega T_m})(K_r N_g^2(e^{j\omega T_m}))} \\ & + \frac{2cos[(\theta_g(e^{j\omega T_m}) + \gamma\omega)T_m]}{N_g(e^{j\omega T_m})} \end{aligned} \tag{12}$$

The first item on the right-hand side of (12) is a non-negative value because $0 \leq N_q(e^{j\omega}) \leq 1$. Then, (12) will be satisfied if the following condition holds:

$$0 < K_r \leq \frac{2cos[(\theta_g(e^{j\omega}) + \gamma\omega)T_m]}{N_g(e^{j\omega})} \tag{13}$$

From (13), the frequency bandwidth condition can be obtained as:

$$| \theta_g(e^{j\omega}) + \gamma\omega | < 90^\circ - \varepsilon \tag{14}$$

where ε is a small positive constant to enhance the system robustness.

The advantage of the design is that it decouples the gain K_r and phase lead γ in (10) such that they can be designed separately. In practice, since the processing unit and circuit will introduce un-modeled delays in the system, the selection of γ could be different from the one given by Eq. (14) based on the theoretical model.

IV. Application Example: Single-phase Programmable AC Power supply

Programmable AC power sources that provide adjustable frequency and adjustable amplitude AC voltages are widely used in automatic testing and bench-top applications, such as avionics testing, International Electrotechnical Commission (IEC) testing, shipboard testing, and power supply test applications. Both output amplitude and output frequency can be set over a large range. For example, electrical utilities require power supply with frequency of 50 Hz and 60 Hz while ship and aircraft requires power supply with 400 Hz. Under various load conditions, a high-performance programmable AC power source needs to generate very clean sinusoidal output voltage. In addition to the state-of-the-art high-frequency PWM technology, advanced control techniques should be employed to enable power converters to achieve these targets.

In this section, the system modeling and state feedback controller are built first, then two scenarios are used to test the advantage of the proposed fractional-order design of linear phase lead compensation MRC:

1) 110V output with frequency variation from 59 Hz to 61 Hz under MRC (m=4), and
2) 110V, 400Hz output under MRC (m=1). Both of them have sampling frequency of 11 kHz.

A. System Modeling and State Feedback Controller

Fig. 5 shows a MRC controlled single-phase DC/AC inverter, where E_n is the DC bus voltage; L and C are inductor-capacitor filter; R is the linear load; C_r, L_r, and R_r are capacitor, inductor, and resistor in the rectifier load, respectively. The output voltage V_{out} and inductor current I_L are two states for state feedback controller; V_{in} is the input PWM voltage.

The experimental testbed consists of the state feedback controller and plug-in universal fractional-order MRC controller designed in Matlab Simulink and implemented by dSPACE DC1103 board to control the H-bridge IGBT converter. The output voltage and current waveform are recorded

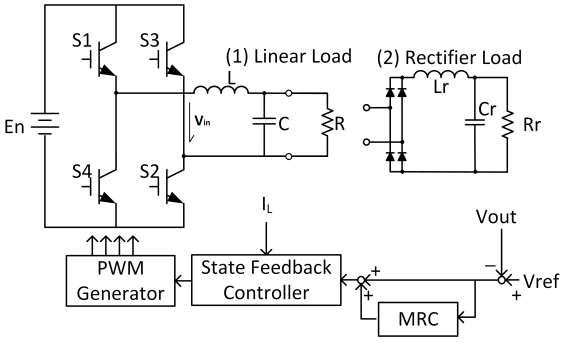

Fig. 5. Plug-in MRC controlled inverter system

via sampling circuit by ControlDesk for real-time control and performance analysis.

With the MRC sampling rate of f_s/m, the discrete-time state space of the single-phase inverter system in Fig. 5 can be written as:

$$\begin{bmatrix} v(k+1) \\ i(k+1) \end{bmatrix} = \begin{pmatrix} \varphi_{11} & \varphi_{12} \\ \varphi_{21} & \varphi_{22} \end{pmatrix} \begin{bmatrix} v(k) \\ i(k) \end{bmatrix} + \begin{pmatrix} g_1 \\ g_2 \end{pmatrix} u(k) \qquad (15)$$

where $\varphi_{11} = 1 - T_m/(RC) + T_m^2/(2R^2C^2) - T_m^2/(2LC)$, $\varphi_{12} = T_m/C - T_m^2/(2RC^2)$, $\varphi_{21} = -T_m/L + T_m^2/(2RLC)$, $\varphi_{22} = 1 - T_m^2/(2LC)$, $g_1 = E_n T_m^2/(2LC)$, $g_2 = E_n T_m/L$.

The state feedback controller has the form as:

$$u = -k_1 v(k) - k_2 i(k) + g v_{ref}(k) \qquad (16)$$

where k_1, k_2 and g are controller parameters, v_{ref} is the reference sinusoidal voltage. With the state feedback controller (16), the transfer function can be rewritten as:

$$G(z) = \frac{m_1 z + m_2}{z^2 + p_1 z + p_2} \qquad (17)$$

where $p_1 = -(\varphi_{22} - g_2 k_2) - (\varphi_{11} - g_1 k_1)$, $p_2 = (\varphi_{11} - g_1 k_1)(\varphi_{22} - g_2 k_2) - (\varphi_{12} - g_1 k_2)(\varphi_{21} - g_2 k_1)$, $m_1 = g_1 k$, $m_2 = g_2 k - g_1 k(\varphi_{22} - g_2 k_2)$.

TABLE I
SYSTEM PARAMETERS

Parameter	Value	Parameter	Value
DC voltage, E_n	200 V	Inductor, L	3 mH
Capacitor, C	10 μF	PWM frequency	11 kHz
Sampling frequency, f_s	11 kHz	Linear load, R	200 Ω
Rectifier capacitor C_r	60 μF	Rectifier inductor L_r	3 mH
Rectifier resistance R_r	200 Ω		

B. Experimental scenario I: 110V output with variable frequency 59 Hz, 60 Hz, and 61 Hz

With parameters in Table I and state feedback control gain $k_1 = 1.5$, $k_2 = 7$, and $g = 0.5$, the closed loop transfer function $G(z_m)$ can be derived as:

$$G(z_m) = \frac{1.396 z_m + 0.899}{z_m^2 + 0.9915 z_m + 0.3569} \qquad (18)$$

The feedback control system is stable with the poles at $-0.4957 \pm 0.3334i$ in the unit cycle. With this feedback

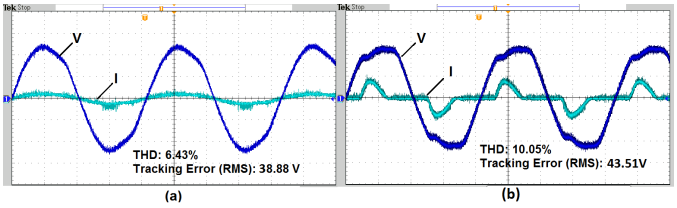

Fig. 6. Output performance under feedback control: (a) linear load, (b) rectifier load

controller, the system response under two kinds of loads for 60 Hz 110V voltage is shown in Fig. 6. From the results, state feedback presents the stable response, but serious magnitude error, phase lag and voltage waveform distortion result in the large tracking error, which are 38.88V and 43.51V, and poor THD performance, which are 6.43% and 10.05%.

The experiment employs a MRC controller with down-sampling ratio $m = 4$, which reduces RC sampling frequency to 1/4 of CRC. For 60 Hz reference frequency, the ratio of the MRC sampling frequency and reference frequency f_r equals to $f_s/f_r/m = 45.83$ which is not an integer. Therefore, the delay period $\lfloor N_m \rceil$ for integral MRC is chosen as the closest integer 46, while the N_m in FOMRC is chosen as 45.83, which is approximated by a $3rd$-order FIR filter as:

$$z_m^{-45.83} \approx -0.02 z_m^{-44} + 0.18 z_m^{-45} + 0.89 z_m^{-46} - 0.04 z_m^{-47}. \qquad (19)$$

For the other two reference frequency cases, the similar designs for delay period N_m are applied: $N_m = 46.61$ for 59 Hz and $N_m = 45.08$ for 61 Hz.

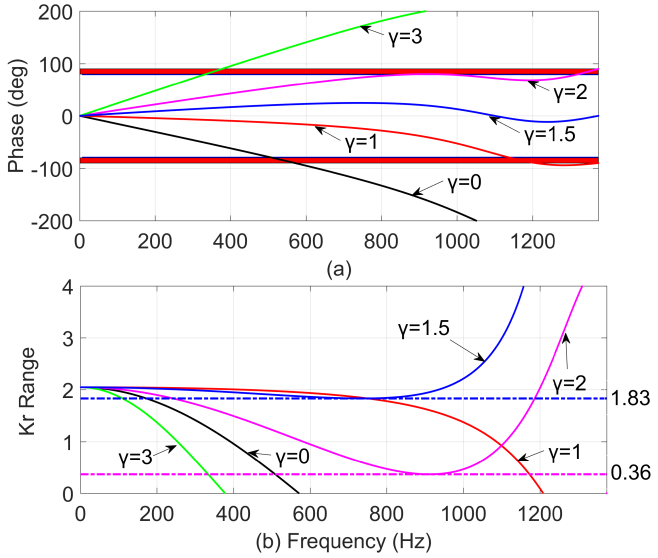

Fig. 7. Phase lead compensation comparison: (a) frequency bandwidth (b) K_r upper limit

Fig.7 (a) and (b) show the phase lead compensation bandwidth and K_r in the range of the Nyquist frequency with different phase lead steps of γ. Based on condition (14), the phase after compensation should stay within $\pm 75°$ with $\varepsilon = 15°$. Condition (13) indicates that the upper limit of the gain K_r must be positive but smaller than the minimum value of the

curve $2cos[(\theta_g(e^{j\omega_m})+\gamma\omega_m)T_m]/N_g(e^{j\omega_m})$. Fig.7 (a) shows that in the cases of no phase lead ($\gamma = 0, 1$) and excessive phase lead ($\gamma = 3$), the phase lead compensation results in limited controllable bandwidth of about 550 Hz, 1200 Hz, and 350 Hz respectively. Although the phase lead compensation with $\gamma = 2$ stays in stable area, it already reaches the limited stability area at high frequency. On the contrary, the phase lead compensation with $\gamma = 1.5$ stays in $\pm 75°$ below the Nyquist frequency, which means it can guarantee zero error tracking of periodic signals. From Fig. 7 (b), the gain K_r of the fractional-order compensator with $\gamma = 1.5$ has an upper limit of 1.83 below the Nyquist frequency, compared with 0.36 for $\gamma = 2$. For $\gamma = 0$, 1 and 3, it is not possible to hold K_r positive for the whole Nyquist frequency. This result shows that fractional-order phase compensation leads to a larger stable frequency bandwidth and a larger gain K_r upper-limit.

As mentioned early, the practical γ could be different from the theoretical value. By carrying out experiments with different phase leads, the best result for integral phase lead can be obtained when $\gamma = 2$; for FOPL, the best performance happens when setting $\gamma = 1.7$. This is different from the theoretical analysis and is mainly caused by the system modeling uncertainty and delay in the DSP controlled PWM [25], [26].

The MRC gain K_r for both integral phase lead and FOPL are 1, which is within K_r upper limit for both systems. Based on Eq. (5) and (7) the FOPL with $\gamma = 1.7$ has the form of:

$$z_m^{1.7} \approx -0.05z_m^1 + 0.33z_m^2 + 0.77z_m^3 - 0.06z_m^4 \qquad (20)$$

Experiments are compared under three MRC design methods: MRC with integral-order phase lead, FOMRC with integral phase lead, and FOMRC with FOPL.

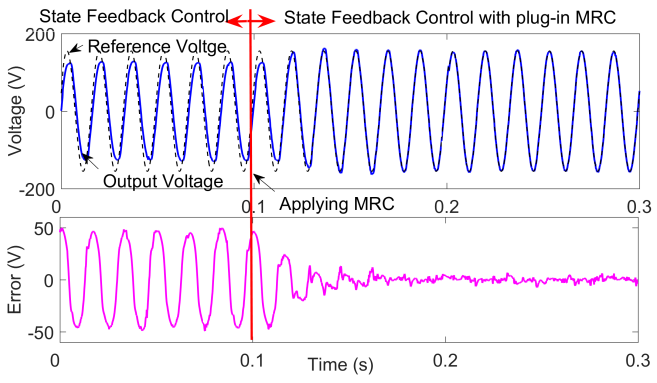

Fig. 8. Transient response of FOMRC with FOPL

Fig. 8 shows the transient response and tracking error after applying FOMRC with FOPL for 60Hz reference frequency. When system operates under state feedback control, the peak tracking error is about 50 V and this is mainly caused by the response phase lag and magnitude error. After applying FOMRC with FOPL, the system tracking error converges and becomes stable within about 4 cycles.

Fig. 9 shows the steady-state performance comparison between MRC, FOMRC, and FOMRC with FOPL for 60 Hz reference under linear load and rectifier load. It is clear that FOMRC with FOPL has the best waveform performance. Similar comparison results can be obtained for reference signals with 59 Hz and 61 Hz, in which MRC and FOMRC show even worse waveform performance. To further demonstrate the performance of FOMRC with FOPL, Fig. 10 shows the waveforms for 59 Hz, 60 Hz, and 61 Hz under Linear and rectifier load, respectively. It shows that FOMRC with FOPL has very good performance under different frequencies.

The tracking accuracy of PWM inverters is normally evaluated in two important aspects: (1) THD concerning how "sinusoidal" the output is (in term of power quality); (2) tracking error concerning the absolute control accuracy. Table II shows the variable input frequency steady-state performance comparison between the three MRC methods, where LL, NL, and RL means the load conditions of linear load, no load, and rectifier load, respectively. The steady state performance is mainly considered in tracking error root mean square (RMS) value and THD. For 59 Hz reference input, FOMRC gives an obvious improvement when it is compared against the integral-order MRC. This is mainly caused by the accurate delay period in FOMRC. FOPL gives a further improvement by achieving more accurate compensation. The FOMRC with FOPL achieves 31.4%, 28.1%,and 41.5% improvement on tracking error and 15.2%, 28.1%, and 40.4% on THD comparing with FOMRC without FOPL for linear, no, and rectifier loads, respectively.

For 60 Hz and 61 Hz reference input, similar results are obtained. For general cases (beyond PWM converters), the assessment of the tracking accuracy of a control system only concerns the tracking error. That means the proposed method offers a general control solution to extensive applications (including power converters).

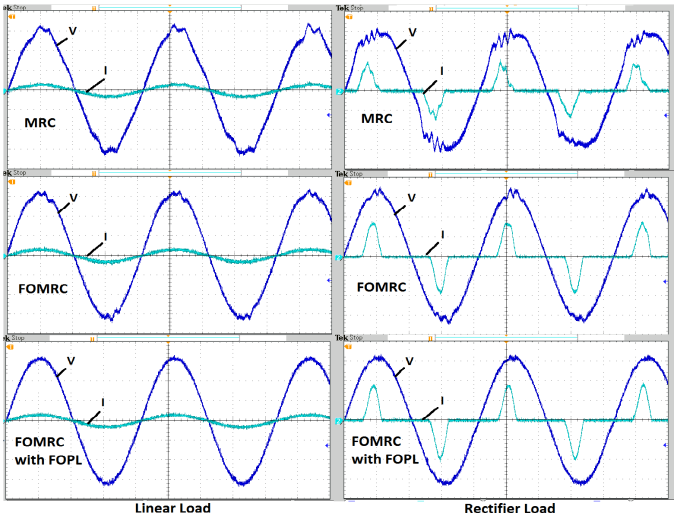

Fig. 9. Steady-state performance comparison between MRC, FOMRC and FOMRC with FOPL for 60 Hz reference voltage

From Fig. 9, Fig. 10, and Table II, it is easy to draw the conclusion that the proposed FOMRC with FOPL design is insensitive to the ratio of f_s/f_r and is able to deal with fractional order delay unit. More importantly, the proposed design is able to efficiently deal with the varying reference frequency or frequency fluctuation and thus increases the robustness of the repetitive control design.

TABLE II
STEADY-STATE PERFORMANCE COMPARISON OF MRC CONVERTERS AT DIFFERENT FREQUENCIES

	59 Hz reference input						60 Hz reference input						61 Hz reference input					
	Tracking Error (V)			THD(%)			Tracking Error (V)			THD(%)			Tracking Error (V)			THD(%)		
	LL	NL	RL	LL	NL	RL	LL	NL	RL	LL	NL	RL	LL	NL	RL	LL	NL	RL
MRC	6.12	4.60	9.17	3.84	2.44	6.59	7.59	5.72	11.2	3.92	2.76	8.25	9.31	7.11	13.4	4.31	2.82	9.70
FOMRC	2.13	1.17	2.99	1.05	0.64	1.78	1.71	1.11	1.91	0.91	0.66	1.26	1.94	1.01	2.22	0.98	0.62	1.28
FOMRC with FOPL	1.46	0.82	1.75	0.89	0.46	1.06	1.10	1.00	1.39	0.62	0.41	0.92	1.37	1.00	1.29	0.70	0.57	0.75

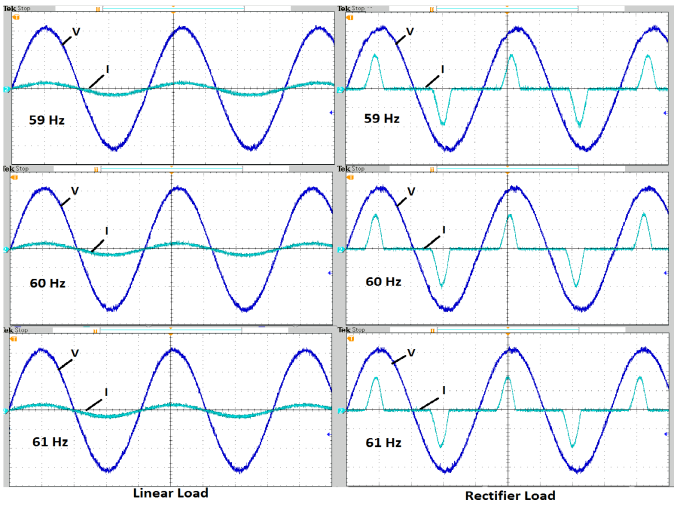

Fig. 10. Steady-state voltage response of FOMRC with FOPL for 59 Hz, 60 Hz, and 61 Hz reference voltage under linear load and rectifier load

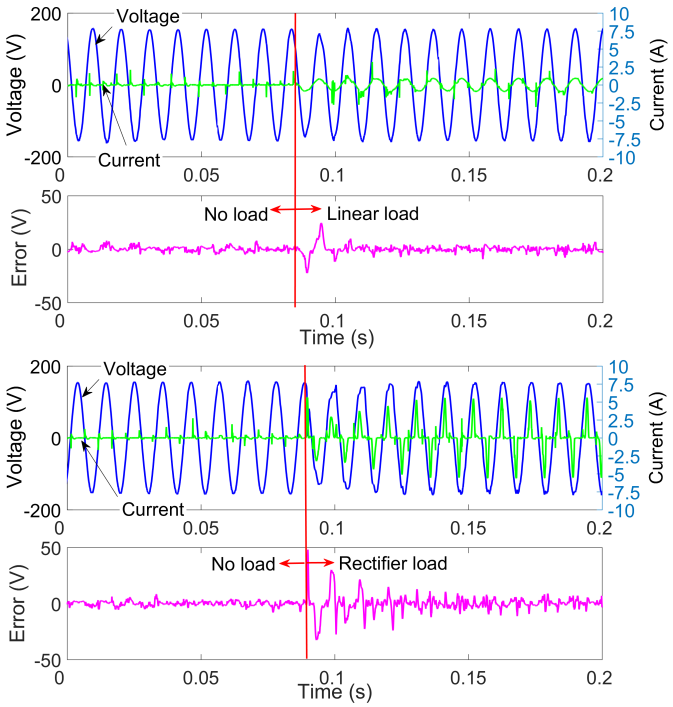

Fig. 11. Sudden load switch of 60Hz reference voltage: (a) from no load to linear load, (b) from no load to rectifier load

Fig. 11 shows the transient response of the universal fractional-order design of MRC at 60Hz operates under sudden load switches from (a) no load to linear load and (b) from no load to rectifier load, respectively. From the response, the output voltage recovers from sudden step load change within 2 cycles (0.033 second) when a linear load is switched on, and recovers within 5 cycles (0.083 second) when a rectifier load is switched on. The experiments demonstrate that the proposed universal fractional-order design of MRC is robust to sudden load changes.

C. Experimental scenario 2: 110V, 400Hz output

The high frequency power supply can reduce equipment volume and weight, which is significant for aircraft and ship. Therefore, 110 VAC at 400 Hz is much popular used in aircraft and ship AC power supply. However, with the same sampling frequency f_s = 11 kHz, high reference frequency f_r leads to a small delay period $N = f_s/f_r$ in RC, which may result in a fractional ratio and a low phase lead compensation resolution. With a small N, we do not downsample the signal, i.e. $m = 1$, thus we drop the subscript m. However, we still use FOMRC to make the notation consistent.

The state feedback control gain is chosen as $k_1 = 1$, $k_2 = 7$, and $g = 0.5$ for 400 Hz system, the closed-loop transfer function $G(z)$ based on Eq. (17) is derived as:

$$G(z) = \frac{0.1223z + 0.1121}{z^2 - 1.413z + 0.7729} \tag{21}$$

The poles of the system are $0.7065 \pm 0.5232i$, which are within the unit circle. Under only feedback controller, it gives stable responses for different loads. However, it cannot present a satisfactory performance in both tracking error and THD. The THDs for no load, linear load, and rectifier load are all larger than 10%.

As the ratio of f_s/f_r is a fraction in this case study, FOMRC with $N = 27.5$ and CRC with $\lfloor N \rceil = 28$ are used; the RC gain K_r for both integral phase lead and FOPL are also set as 0.5, which is within K_r upper limit for both systems. With the similar experiment process, the best result for integral phase lead can be obtained as $\gamma = 3$; for FOPL, the best result is achieved when $\gamma = 3.5$ which can be approximated as:

$$z^{3.5} \approx -0.06z^2 + 0.56z^3 + 0.56z^4 - 0.06z^5. \tag{22}$$

Experiments are carried out under three kinds of loads by comparing three RC design methods: CRC with integral-order phase lead ($N = 28, \gamma = 3$), FOMRC with integral-order phase lead ($N = 27.5, \gamma = 3$), and FOMRC with FOPL ($N = 27.5, \gamma = 3.5$).

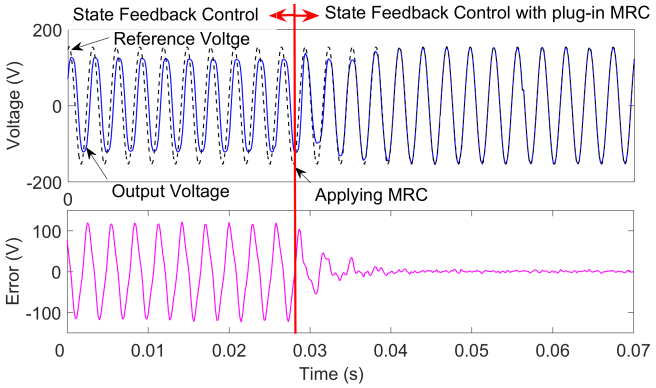

Fig. 12. Transient response after applying FORC with FOPL

Fig. 12 shows the transient response and tracking error after applying RC with FOPL. It shows that the system tracking error converges and becomes stable within about 3 cycles.

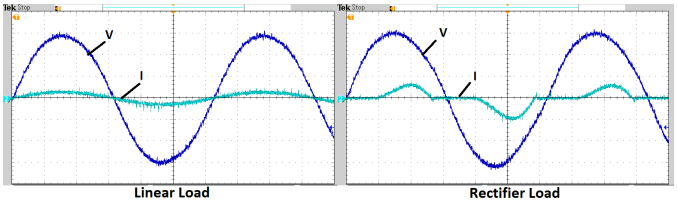

Fig. 13. 400 Hz RC system steady-state voltage response of FORC ($N = 27.5$) with FOPL ($\gamma = 3.5$) under linear load and rectifier load

TABLE III
STEADY-STATE PERFORMANCE COMPARISON AT 400 HZ

	N	γ	Tracking Error (V)			THD (%)		
			LL	NL	RL	LL	NL	RL
CRC	28	3	61.29	-	-	6.53	-	-
FOMRC (m=1)	27.5	3	1.63	2.35	3.99	0.85	1.81	3.38
FOMRC (m=1) with FOPL	27.5	3.5	1.54	1.90	3.84	0.81	1.10	2.85

Fig. 13 shows the waveforms of FOMRC with FOPL under linear and rectifier load, respectively. It is clear that the output voltage traces the reference accurately under different load conditions, which presents a strong robustness of FOPL compensation. Table III summaries the steady state performance comparison among RC methods ('-' means unstable). Comparing between CRC and FOMRC, an accurate delay period is achieved in FOMRC. On the contrary, the CRC cannot even maintain a stable output under no load and rectifier load conditions. Comparing with integral-order phase lead compensation, FOPL achieves more accurate compensation which results in smaller tracking error and lower THD. Comparing with FOMRC without FOPL, FOMRC with FOPL achieves 5.5%, 19.1%, and 37.6% improvement on tracking error and 4.7%, 39.2%, and 15.7% on THD for linear, no, and rectifier loads, respectively. Fig. 12, Fig. 13, and Table III show that the proposed FOMRC with FOPL has excellent capability to deal with applications with low delay periods and overcomes its limitation on inaccurate phase compensation.

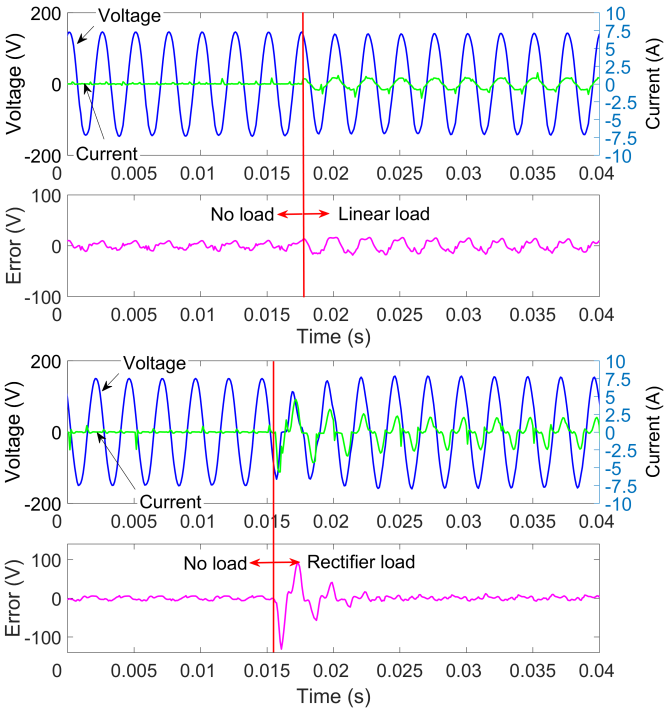

Fig. 14. Sudden load switch of 400Hz reference voltage: (a) from no load to linear load, (b) from no load to rectifier load

Fig. 14 shows the transient response of the universal fractional-order design of MRC at 400Hz operates under sudden load switches from (a) no load to linear load and (b) from no load to rectifier load, respectively. From the response, the output voltage recovers from sudden step load change in 1 cycle (2.5 ms) when linear load is switched on, and recovers within 3 cycles (7.5 ms) when rectifier load is switched on.

V. CONCLUSION

In this paper, a universal fractional-order design of linear phase lead multirate repetitive control is proposed to provide a general frequency adaptive RC design. The proposed approach is simple and effective in the applications where sampling frequency f_s, the fundamental frequency of the reference signal f_r, and downsampling ratio m can be flexibly selected. Theoretical analysis and experiments show that this new FOMRC with FOPL design leads to significant performance improvement in applications where the unit delays in a period of the reference signal (ratio of $f_s/f_r/m$) is not an integer, the fundamental reference frequency f_r has fluctuations, and the phase compensation resolution is low. It is noted that conventional RC is a special case of MRC and therefore the proposed design can be used for conventional RC. The effectiveness of the proposed FOMRC with FOPL is verified on a series of application examples of programmable AC power supplies with high tracking accuracy, low THD, and good transient response.

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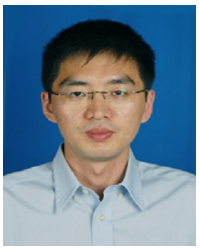

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