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DC-Link Protection and Control in Modular Uninterruptible Power Supply

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Abstract—In this paper, a DC-link voltage protection (DCVP) control method is proposed to address the DC-link overvoltage issue due to power back-feeding in parallel Uninterruptible Power Supply (UPS) system. The proposed control method is able to protect the inverter against the excessive DC-link voltage, which increases the system reliability and robustness. Moreover, a current sharing control strategy is proposed by online regulating the virtual resistance of each UPS module. The proposed current sharing control strategy is able to address the circulating fundamental and harmonic current caused by the line impedance mismatching or power back-feeding issue in the UPS system. In addition, an improved consensus-based distributed controller is proposed to alleviate the overshoot issue during the transient process in voltage amplitude and frequency restoration. Finally, the feasibility of the proposed methods are verified by experimental results from the parallel UPS prototypes.

Index Terms—Uninterruptible Power Supply(UPS), DC link voltage protection, current sharing, consensus control, Anti-windup.

I. INTRODUCTION

DRIVEN by the increasing importance of the Uninterruptible Power Supply (UPS) in the industry including enterprise IT, commercial telecom, data center and cloud computing area [1], the global market for the UPS system is projected to soar dramatically in the next few years. Meanwhile, the strong need for the UPS system to provide more reliable, efficient and secure electrical power supply for the modern digital equipment propels the UPS technology advancement by engineers and academic researchers [2].

According to the European Standard EN 62040-3 [3], the UPS systems are divided into on-line, off-line and line-interactive UPSs. In an on-line UPS system, the load is always powered by the inverter regardless of the grid condition; the only exception is that when the overloading occurs and the bypass switch closes to connect the load with the grid. In off-line and line-interactive UPS systems, however, the load power is supplied from the grid or a combination of the inverter and the grid, respectively [4]. The on-line UPS system is the most

popular and widely configured for sensitive load [5], as it provides excellent characteristic in being immune to the grid frequency variation, voltage irregularity, and other power issues [6]. The on-line UPS system is usually comprised of AC/DC rectifier, DC/AC inverter, battery and a static bypass switch [7]. Normally, Silicon Controlled Rectifier (SCR) or PWM rectifier with a diode in the DC link is widely used as the AC/DC rectifier in high power or low power UPS systems, respectively. The implementation of these topologies come from the view of cost saving and preventing the power back-feeding from the DC link to the grid [7, 8]. Meanwhile, the two-level or Neutral-Point Clamped (NPC) PWM converters are adopted as the inverters [9].

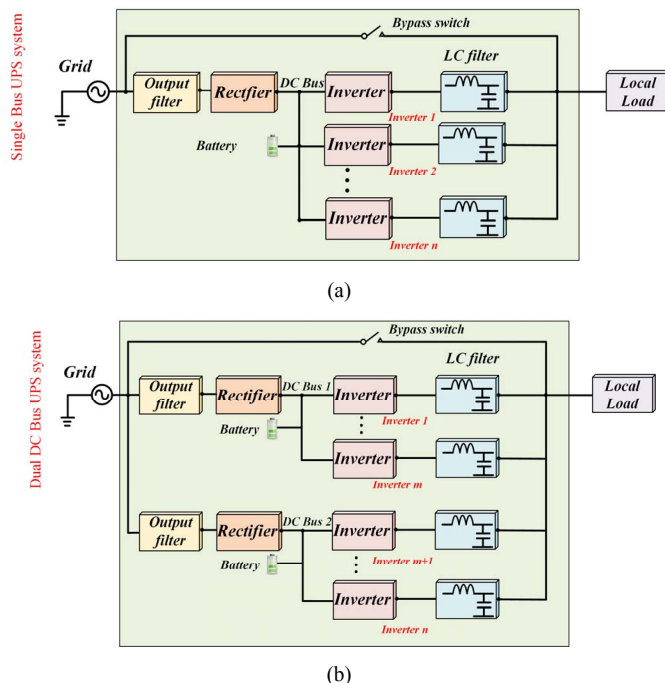


Fig. 1. Categories of parallel UPS system. (a) Single DC Bus UPS system (b) Dual DC Bus UPS system.

To realize more reliable power supply to the load, the UPS modules are connected in parallel to deliver the power to the

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load [10]. Based on IEC 62040-3:2011[7], parallel UPS systems are classified into Single DC Bus (SDB) and Dual DC Bus (DDB) structure, as shown in Fig. 1, where it is observed that SDB UPS system connects all the inverters with only one DC bus, whereas DDB one (Fig. 1(b)) assigns all the inverters into two groups. By comparison of these two topologies, it is observed that the DDB UPS system presents higher reliability and redundancy, but at the expense of higher cost.

For the normal operation of the DDB UPS system, master-slave control [11], average load sharing control [12], droop control [13] and circular chain control [14] have been proposed to regulate the power delivery, and among them, the droop control strategy has been mostly adopted. As the droop control is able to regulate the voltage amplitude and frequency without inter-communication among UPS modules, system stability and reliability can be greatly improved. However, the droop control is a load-dependent strategy that can not recover the frequency and voltage deviations caused by the load. Consequently, communication-based secondary control strategies, such as central [15] and distributed controllers [16], have been employed to compensate the frequency and voltage amplitude deviations. Recently, several works [17-20] have presented the consensus algorithm-based distributed control strategies to achieve the frequency and voltage restorations, where only UPS module's own information and its neighbor's information are needed to guarantee the stable operation. Among them, [17] proposed an unbalance voltage compensation method with the dynamic consensus control strategy. [18]-[20] proposed the consensus-based energy management algorithm to deal with the state of charge (SoC) balance in the AC/DC microgrid. However, from the experimental results of [18, 19], it is found that the consensus-based control strategy causes a large overshoot of the frequency and voltage amplitude during the restoration process. This large overshoot, which is harmful to the sensitive load, has not been reported in the previous works.

Moreover, under light load, fault or temporary overshoot situation in the DDB UPS system, the voltage difference between the UPS modules inevitably leads to the power back-feeding from higher to lower output voltage. As the unidirectional power flow rectifier (SCR type or PWM rectifier with a diode in the DC link) is adopted as the AC/DC converter, the back-feeding power can not be delivered back into the grid. Consequently, this power results in an excessively high voltage of the DC link, provokes the circulating current and even damages the DC link capacitor [21]. In addition, the power back-feeding issue exists as well when the UPS operation shifts from the normal mode to the Eco-mode [22, 23], where the grid voltage may suffer from temporally overvoltage issue when the bypass switch closes. As a result, the DC link may suffer from overvoltage as well. From the above discussion, it is imperative to investigate a DC-link voltage protection (DCVP) method to protect the DC link from overvoltage. Until now, the research on the DCVP methods is quite limited. The work of [21] proposed a method to protect the DC link by detecting the rise of the DC-link voltage. However, this method may lead to the failure of the DC-link protection as the slow dynamic response of the DC-link controller. Moreover, the circulating

fundamental and harmonic current, which are caused by the power back-feeding and line impedance mismatching, are harmful to the stable operation of the UPS system, as these circulating currents lead to the increased power losses and even overloading one of the UPS units. The circulating current issue has been investigated by some previous works [24-28]; [24, 28] proposed the circulating suppression methods to deal with zero sequence current in the common DC-bus inverter system. The PWM switching strategies were investigated by [25-27] to solve the circulating current caused by the common mode voltage. However, the aforementioned methods can not deal with the circulating current caused by the line impedance mismatching. Recently, [29-31] proposed the virtual impedance-based control strategies to deal with the circulating current in the mismatched line impedance microgrid. However, these control strategies achieve the current sharing by disturbing the frequency, which is unacceptable for the UPS system, as the critical load is sensitive to large frequency fluctuation. Overall, the previously presented works are not suitable to deal with the current circulation issue caused by power back-feeding and line impedance mismatching in the UPS system. Accordingly, an effective method needs to be explored for the fundamental and harmonic current sharing in the UPS system.

In this paper, first, a DCVP method is proposed for the DDB UPS system to solve the power back-feeding issue caused by output voltage difference and bypass switch closes without voltage amplitude synchronization. Based on the proposed method, the power back-feeding issue is significantly mitigated and will not trigger the DC-link protection. Moreover, a virtual resistance based current sharing method for fundamental and harmonic current is proposed to deal with the power back-feeding and feeder impedance mismatching. Finally, an anti-windup dynamic consensus algorithm (ADCA) is applied for voltage amplitude and frequency restoration to alleviate the large overshoot issue. The feasibility and effectiveness of the proposed methods are validated by a dSPACE 1006 based experimental prototype.

The main contributions of this paper are summarized as follows:

- 1) Active power detection-based control strategy for DCVP is proposed to prevent inverter against the excessive DC-link voltage.
- 2) Theoretical analysis for the fundamental and harmonic current sharing is presented for the UPS system. Meanwhile, the adaptive virtual resistance based control strategy is proposed for the fundamental and harmonic current sharing.
- 3) An anti-windup based consensus algorithm is proposed to solve the large overshoot problems during the process of voltage amplitude and frequency restoration.
- 4) Extensive experimental results are provided to validate the effectiveness of the proposed methods.

The rest of the paper is organized as follows: In Section II, the UPS structure and power flow analysis for the DDB UPS system is reviewed. In Section III, the proposed DCVP strategy, fundamental and harmonic current sharing techniques are illustrated. Section IV provides the anti-windup strategy for

consensus control. The experimental results are provided in Section V to show the effectiveness of the proposed methods. Finally, the conclusions are given in Section VI.

II. POWER FLOW ANALYSIS FOR UPS SYSTEM

In this paper, the DDB parallel UPS system, which is composed of SCR and two-level PWM inverter (see Fig.2), will be adopted. The SCR type rectifier is used for the power delivery from AC input to the DC link. The inverter works in Voltage Control Mode (VCM) to directly regulate the output filter's capacitor voltage and inner loop inverter side inductor's current. The bypass switch will be closed in case of overloading or when the UPS is intended to work in Eco-mode. In addition, the LC type filters are adopted to avoid the resonance brought by the LCL type filter. Some critical information, such as each UPS's output active power, is inter-communicated among the UPS modules.

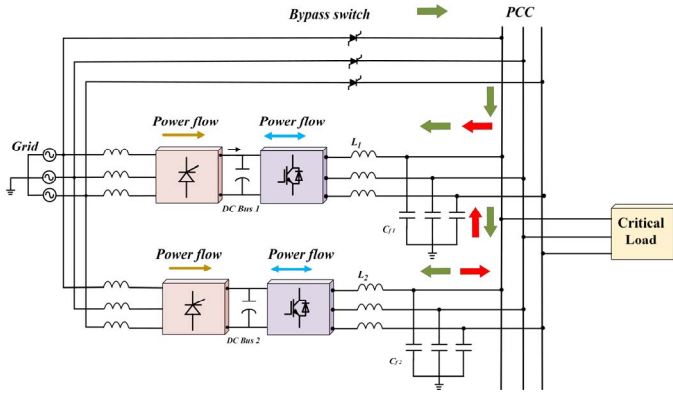


Fig.2. Active Power Feeding in the DDB UPS system

Based on IEC 62020-3:2011 standard [7], for the on-line UPS system, the battery is fully charged and works in standby mode in the normal operation. The SCR delivers the active power in unidirectional direction (Fig. 2 brown arrows) from the grid to the DC link. In the meantime, the inverter is able to operate in four-quadrants (Bi-directional, Fig. 2 blue arrows). As shown in Fig. 2, under light load and due to the tolerance between the output voltage of parallel inverters or because of the one inverter's output fault, the UPS module with higher output voltage can feed effective power into the other UPS module (red arrow in Fig.2). This feeding power may lead to the DC link voltage (in this case V_{DC1}) increase and as a result, the DC-link voltage exceeds its upper limitation, eventually, system protection is triggered without the DCVP. In addition, when UPS's operation shifts from normal mode to the Eco-mode, the bypass switch needs to be closed. In this case, the grid voltage amplitude may be higher than the voltage at PCC if the grid suffers from temporary overvoltage or voltage amplitude synchronization is not performed. In this scenario, grid power may feed into both UPS modules (Fig. 2 green arrows), which may lead to excessively high DC link voltage of both UPS modules. Consequently, the excessive DC link voltage results in the interruption of inverter's operation. Therefore, it is imperative to explore a DCVP control algorithm

III. PROPOSED METHOD FOR DC LINK PROTECTION AND CURRENT SHARING

A. Proposed method for DCVP

The principle of the DCVP is based on equipping a local DCVP controller in each UPS module; each module detects its own local output active power P_{LPF} (Fig.3), if the detected active power P_{LPF} falls below zero, which indicates this UPS module is absorbing active power ($P_{LPF} < 0$), at this time, the falling edge of active power signal (P_{LPF}) is employed to activate the DCVP controller. The error generated by comparison of zero and the negative active power P_{LPF} goes through a proportional controller K_p to generate an additional voltage amplitude reference ΔE_{comp} . This additional voltage amplitude reference ΔE_{comp} will be added to the original voltage amplitude reference E_1 from P - E droop controller to elevate the voltage reference in order to generate more active power. As a result, the additional active power counteracts the injected active power and prevents the DC link voltage from further increasing. Finally, the DC link voltage will be stabilized and operate in a new steady state point.

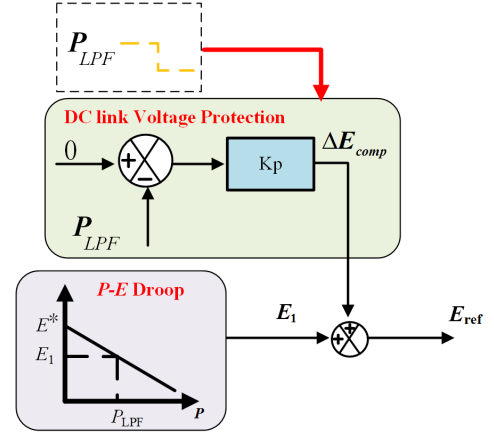


Fig.3. DC link voltage protection in UPS system

The control strategy is expressed as:

$$\Delta E_{comp} = (0 - P_{LPF}) \cdot K_p \quad (1)$$

To have a better understanding of the principle of the proposed method, first, it is assumed that output voltage of UPS 2 module drifts up (Fig.2), the excessive power is injected into UPS1, leading to the active power direction reversal in UPS 1 (Fig.2 red arrow). Due to the injected active power, the DC link voltage of UPS1 begins to increase. At the same time, the UPS local DCVP controller keeps on monitoring its own output active power. Once it detects the active power falling below zero, the DCVP controller is activated. The difference between 0 and the negative active power will be employed to generate the additional reference voltage amplitude for UPS 1 to increase the output voltage amplitude of UPS 1 and generate more active power to counteract the injected active power. Therefore, by increasing the output voltage amplitude of UPS 1, the DC-link voltage of UPS 1 will be stabilized.

The proposed DCVP controller can be applied to prevent the active power back-feeding in the transition from normal mode to the Eco-mode of the UPS system. During the transition, the

bypass switch needs to be closed in order to feed the active power to the load directly from the grid. Normally, before the bypass switch closing, the voltage amplitude and frequency between the PCC voltage and grid voltage should be synchronized. However, if grid voltage suffers from temporary overvoltage during the process of the bypass switch closing, the extra active power provided by the grid will be injected into the UPS modules, leading to overvoltage of DC bus 1 and DC bus 2 and possibly damage the DC link capacitor. However, the active power back-feeding from the grid can be effectively prevented by the DCVP controller.

B. Proposed method for current sharing

In the parallel UPS system, the circulating current may be provoked by line resistance mismatching or power feeding. Therefore, the current sharing strategy among the UPS modules should be carried out to suppress the circulating current. First, the principle of fundamental and harmonic current sharing should be investigated. Normally, the UPS system is integrated into the 120/220 V low voltage grid, where the line impedance shows the resistive characteristic. In addition, by considering the distance from the output filter of the UPS system to the load is usually short, the line resistance is quite small. In order to enhance the stability of the droop control strategy, the virtual resistance is embedded in the control strategy [4]. As the line impedance shows the resistive nature, the reactive power-frequency and active power-voltage magnitude droop control are adopted in the LC type filter based UPS systems. The droop equation can be expressed as [32]:

$$\omega = \omega^* + D_Q Q_{LPF} \quad (2)$$

$$E = E^* - D_P P_{LPF} \quad (3)$$

where ω^* and ω are the UPS nominal and reference angular frequency, E^* and E are the UPS nominal and reference voltage amplitude. P_{LPF} and Q_{LPF} are the output active and reactive power through a low pass filter with cut-off frequency ω_c . D_P and D_Q are the droop coefficients for regulating the UPS active power and reactive power, respectively. In this paper, the design of the droop coefficient is based on the static deviation method, D_Q and D_P are defined as: $D_Q = \Delta\omega/2Q_{max}$ and $D_P = \Delta V/P_{max}$, $\Delta\omega$ and ΔV are the maximum frequency and voltage deviations, and P_{max} and Q_{max} are the maximum active and reactive power delivered by the inverter, respectively. [33].

In Fig. 4 (a), the parallel UPS modules are modeled as the controlled voltage source (V_{ref}) with virtual resistance $R_{v,f}$ at fundamental frequency. $R_{line,f}$ indicates the line resistance at the fundamental frequency. It is noted that the $R_{line,f}$ can not be omitted even it is small. PCC linear load is modeled as passive RL load.

Normally, for the power flow through the feeder that consists of inductance and resistance, the voltage drop on the impedance leads to the following expression:

$$\Delta V = \frac{X \cdot Q + R \cdot P}{E^*} \quad (4)$$

where P and Q are the active and reactive instantaneous power that flows out of the general line impedance, R and X are the corresponding resistive and inductive component of the line

impedance. E^* is the nominal voltage magnitude, ΔV is the voltage magnitude drop on the impedance.

In the UPS system, by neglecting the line inductance, the voltage drop on the resistance is expressed as:

$$\Delta V = \frac{R \cdot P}{E^*} \quad (5)$$

Therefore, the relationship between the UPS output voltage and PCC voltage is expressed as:

$$V_{ref1} = V_{pcc} + \frac{R_{e1} \cdot P_1}{E^*} \quad (6)$$

$$V_{ref2} = V_{pcc} + \frac{R_{e2} \cdot P_2}{E^*} \quad (7)$$

where $R_{e1} = R_{v,f1} + R_{Line,f1}$, $R_{e2} = R_{v,f2} + R_{Line,f2}$. P_1 and P_2 are the output active power of UPS 1 and UPS 2, respectively.

It is noteworthy that the reactive power sharing with the droop control strategy should always be accurate in steady state operation of UPS system as the frequency is a global parameter for all UPS modules. The fundamental circulating current is mainly caused by the active power sharing errors. By combining (6) and (7), the active power error is expressed as:

$$P_2 - P_1 = \frac{(V_{ref2} - V_{pcc})E^*}{R_{e2}} - \frac{(V_{ref1} - V_{pcc})E^*}{R_{e1}} \quad (8)$$

It can be observed from (8) that the active power sharing error is related to two factors that include the total resistance difference (R_{e1} and R_{e2}) of the two UPS system and the voltage magnitude difference (V_{ref1} and V_{ref2}). If the circulating current is caused by the difference between V_{ref1} and V_{ref2} or line resistance mismatching (R_{Line1} and R_{Line2}), the best way to mitigate the circulating current is to adjust each UPS's virtual resistance ($R_{v,f1}$ and $R_{v,f2}$).

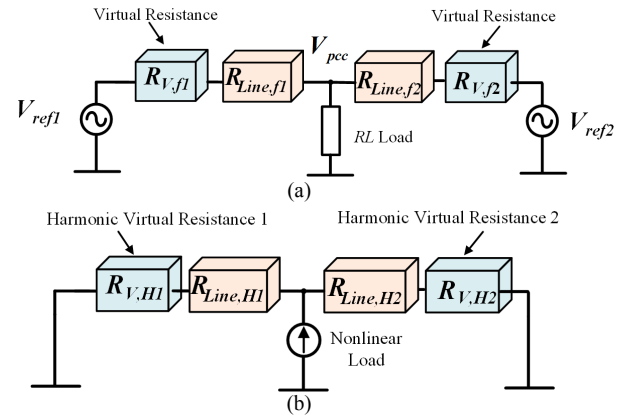


Fig.4. Equivalent circuit for UPS (a) at fundamental frequency. (b) at harmonic frequency

Meanwhile, the equivalent circuit at the harmonic frequencies when connecting a nonlinear load to PCC is shown in Fig.4(b). The harmonic resistance is expressed as:

$$R_H = R_{Line,H} + R_{v,H} \quad (9)$$

where $R_{line,H}$ and $R_{v,H}$ are the physical feeder and virtual resistance at the harmonic frequencies, respectively. It should be noted that at harmonic frequency, voltage source is considered as short circuit, since the controlled harmonic voltage source is considered as zero in the system. From Fig.4

(b), it can be observed that the decrease of UPS equivalent resistance will result in the increase of the corresponding harmonic current and vice versa. Therefore, by proper control of the virtual harmonic resistance, the circulating harmonic current can be mitigated due to line resistance mismatching.

The proposed method for current sharing at fundamental and harmonic frequencies is shown in Fig. 5. First, it is assumed that the distance from each UPS module to the critical load is different, which results in mismatching of feeder's resistance. Moreover, the DC link voltage protection controller has been activated due to the power back-feeding. At this moment, the circulation of fundamental current (due to line resistance mismatching and power feeding) and harmonic currents (due to line resistance mismatching) both exist in the parallel UPS system. When the fundamental current sharing signal activates the controller by changing the flag from 0 to 1, the active power of each UPS module will be compared with the average active power reference. The error of comparison goes through a PI controller to generate additional adaptive fundamental virtual resistance until the output fundamental current for all UPS modules are equalized.

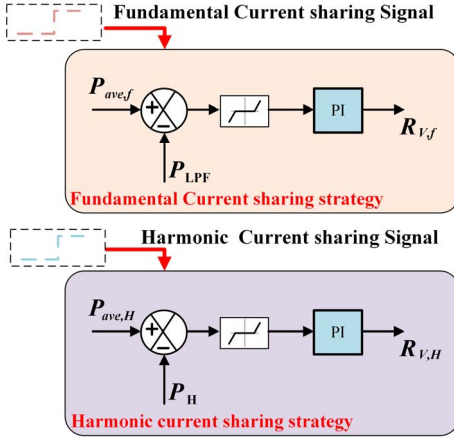


Fig. 5. Fundamental and harmonic current sharing strategy

The controller is expressed as:

$$R_{v,f} = (P_{ave,f} - P_{LPF,i}) \cdot (K_{p,f} + \frac{K_{i,f}}{s}) \quad (10)$$

where $P_{ave,f} = \frac{1}{N} \sum_{i=1}^N P_{LPF,i}$, $P_{ave,f}$ is the active power reference for all UPS modules, and $P_{LPF,i}$ indicates the active power of the i th UPS module. It is noted that the $P_{ave,f}$ can be obtained by the central or distributed communication system [19-21], where each inverter updates its active power $P_{LPF,i}$ to the central controller/distributed controller. After generating $P_{ave,f}$ by the central or the distributed controller, it will be sent to each inverter again as the reference signal of the active power sharing strategy.

For each UPS module, the active power is expressed as:

$$P_{LPF} = \frac{3\omega_c}{2(s+\omega_c)} (V_{c\alpha} \cdot I_{\alpha,f} + V_{c\beta} \cdot I_{\beta,f}) \quad (11)$$

$V_{c\alpha}$ and $V_{c\beta}$ are the measured sinusoidal UPS voltage in stationary frame, $I_{\alpha,f}$ and $I_{\beta,f}$ are the UPS fundamental positive sequence currents. The ripples of active and reactive powers are attenuated by the low-pass filter with cut-off frequency ω_c [34, 35].

Similarly, if the harmonic current sharing signal is flipped from zero to one, the harmonic power error will be employed to

regulate the harmonic virtual resistance $R_{v,H}$ at the selected harmonic frequencies as:

$$R_{v,H} = (P_{ave,H} - P_{H,i}) \cdot (K_{p,H} + \frac{K_{i,H}}{s}) \quad (12)$$

where $P_{ave,H} = \frac{1}{N} \sum_{i=1}^N P_{H,i}$, $P_{ave,H}$ is the harmonic power reference for all UPS modules, $P_{H,i}$ indicates the harmonic power of i th UPS module. For each UPS module, the harmonic power is expressed as:

$$P_H = \frac{3}{2} E^* \left(\sqrt{(I_{\alpha,5}^-)^2 + (I_{\beta,5}^-)^2 + (I_{\alpha,7}^+)^2 + (I_{\beta,7}^+)^2} \right) \quad (13)$$

where E^* is the rated UPS phase voltage. $I_{\alpha,5}^-$ and $I_{\beta,5}^-$ are the negative sequence component of UPS fifth harmonic current. $I_{\alpha,7}^+$ and $I_{\beta,7}^+$ are the positive sequence component of UPS seventh harmonic current. It should be noted that in the harmonic power calculation, only low order harmonic currents are employed to calculate the harmonic power as 5th and 7th harmonic current are the main components of harmonic orders. Finally, fundamental and harmonic current of UPS can be separated by the second-order generalized integrator (SOGI) based sequence decomposition method in Fig. 6 [36, 37], which consists of a harmonic decoupling network, Frequency Locked Loop (FLL), and multiple SOGI quadrature signal generators (SOGI-QSGs). The SOGI-based sequence extraction method shows a fast and accurate performance in detecting the fundamental frequency and harmonic frequency current under highly distorted current condition.

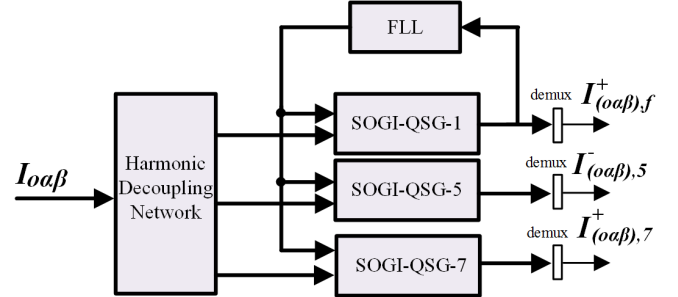


Fig. 6. Decomposition of fundamental sequence and harmonic component of the current.

In addition, once the virtual resistance is determined, the voltage drop on its corresponding virtual resistance can be calculated in stationary frame. As shown in Fig. 7, $R_{v,f}$ and $R_{v,H}$ are the fundamental and harmonic virtual resistance, respectively.

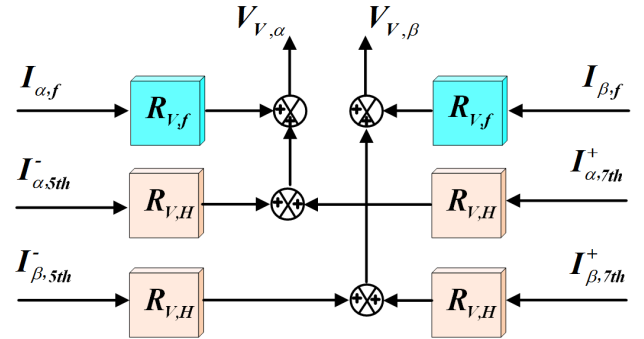


Fig. 7. Implementation of virtual resistance at the fundamental sequence and harmonic frequencies.

IV. ANTI-WINDUP DYNAMIC CONSENSUS ALGORITHM

The dynamic consensus algorithm (DCA), which has been successfully employed for secondary distributed control [38] in microgrid to achieve effective information sharing among Distributed Generation system (DGs), can be applied to UPS system as well.

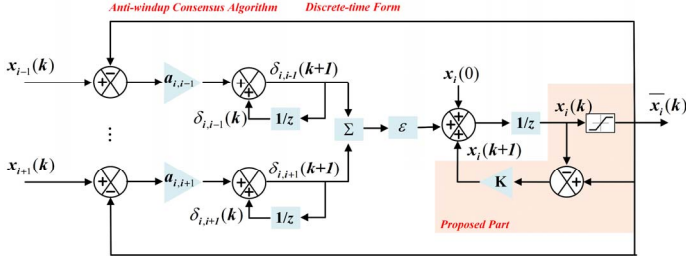


Fig.8. Control structure for ADCA

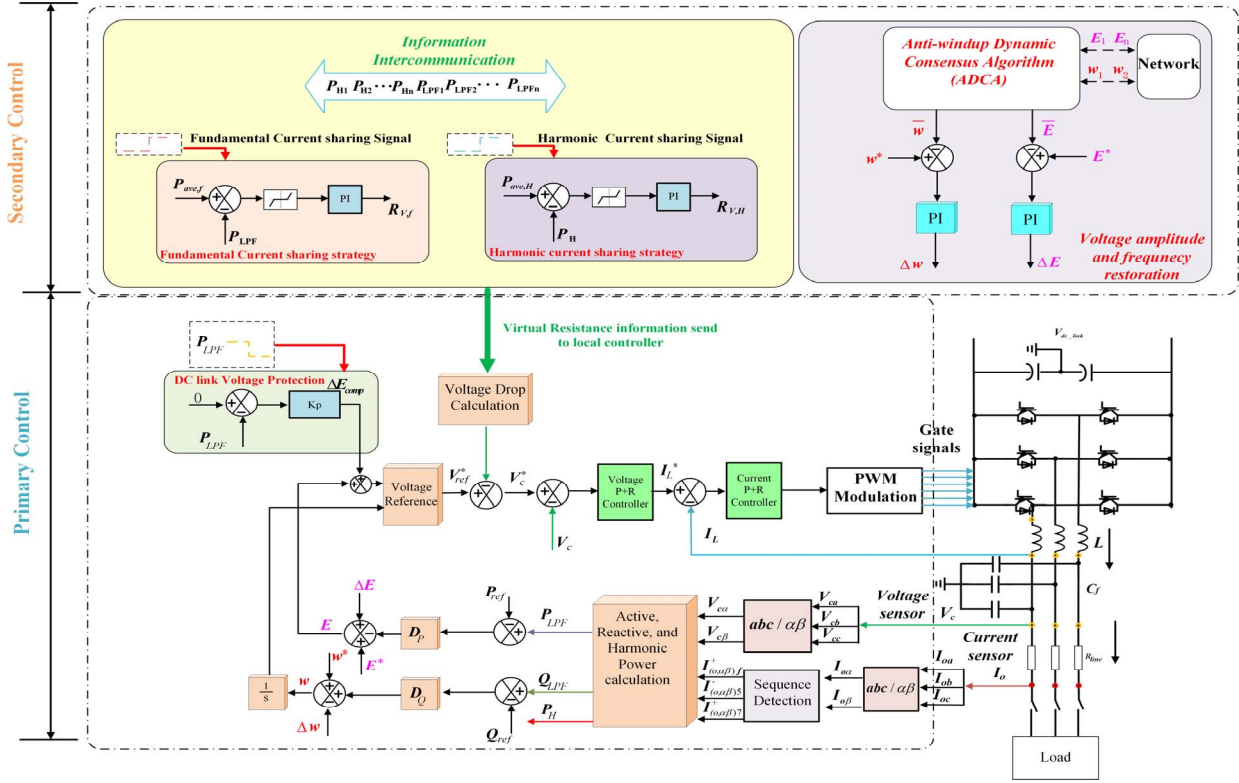


Fig.9. Complete diagram of the UPS module with the proposed control method

However, it needs to be pointed out that the voltage amplitude and frequency restoration process may suffer from large overshoot when the DCA is implemented in the secondary control. This issue is caused by the difference between fast dynamic response of DCA and slow dynamic response of PI controllers in secondary control strategy. Therefore, in this section, an anti-windup dynamic consensus algorithm (ADCA) is proposed to reduce the fast dynamic response of DCA, in this way the overshoot issue can be alleviated. The details of ADCA is shown in Fig. 8,

The discrete form of consensus algorithm is presented as:

$$x_i(k+1) = x_i(k) + \varepsilon \cdot \sum_{j \in N} a_{ij}(x_j(k) - x_i(k)) \quad (14)$$

where $x_i(k)$ indicates the information status of agent i at iteration k , a_{ij} is the connection status between node i and node

j , ε is the consensus edge weight used for tuning the dynamic of DCA.

In order to ensure the convergence of consensus to accurate value in dynamic system, a modified algorithm is applied in the paper and can be expressed as [39]:

$$x_i(k+1) = x_i(0) + \varepsilon \cdot \sum_{j \in N} \delta_{ij}(k+1) \quad (15)$$

$$\delta_{ij}(k+1) = \delta_{ij}(k) + a_{ij} \cdot (x_j(k) - x_i(k)) \quad (16)$$

where $\delta_{ij}(k)$ stores the cumulative difference between the two agents.

In this paper, $x_i(k)$ may indicate the frequency and voltage amplitude. As seen in Fig.8, the saturation block is inserted between $x_i(k)$ and $\bar{x}_i(k)$ to prevent the frequency or voltage amplitude from exceeding the permitted value and reducing the overshoot. However, only adding the saturation block in the consensus algorithm will lead to the long time windup. In order

to prevent windup and slow down the dynamic response, the back calculation method [40] is adopted to calculate the $x_i(k+1)$. Therefore, the updated $x_i(k+1)$ is expressed as:

$$x_i(k+1) = x_i(0) + \varepsilon \cdot \sum_{j \in N} \delta_{ij}(k+1) + K \cdot (\bar{x}_i(k) - x_i(k)) \quad (17)$$

From Eq.(17), it is seen that in steady state $x_i(k)$ does not exceed the saturation value, $\bar{x}_i(k) = x_i(k)$, therefore, Eq.(17) equals with Eq.(15). However, in dynamic restoration process, $x_i(k)$ exceeds the saturation block value, the anti-windup part will force the $x_i(k)$ to be lower than upper limitation value of saturation block to alleviate the frequency and voltage amplitude overshoot.

The complete control diagram is shown in Fig.9, which includes primary and secondary control level. The primary control level includes the droop control strategy, DCVP method, as well as voltage and current loops. In the secondary

control level, the fundamental current sharing, harmonic current sharing strategy, and the ADCA strategy are implemented. It should be pointed out that in order to achieve voltage tracking, a dual loop control strategy with harmonic compensators is adopted in the paper. The outer loop voltage controller is implemented to regulate the output capacitor's voltage. The inner loop current controller is nested inside the voltage control loop to regulate the inverter side current. The controllers for voltage and current regulation are expressed as:

$$G_v(s) = k_{pv} + \frac{k_{rv}s}{s^2 + (\omega_o)^2} + \sum_{h=5,7} \frac{k_{vh}s}{s^2 + (h\omega_o)^2} \quad (18)$$

$$G_i(s) = k_{pi} + \frac{k_{ri}s}{s^2 + (\omega_o)^2} \quad (19)$$

where k_{pv} and k_{pi} are the proportional terms, k_{rv} and k_{ri} are the resonant term coefficient at $\omega_o = 314 \text{ rad/s}$. k_{vh} is the resonant coefficient term for the h^{th} harmonics (5^{th} , 7^{th}). The inner current loop is designed to provide sufficient damping and protect the inductor's current from overcurrent. Finally, it should be pointed that the DCVP control strategy is used to prevent the power back-feeding. The current sharing strategy can be applied after the activation of DCVP to share the currents among the UPS modules. It can be applied in current sharing due to the line resistance mismatching as well. ADCA is implemented for secondary control strategy in normal mode of operation in UPS system.

V. EXPERIMENTAL RESULTS

TABLE I. SYSTEM PARAMETERS

System Parameter	
Filter Inductor L_f	1.8mH
ESR of Inductor	0.02ohm
Filter Capacitor C_f	27uF
DC link Capacitor	1100uF
Sampling frequency	10kHz
Rated Line to Line RMS voltage	120V
R-L load	50Ω – 1.8mH
Nonlinear load (R-L-C type)	C=20uF, L=1.8 mH, R=20Ω
DC link Voltage Protection	
Proportional gain K_p	0.2
Fundamental Current sharing Control strategy	
Proportional gain $K_{p,f}$	2e – 4
Integral gain $K_{i,f}$	1e – 4
Harmonic Current sharing Control strategy	
Proportional gain $K_{p,H}$	2e – 4
Integral gain $K_{i,H}$	1e – 4
Droop Coefficient	
Frequency droop D_q	0.0001
Voltage droop D_p	0.00005
Cut-off frequency ω_c	30 rad/s
Virtual Resistance	0.4Ω
Voltage Control Parameter	
Proportional gain K_{pv}	0.2
Resonant gain K_{iv}	100
Current controller Parameter	
Proportional $K_{p,i}$	5.6
Resonant gain $K_{i,i}$	500
ADCA parameter	
Parameter K in ADCA	0.2

In order to validate the feasibility of the proposed control strategies, a two parallel DDB UPS system shown in Fig.2 is

built up as shown in Fig. 10. The setup consists of two SCR type rectifiers and two inverters. Two DC buses are formed by DC link capacitors. The control algorithm is tested in dSPACE 1006 platform for real-time control. The system parameters are listed in Table I. Waveforms are captured by both oscilloscope and Control Desk.

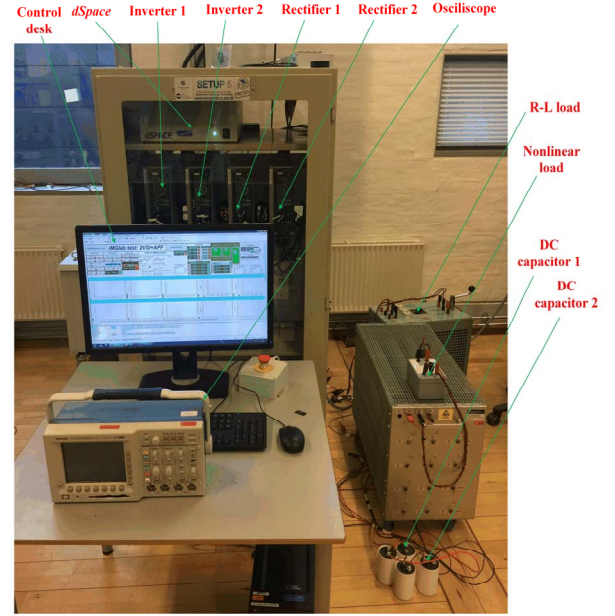


Fig.10. Experimental setup.

A. Parallel UPS Transient Response in Plug-and-Play process.

First, the power sharing capability between the two UPS modules is evaluated in the UPS plug-and-play process. As shown in Fig.11 (a), the active and reactive power are equally shared after the plug-and-play process. The output current for the two UPS modules and their errors are shown in Fig.11 (b), where it is seen that the circulating current is almost zero due to the accurate active and reactive power sharing. It is noted that the background noise is caused by the connection of D/A board to the oscilloscope.

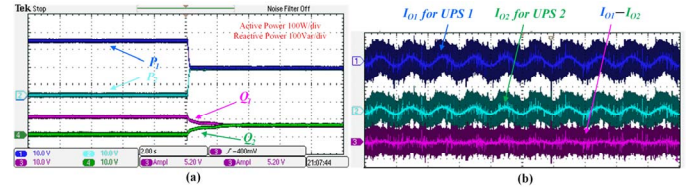


Fig. 11. UPS parallel Power sharing performance, (a) process of active and reactive power sharing, (b) current of UPS1 and UPS2 after power sharing

B. Power feeding without DC-link voltage protection

To emulate the DC-link voltage drifting-up and circulating current phenomenon in the parallel UPS modules, voltage reference in UPS 2 steps up from 100V to 103V at 2.5s; during the period between 2.5s and 2.9s, As is observed from Fig. 12, the DC link voltage V_{DC1} keeps increasing from 542V to 600V (the DC link voltage upper limit), which eventually triggers the system protection mechanism, leading to the stop operation of inverter 1 after 2.9s.

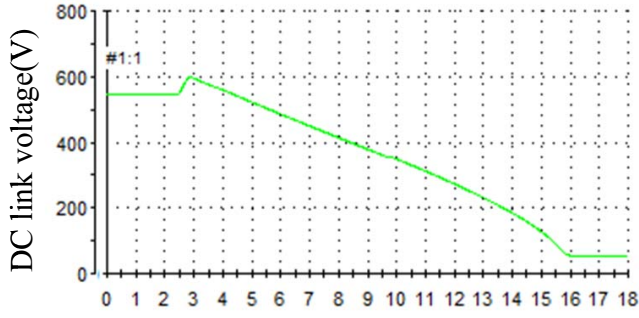


Fig.12. DC link voltage of UPS 1 without DCVP strategy

C. Active Power feeding with DC link voltage protection

When the UPSs are equipped with the DCVP controller, at 4.4s, a voltage reference in UPS 2 steps up from 100V to 103V, which leads to the active power feeding from UPS 2 to UPS 1. When the active power in UPS 1 falls below zero, the falling edge signal activates the DCVP controller. The DCVP controller tries to increase the voltage reference of UPS1 to prevent the further feeding of active power. It can be seen from Fig.13 that at 4.5s, the negative power feeding occurs and active power of UPS 1 quickly drops below zero. At this time, the DCVP is activated and increases the voltage reference of UPS1 to generate more active power and counteract the injected power. Therefore, at 4.6s, active power increased from -20W to 25W. Moreover, the DC link voltage of V_{DC1} is shown in Fig.14, it is observed that V_{DC1} increases from 542V at 4.4s but stabilized at 544V at 4.6s. However, due to the power feeding, the active power P_2 is greater than P_1 , leading to the significant fundamental circulating current between the two UPS modules (Fig.15). This issue can be solved in the next subsection.

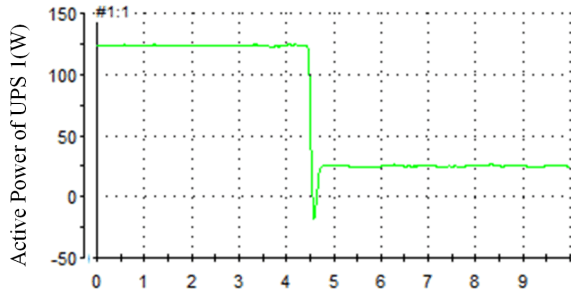


Fig.13. UPS 1's active power with DCVP

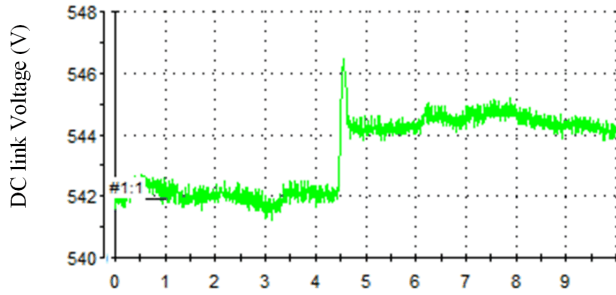


Fig.14. DC link voltage of UPS 1 with DCVP strategy.

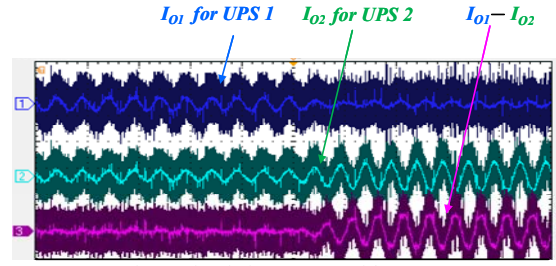


Fig.15 circulating current with DCVP

D. Fundamental current sharing

As seen in the previous subsection, after enabling the DCVP controller, the circulating current exists in the UPS system. Thus, the current sharing strategy should be activated to mitigate the circulating current. Therefore, a flag signal enables the activation of the fundamental current sharing controller at t_3 . As is shown in Fig.16, thanks to the on-line adjustment of the virtual resistance in the proposed control strategy, active power equalization for P_1 and P_2 is achieved, and the circulating current between I_{o1} and I_{o2} are minimized.

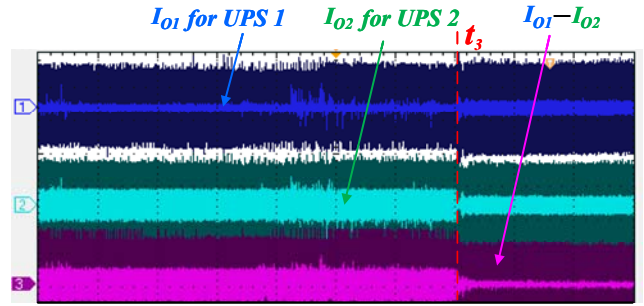


Fig.16. Circulating fundamental current

E. Harmonic current sharing

Line impedance mismatching may lead to the harmonic power sharing errors when the nonlinear load is connected in the system. In this section, three phase nonlinear load (see Fig. 17) is connected at the terminal. The value of 0.4Ω and 0.2Ω resistance are respectively adopted as the line resistance for UPS 1 and UPS2. Before activation of the harmonic current sharing strategy, the line resistance mismatching (the smaller value of line resistance in UPS 2 side) leads to the higher output harmonic current, as is shown in Fig.18. When the harmonic current sharing signal flips from zero to 1, the harmonic power begins to share as shown in Fig.19, the process of harmonic current sharing takes 25s. After completion of harmonic current sharing, the output harmonic current of UPS1 and UPS2 are equalized, as is observed in Fig.20.

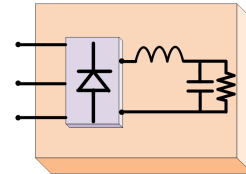


Fig. 17. Terminal harmonic load type in the experiment.

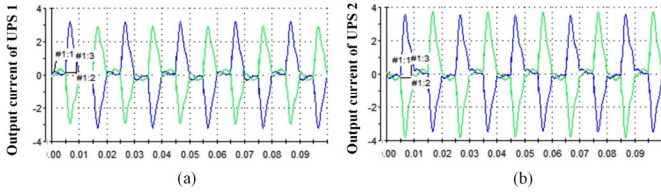


Fig. 18. Output current shown in $\alpha - \beta$ frame for UPS1 and UPS2 without harmonic current sharing. (a) Output current in $\alpha - \beta$ frame for UPS1. (b) Output current in $\alpha - \beta$ frame for UPS2.

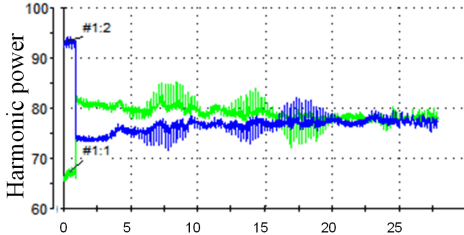


Fig. 19. Harmonic power sharing process

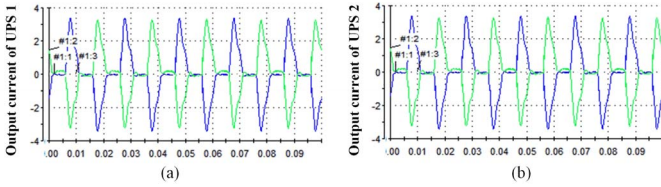


Fig. 20. Output current shown in $\alpha - \beta$ frame for UPS1 and UPS2 after harmonic current sharing. (a) Output current in $\alpha - \beta$ frame for UPS1. (b) Output current in $\alpha - \beta$ frame for UPS2.

F. Transient performance for the frequency and voltage amplitude restoration under load change

The transient frequency and voltage amplitude performance under load disturbance is examined by comparing the DCA and ADCA strategy. When the UPS's load switch from full load to half load, the frequency drops from 314.19 rad/s to 313.8 rad/s (Fig.21 (a)) when only DCA is active; while the frequency's deviation reduced by 50% when adopting ADCA (Fig.21 (b)). Meanwhile, the voltage amplitude deviation goes up to 110V with only DCA strategy, as shown in Fig.22 (a). However, the voltage amplitude deviation drop to 104V with ADCA strategy.

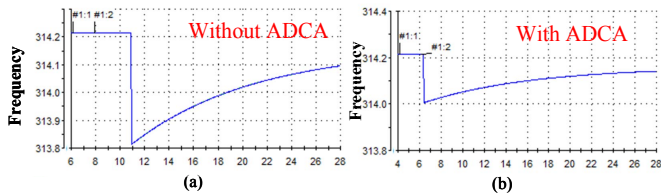


Fig.21. Comparison of frequency deviation with ADCA and DCA

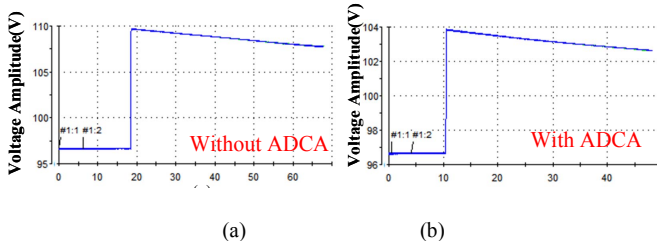


Fig.22. Comparison of voltage amplitude deviation with ADCA and DCA

VI. CONCLUSION

This paper discussed the DC-link protection and control in the modular UPS system. First, a DCVP strategy was proposed to prevent inverter against the excessive DC-link voltage. With the DCVP control strategy, the power back-feeding issue can be greatly mitigated. Moreover, an effective strategy for sharing fundamental and harmonic current in the UPS system is proposed to mitigate the impact of line resistance mismatching and the power back-feeding. Finally, an anti-windup dynamic consensus algorithm is proposed to alleviate the overshoot issue in the frequency and voltage amplitude restoration process. Experimental results show the effectiveness of the proposed methods.

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