A Step-Up Modular High-Voltage Pulse Generator Based on Isolated Input-Parallel/Output-Series Voltage-Boosting Modules and Modular Multilevel Sub-modules

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***Abstract*— Irreversible electroporation for disinfection applications involve exposing the specimen cell-membrane to a pulsed electric field in order to kill harmful microorganisms. High voltage (HV) pulses, of relatively short durations in range of few micro-seconds, are generated across the sample chamber. The HV pulse specifications such as: voltage magnitude, waveform, repetition rate, and duration differ according to the conditions of the sample being processed. This paper proposes a new step-up power electronic converter topology for generating the required HV pulses from a relatively low input voltage. The converter consists of two main stages; the first stage is responsible for boosting the input voltage to the desired level using input-parallel/output-series connected dc/dc modules while the second stage forms the required HV pulses with the proper magnitude, duration and repetition rate using modular multilevel converter sub-modules. The proposed topology is able to produce the HV pulses with controlled voltage and current stresses across the employed semiconductor switches and diodes, hence, it can be implemented with the market-available semiconductor technology. Mathematical analysis of the proposed topology is developed and MATLAB/Simulink simulation results explore operational conditions. Experimental results from a scaled-down prototype validate the functionality of the proposed system.**

***Index Terms*—DC/DC converters, Irreversible electroporation, Modular multilevel converters, pulsed electric field, pulse waveforms generator, voltage boosting**

I. Introduction

In the irreversible electroporation (IRE) process, a harmful microorganism cell-membrane is subjected to high electric field strength via a train of sufficiently high-voltage (HV) pulses [1]. IRE is useful in tumor treatment, food sterilization and air infection control [2].

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It is a good candidate for chlorination in water disinfection applications [3]. For a successful IRE process, the strength of the applied electric field, typically ranges between 2.5 kV/cm to 12 kV/cm, according to the type of the harmful microorganism and the application [4]. Applying HV pulses in kV range and microsecond range should deactivate the harmful microorganisms in the water under treatment [5]. Therefore,

HV pulse generators (PGs) are the pillar of IRE application, and should meet several challenging aspects such as modularity, scalability and flexibility [6]. Power electronics based PGs superseded classical PGs such as Blumlein lines, pulse forming networks and Marx generator aiming to meet these aspects [7].

The existing modularity with modular multilevel converter (MMC) sub-modules (SMs) has been harnessed to generate HV pulses for IRE [8]-[14]. Not only conventional rectangular pulse-waveforms can be generated by MMC based PGs, but a wide range of pulse-waveforms is also possible [5] and [10]. The majority of these topologies require an HVDC input supply and the obtained pulse peak-voltage is that of the input HVDC level. They require balancing of the individual SM capacitor voltages, ramping the HVDC input at start-up/shut-down, and protection against HVDC side faults. An exception for obtaining stepped-up voltage pulse from low voltage (LV) DC input are [13] and [14], where several series connected MMC SM capacitors are charged sequentially, then connected in series across the load to discharge. However, the voltage step-up and the pulse repetition frequency are dependent on the number of SMs and the charging process is achieved via resistors in [13] and via resistive-inductive branch in [14].

Solid-state Marx generators are introduced in the literature to provide flexibility compared with the classical Marx generator [15]. However, the ratings of the utilized switches are not identical in order to cope with their respective voltage stresses [13]. In [16], several stages of capacitor-diode voltage multipliers are incorporated to generate HV pulses from a LVDC input, but a HV switch is required to chop the pulse across the load, hence, series connection of switches is not avoided. In [17], an isolated forward converter with a step-up transformer is proposed, however, extending the topology to more than 5 kV requires series-connected semiconductors. Also, the core reset of the transformers is problematic and increasing the number of transformers increases the leakage inductance which limits the generated pulse-duration. In [18]

two boost converters charge two capacitors from a relatively LVDC input. The load is connected differentially between the two capacitors, hence, HV bipolar pulses are obtained from a LVDC input. But the passive parameters of the converters affect the flexibility of the generator and two HV switches are required, hence, series-connected switches is inevitable.

In this paper, a unipolar step-up PG (SUPG) fed from a LVDC supply is proposed based on isolated input-parallel/output-series (IPOS) voltage-boosting modules (VBMs) and MMC-SMs. The VBMs are isolated via nano-crystalline core based transformers which have low leakage and magnetizing inductance and are suitable for high-frequency operation [19]-[20]. The high voltage step-up is obtained from three mechanisms: the number of utilized VBMs, the voltage conversion ratio of the individual VBM, and the turns ratios of the step-up isolation transformers. The generated HVDC from connecting the output of the individual VBMs in series is chopped by employing two arms of series connected MMC-SMs across the load, hence, the SM-capacitors actively clamp the voltage across the semi-conductor switches [21]. High repetition pulse rates are possible, independent of the employed number of VBMs or MMC-SMs. Mathematical modeling of the proposed PG is introduced while the methodology of selecting parameters is detailed. SUPG performance is assessed via Matlab/Simulink simulations and scaled-down experimentation.

II. Basic Voltage Boosting Module of The SUPG

The basic VBM of the proposed SUPG is shown in Fig. 1. Unlike conventional DC-DC converters [22], the secondary side switches S_{x1} and S_{x2} are not necessarily working in a complementary manner. The switching pattern for the VBM devices and the developed circuit configurations are illustrated in Fig. 2. The VBM operation can be explained as follows,

i) $t_1(0 < t < \frac{D-\delta}{2}t_s)$

During period t_1, (Fig. 2b) the input current I_{in} increases and L_{in} charges, the load is connected to an open circuit, and the voltage of capacitors C_{c1} and C_{c2} are constant. The differential equations that describe the circuit in this period can be expressed as

$$\frac{dI_{in}}{dt} = \frac{1}{L_{in}}V_{in} \quad (1a)$$

$$\frac{dV_{c1}}{dt} = 0 \quad (1b)$$

$$\frac{dV_{c2}}{dt} = 0 \quad (1c)$$

$$I_o = 0 \quad (1d)$$

ii) $t_2(\frac{D-\delta}{2}t_s < t < \frac{D+\delta}{2}t_s)$

During t_2, (Fig. 2c) the input current I_{in} continues to increase while the load is connected to capacitor C_{c2} in series with S_{x1}. This leads to a sudden voltage pulse across the load. Capacitors C_{c1} and C_{c2} discharge and their voltages decrease. The differential equations that describe the circuit in this period are:

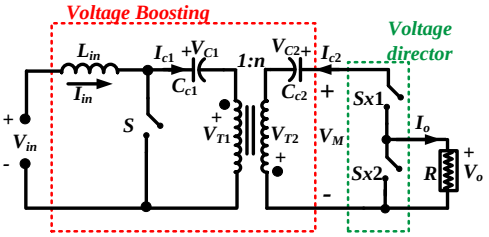


Fig. 1. The basic VBM

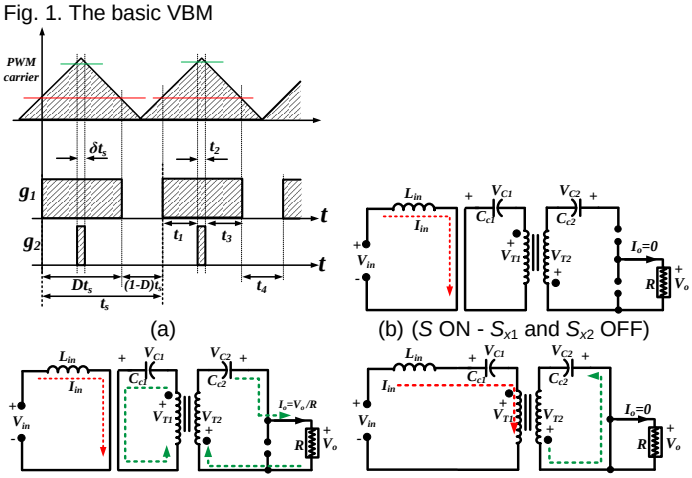


Fig. 2. Normal VBM operation: (a) operational states, (b) circuit configurations during $t_1$and t_3, (c) t_2 and (d) t_4

$$\frac{dI_{in}}{dt} = \frac{1}{L_{in}}V_{in} \quad (2a)$$

$$\frac{dV_{c1}}{dt} = \frac{-n}{C_{c1}}I_o \quad (2b)$$

$$\frac{dV_{c2}}{dt} = \frac{-1}{C_{c2}}I_o \quad (2c)$$

$$I_o = \frac{nV_{c1}+V_{c2}}{R} \quad (2d)$$

iii) $t_3(\frac{D+\delta}{2}t_s < t < Dt_s)$

The same operation is repeated as in period t_1.

iv) $t_4(Dt_s < t < t_s)$

I_{in} decreases and L_{in} discharges into the capacitors while the voltages V_{c1} and V_{c2} increase. No voltage is impressed across the load R, see Fig. 2d. The differential equations that describe the circuit in this period are

$$\frac{dI_{in}}{dt} = \frac{1}{L_{in}}V_{in} - \frac{1}{L_{in}}V_{c1} - \frac{1}{nL_{in}}V_{c2} \quad (3a)$$

$$\frac{dV_{c1}}{dt} = \frac{1}{C_{c1}}I_{in} \quad (3b)$$

$$\frac{dV_{c2}}{dt} = \frac{1}{nC_{c2}}I_{in} \quad (3c)$$

$$I_o = 0 \quad (3d)$$

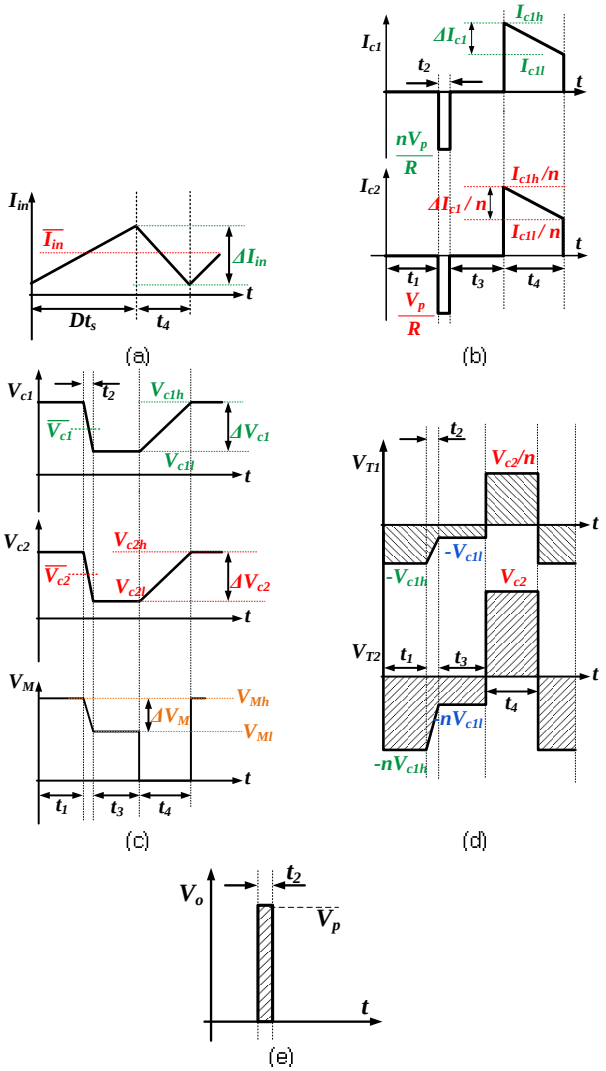


Fig. 3. Waveforms of basic VBM: (a) current through the input inductor, (b) current through C_{c1} and C_{c2}, (c) voltage across C_{c1} and C_{c2}, (d) isolation transformer primary and secondary voltages and (e) the output generated pulse.

The voltage and current waveforms of the basic VBM during one complete cycle of pulse generation are depicted in Fig. 3. Fig. 3a shows the current through the input inductor. The current through C_{c1} and C_{c2} are shown in Fig. 3b, while the voltage waveforms across C_{c1} and C_{c2} are shown in Fig. 3c along with the resultant VBM terminal voltage V_M. The isolation transformer's primary and secondary voltages are shown in Fig. 3d. Finally, the generated voltage pulse is shown in Fig. 3e.

Assuming the pulse duty ratio δ is small with respect to the main duty ratio D and solving equations (1) to (3), the values of the circuit currents and voltages are

$$\bar{I}_{in} = \frac{\delta V_p^{\,2}}{RV_{in}} \tag{4a}$$

$$\Delta I_{in} = \frac{DV_{in}t_s}{L_{in}} \tag{4b}$$

$$I_{c1h} = \frac{\delta V_p^{\,2}}{RV_{in}} + \frac{DV_{in}t_s}{2L_{in}} \tag{4c}$$

$$I_{c1l} = \frac{\delta V_p^{\,2}}{RV_{in}} - \frac{DV_{in}t_s}{2L_{in}} \tag{4d}$$

$$V_P = \frac{n}{1-D}V_{in} \tag{4e}$$

$$\bar{V}_{c1} = V_{in} \tag{4f}$$

$$\Delta V_{c1} = \frac{(1-D)\bar{I}_{in}t_s}{C_{c1}} \tag{4g}$$

$$V_{c1h} = V_{in} + \frac{(1-D)\bar{I}_{in}t_s}{2\,C_{c1}} \tag{4h}$$

$$\bar{V}_{c2} = \frac{nD}{1-D}V_{in} \tag{4i}$$

$$\Delta V_{c2} = \frac{(1-D)\bar{I}_{in}t_s}{nC_{c2}} \tag{4j}$$

$$V_{c2h} = \frac{nD}{1-D}V_{in} + \frac{(1-D)\bar{I}_{in}t_s}{2nC_{c2}} \tag{4k}$$

$$V_{c2l} = \frac{nD}{1-D}V_{in} - \frac{(1-D)\bar{I}_{in}t_s}{2nC_{c2}} \tag{4l}$$

$$V_{Mh} = V_{c2h} + nV_{c1h} \tag{4m}$$

$$V_{Ml} = V_{c2l} + nV_{c1l} \tag{4n}$$

III. Structure and Operation of the Proposed SUPG Topology

Fig. 4 shows the proposed SUPG is comprised of the PISO of N of the voltage boosting modules shown in Fig. 1. Galvanic isolation of the boosting part in the individual VBM enables series connection of N modules, while for HV voltage sharing the initial switches S_{x1} and S_{x2} are replaced by two arms (Arm1 and Arm2) of series connected MMC-SMs.

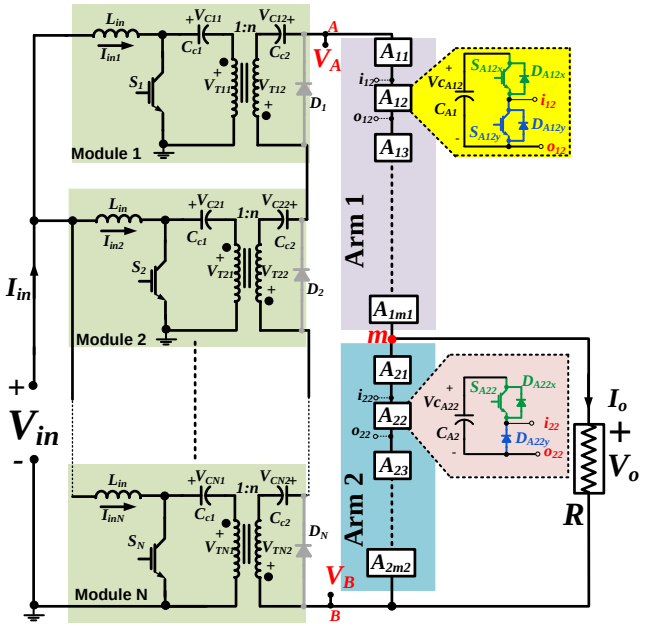


Fig. 4. The proposed SUPG.

Arm1 is formed of m_1 conventional half-bridge SMs, while each of the m_2 SMs of Arm2 are formed with two diodes, a switch, and a capacitor.

The basic operation of the proposed SUPG can be described as follows: with the operation sequence shown in Fig. 2a, switches S_1, S_2…S_N are turned ON during t_1, t_2, and t_3 and OFF otherwise, allowing the input inductors to energise. During t_2, the lower switches of the SMs in Arm1 (S_{A1jy} where, $j \in \{1, 2, \ldots m_1\}$) are turned ON, that is bypassed while the lower diodes in Arm2 (D_{A2ky} where $k \in \{1, 2, \ldots m_2\}$) are reverse biased, thus, a voltage difference V_{AB} is impressed across the load. During t_4, the lower diodes of the SMs in Arm1 (D_{A1jy} where $j \in \{1, 2, \ldots m_1\}$) and Arm2 conduct a charging current of $I_{in}/n/N$ through the N charging capacitors C_{c2}.

Diodes (D_1, $D2$,…D_N) are installed to prevent unintended series connection of secondary sides of the isolation transformers due to any delay in primary side switches gate signals.

Thus based on the VBM in section II and assuming that the component values of the N VBMs are identical, the average voltages of the voltage boosting stage can be calculated as

$$\bar{V}_{Ci1} = V_{in} \tag{5a}$$

$$\bar{V}_{Ci2} = \frac{nD}{1-D} V_{in} \tag{5b}$$

where $i \in \{1, 2, \ldots N\}$. The input inductor current of the individual VBMs are:

$$\bar{I}_{ini} = \frac{\delta V_p^2}{NRV_{in}} \tag{6}$$

The primary and secondary transformer voltages are:

$$\bar{V}_{Ti1} = \begin{cases} -V_{in} & 0 < t < Dt_s \\ \dfrac{DV_{in}}{(1-D)} & Dt_s < t < t_s \end{cases} \tag{7a}$$

$$\bar{V}_{Ti2} = \begin{cases} -nV_{in} & 0 < t < Dt_s \\ \dfrac{nDV_{in}}{(1-D)} & Dt_s < t < t_s \end{cases} \tag{7b}$$

During t_2, the midpoint 'm' is connected to the upper point 'A' through the semiconductor switches S_{A1jy}. Consequently, a voltage pulse with duty ratio δ and magnitude V_p is impressed across the output load R. The voltage peak is:

$$\begin{aligned} V_p &= \sum_{i=1}^{i=N} (V_{Ci2} - V_{Ti2}) \\ &= N\left(\frac{nD}{1-D} V_{in} + nV_{in}\right) \\ &= \frac{nN}{1-D} V_{in} \end{aligned} \tag{8}$$

As concluded from (8), the output voltage is amplified by three mechanisms: (i) the N utilized VBMs basic cell converters, (ii) transformer turns ratio n, and (iii) the individual VBMs duty ratio D. The average capacitor voltages of the Arm1 and Arm2 SM-capacitors are:

$$V_{cA1j} = \frac{V_p}{m_1}, \quad j \in \{1, 2, \ldots m_1\} \tag{9a}$$

$$V_{cA2k} = \frac{V_p}{m_2}, \quad k \in \{1, 2, \ldots m_2\} \tag{9b}$$

In the next section, a design process is presented for SUPG system parameter selection.

IV. Proposed SUPG Parameters Selection

The main merits of the proposed SUPG are that of obtaining high voltage output pulses with the readily available semiconductor technology and a relatively low input voltage; thus modularity, scalability and flexibility features arise. Starting from the load side, the voltage and current stresses of the Arm1 SMs are:

$$\hat{V}_{SA1jx} = \frac{V_p}{m_1}, \quad j \in \{1, 2, \ldots m_1\} \tag{10a}$$

$$\hat{V}_{SA1jy} = \frac{V_p}{m_1} \tag{10b}$$

$$\hat{I}_{SA1jy} = \frac{V_p}{R} \tag{10c}$$

$$\hat{I}_{DA1jy} = \frac{\bar{I}_{in}}{n} \tag{10d}$$

The current stresses of the clamping switches and diodes (S_{A1jx} and D_{A1jx}) are relatively small and hence, switches with lower current ratings can be used. Similarly, the voltage and current stresses of the Arm2 SMs are:

$$\hat{V}_{SA2kx} = \frac{V_p}{m_1}, \quad k \in \{1, 2, \ldots m_2\} \tag{11a}$$

$$\hat{V}_{DA2ky} = \frac{V_p}{m_1} \tag{11b}$$

$$\hat{I}_{DA2ky} = \frac{\bar{I}_{in}}{n} \tag{11c}$$

Assuming a modular design and 'γ' and 'ε' are the voltages and current derating factors of the Arm SMs devices, the number of Arm1 SMs (m_1) is:

$$m_1 \geq \frac{V_p}{\gamma V_{rA1}} \tag{12a}$$

$$I_{rA1} \geq \frac{\bar{I}_{in\_max}}{\varepsilon n} \tag{12b}$$

where, V_{rA1} and I_{rA1} are the rated voltage and current of Arm1 devices respectively. The number of Arm2 SMs (m_2) is:

$$m_2 \geq \frac{V_p}{\gamma V_{rA2}} \tag{13}$$

where, V_{rA2} is the rated voltage of Arm 2 devices. As they conduct the charging currents of the clamping capacitors, the current ratings of Arm2 SM devices can be small compared to Arm1 device ratings. Similarly, assume that 'α' and 'β' are the voltages and current derating factors of the devices in the

VBMs, the number of the boosting modules (N) is:

$$N \geq \frac{\bar{I}_{in\_max}}{\beta I_{rM}} \quad (14)$$

The maximum duty ratio D_{max} is related to the voltage stresses across the module's devices,viz.:

$$D_{max} \leq \frac{V_{rM} - \alpha V_{in}}{V_{rM}} \quad (15)$$

'V_{rM}'and 'I_{rM}'are the rated voltage and current of the VBM devices.

The passive element values are selected in order to keep the ripple current and voltage within certain ranges. The ripples across the different elements can be calculated from [23], [24] as:

$$\Delta V_{cc1} = \frac{\bar{I}_{in\_max}(1-D_{max})t_s}{NC_{C1}} \quad (16a)$$

$$\Delta V_{cc2} = \frac{\bar{I}_{in\_max}(1-D_{max})t_s}{nNC_{C2}} \quad (16b)$$

$$\Delta I_{in1} = \frac{V_{in}D_{max}t_s}{L_{in}} \quad (16c)$$

Defining the ripple factors as:

$$x = \Delta V_{Cc1}/\bar{V}_{Cc1}, y = \Delta V_{Cc2}/\bar{V}_{Cc2}, and \quad z = \Delta I_{in1}/\bar{I}_{in1} \quad (17)$$

Accordingly, the passive element values should be kept as:

$$C_{C1} \geq \frac{\bar{I}_{in\_max}(1-D_{max})^2 t_s}{Nx V_{in}} \quad (18a)$$

$$C_{C2} \geq \frac{\bar{I}_{in\_max}(1-D_{max})^2 t_s}{n^2 Ny V_{in}} \quad (18b)$$

$$L_{in} \geq \frac{N V_{in} D_{max} t_s}{z \bar{I}_{in\_max}} \quad (18c)$$

TABLE I
SUPG PARAMETERS SELECTION TO GENERATE 10KV PULSES

Parameter	Value
Input dc voltage	V_{in} = 100V
Output Pulse peak-voltage	V_p= 10 kV
Pulse repetition time	t_s = 100 µs
Maximum pulse duty ratio	δ_{max}= 0.1
Maximum input current	I_{in_max}= 200A
Rated voltages of SM devices	V_{rA1}=V_{rA2} = 1500V
Rated currents of SM devices	I_{rA1}= I_{rA2}= 40A
Rated voltage of VBM devices	V_{rM} = 600V
Rated current of VBM devices	I_{rM} = 60A
Derating factors of VBMs	α = 0.75 and β = 0.75
Derating factors of MMC-SMs	γ=0.75and ε= 0.75
Number of VBMs	N= 5
Transformers turns ratio	n= 5
Number of SMs in Arm1 and Arm2	m_1= m_2 = 9
Max. duty ratio of VBMs	D_{max} = 0.8
Ripple factors	x=10%, y = 2% and z = 10%
VBMs capacitances	C_{c1}=80µF and C_{c2}=10µF
VBMs inductances	L_{in} = 2mH
MMC-SM capacitances	C_{A1} = C_{A2} = 2 µF

Because the energy transfer is conducted through the boosting modules capacitors C_{c1} and C_{c2}, the SMs capacitance values of Arm1 and Arm2 can be relatively small. The upper switches in SM cells (S_{A1jx} and S_{A2kx}) are responsible for discharging the capacitors when their terminal voltages increase above the desired range for any unexpected reason in order to ensure balanced voltages across the cells. Based on the previous analysis, the parameters of the proposed system are as in Table I for generating a HV pulses of 10 kV peak. For modular design, all the transformers are wound for isolation and clearance voltage higher than the peak value of the pulses as this stress voltage is experienced by the cell at the highest potential. In addition, if the ground point is moved to the point m, the required insulation voltage will drop to half the output voltage, without affecting the main operation of the converter.

V. SIMULATION RESULTS

MATLAB/SIMULINK simulations of the SUPG in Fig. 4, with the values in Table I, illustrate the operation of the proposed HV topology.

TABLE II
SUPG PARAMETERS FOR THE EXPERIMENTAL RIG

Parameter	Value
Input dc voltage	V_{in} = 50V
Output Pulse peak-voltage	V_p= 500 V
Load resistance	R = 100Ω
Switching time	t_s = 100 µs
Number of VBMs	N = 2
Transformers turns ratio	n= 1
Number of SMs in Arm1 and Arm2	m_1= m_2 = 2
Maximum duty ratio of VBMs	D_{max} = 0.8
VBMs capacitances	C_{c1} =10µF and C_{c2}=10µF
VBMs inductances	L_{in} = 30mH
MMC-SM capacitances	C_{A1} = C_{A2} = 2 µF
IGBT switches part no.	FGY75N60SMD

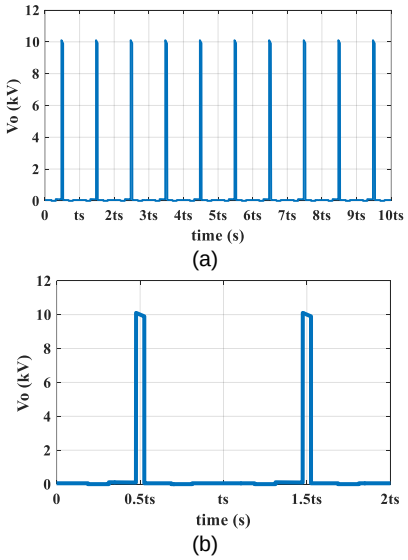


Fig. 5. Simulation results of Load voltage pulses with 10kHz repetition rate and pulse duration of 5µs. (a) Train of pulses. (b) Zoomed-view of the pulses train.

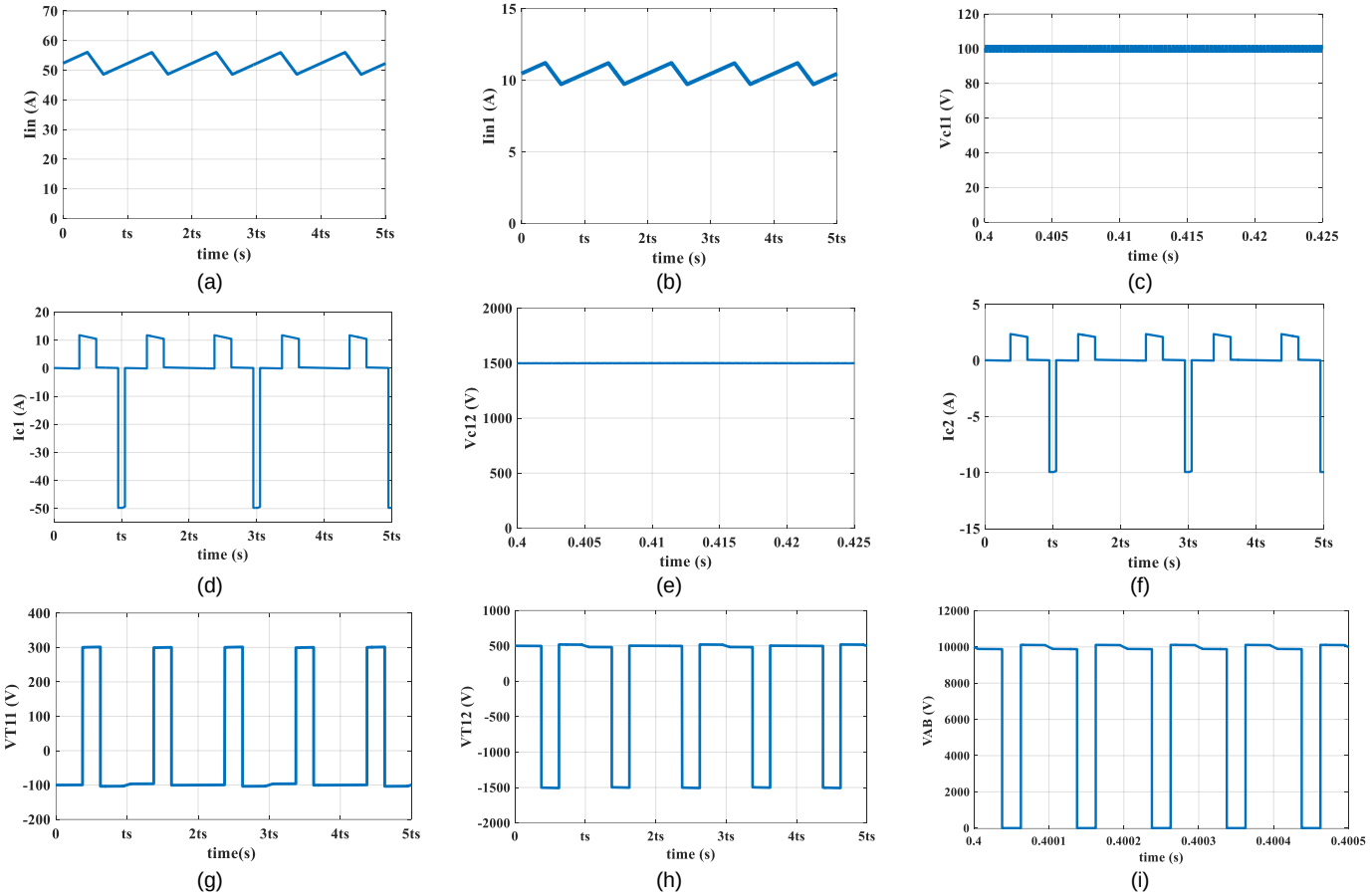


Fig. 6. Simulations of current and voltage waveforms at different parts of the SUPG (5kHz repetition rate and pulse duration of 20µs). (a) Total input current drawn from the dc-input supply. (b) First VBM input current. (c) First VBM primary side capacitor voltage (V_{c11}). (d) First VBM primary side capacitor current. (e) First VBM secondary side capacitor voltage (V_{c12}) (f) First VBM secondary side capacitor current (g) Voltage across the first VBM primary side (V_{T11}). (h) Voltage across the first VBM secondary side (V_{T12}). (i) Total terminal voltage (V_{AB})

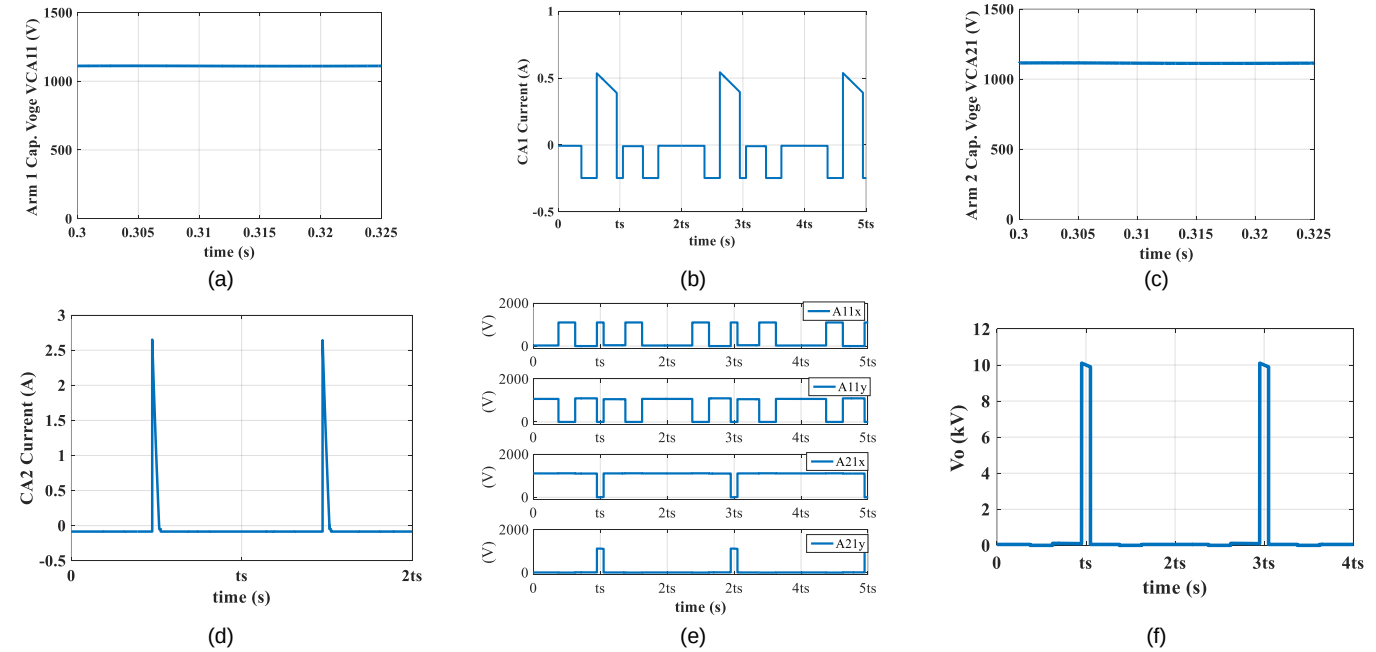


Fig. 7. Simulations of current and voltage waveforms at different parts of the SUPG (5kHz repetition rate and pulse duration of 20µs). (a) First SM capacitor voltage in Arm1. (b) First SM capacitor current in Arm1. (c) First SM capacitor voltage in Arm2. (d) First SM capacitor current in Arm2. (e) Switches voltages, and (f) Output pulses with 5kHz repetition rate and pulse duration of 20µs.

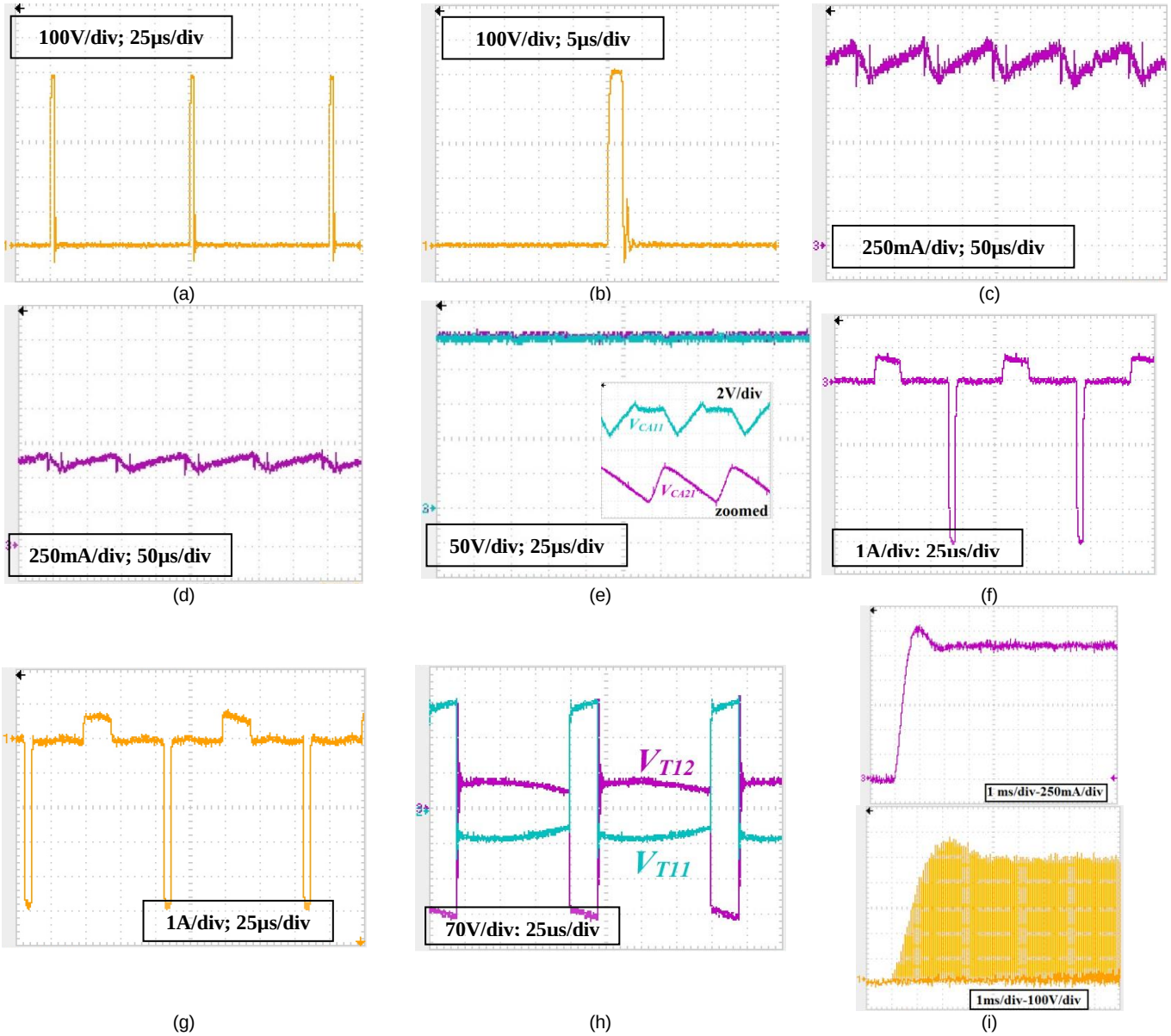
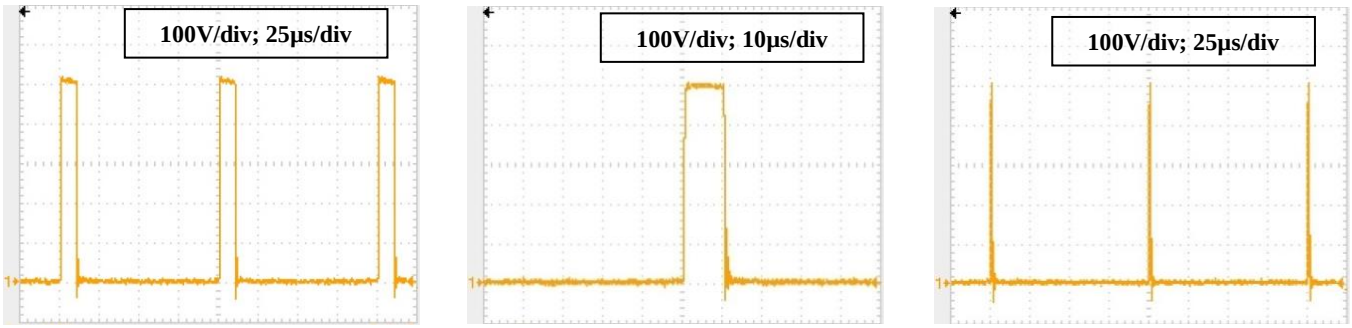


Fig. 8. Experimental results of the scaled-down SUPG topology. (a) Output pulses train of with 10kHz repetition rate and pulse duration of 2.5µs. (b) Zoomed-view for a single pulse. (c)Total input current drawn from the dc-input supply. (d) First VBM input current. (e) SM-Capacitors voltage in Arm1 and Arm2 (Ch2: V_{cA11} and Ch3: V_{cA21}). (f) Current through Cc1. (g) Current through Cc2. (h) Voltage across the first VBM primary and secondary sides. (i) Input current and output voltage dynamic response during starting.



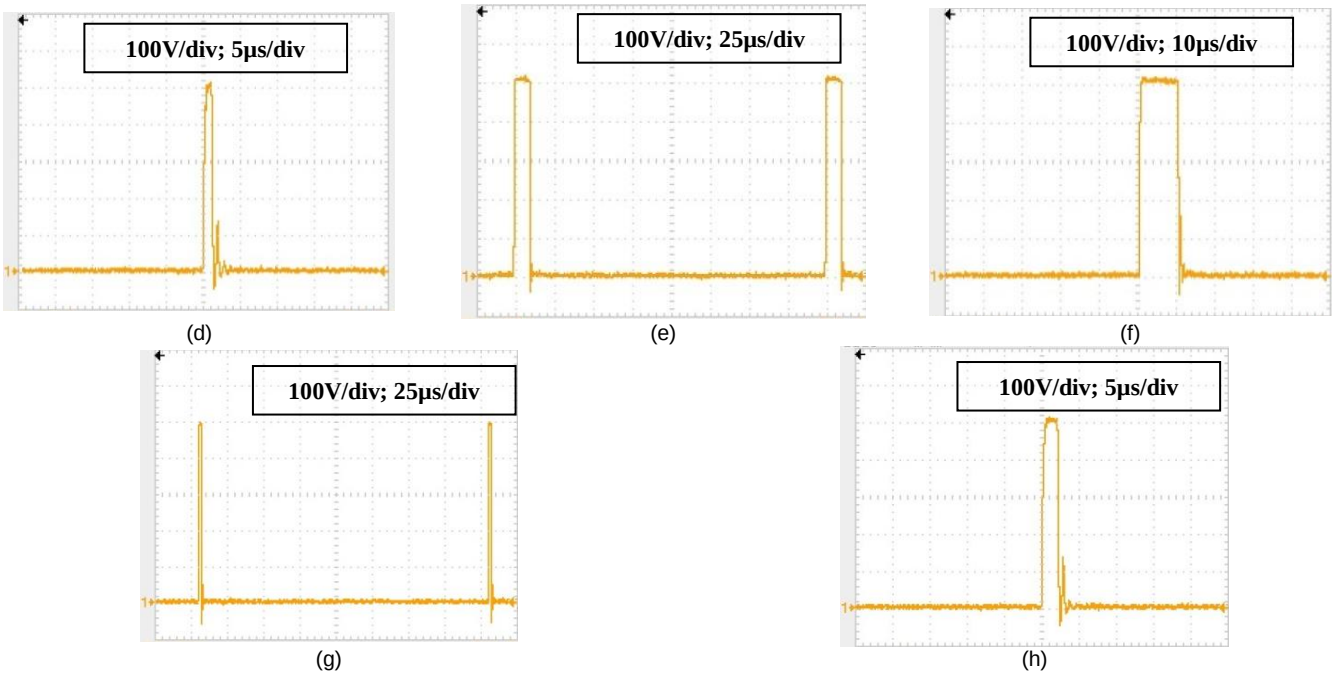


Fig. 9. Experimental results of generating different pulse repetition-rates and pulse-durations by the scaled-down SUPG topology. (a) Train of 10 kHz and 10µs pulses. (b) Zoomed view of (a). (c) Train of 10 kHz and 2.5µs pulses. (d) Zoomed view of (c). (e) Train of 5 kHz and 10µs pulses. (f) Zoomed view of (e). (g) Train of 5 kHz and 2.5µs pulses. (h) Zoomed view of (g).

Fig. 5 shows the load voltage pulses with δ = 0.05 (that is the generated pulse time is 5µs) and when the repetition rate of the output train pulses is equal to the switching frequency of the boosting modules (f_s=10 kHz). Nevertheless, the generated pulses repetition rate is independent of f_s and can be varied according to the application.

The key performance current and voltage waveforms at different parts of the SUPG are depicted in Fig. 6. Fig. 6a shows the total input current drawn from the input supply, while the first VBM current is shown in Fig. 6b with one-fifth the total input current as expected. The capacitor voltages of the primary, V_{c11}, and secondary, V_{c12}, sides of the first VBM are shown in Figs. 6c and 6e, respectively. The currents through C_{c1} and C_{c2} are shown in Fig. 6d and 6f. The terminal voltage V_{AB} is shown in Fig. 6i.

The voltages across the primary (V_{T11}) and secondary (V_{T12}) of the first VBM are shown in Figs. 6g and 6h, respectively, which confirm the voltage second balance for the transformer. The individual SM voltages in Arm1 and Arm2 are explored in Figs. 7a and 7c, respectively. As aforementioned, the generated output pulse train repetition rate not necessarily the same as the VBMs switching frequency. Therefore, Fig. 7f shows the output voltage pulses with repetition rate of 5kHz and pulse duration of 20µs when the boosting modules switching frequency is f_s = 10 kHz.

During the starting of the proposed converter, the duty ratio D can be increased gradually following a first-order capacitive circuit manner until it reaches the final steady-state value in order to ease the charging process of the SM capacitors and avoid exceeding the acceptable limits.

VI. Experimental Results

To show operation of the proposed system and validate the mathematical analyses and simulation results, a scaled-down hardware prototype with the parameters in Table II and controlled with Texas Instruments TMS320F28335 DSP is constructed. Fig. 8a shows a train of the experimentally generated output voltage pulses with 500V pulse-peak, 10 kHz repetition rate and 2.5µs pulse duration. A zoomed view for a single pulse is depicted in Fig. 8b. Figs. 8c and 8d show the total input current drawn from the input supply and the first VBM drawn current, it is clear that since two VBMs are utilized, the first VBM draw one-half the total input current. The first SM-capacitor voltage in Arm1 and Arm2 are explored in Fig. 8e. The current through the first SM-capacitors (C_{c1} and C_{c2}) are shown in Figs. 8f and 8g, respectively. Moreover, the voltages across the primary (V_{T11}) and secondary (V_{T12}) of the first VBM are shown in Fig. 8h. To show the dynamic performance of the proposed pulse generator, Fig. 8i shows the input current drawn from the LVDC supply as well as the created output voltage pulses across the load from the starting moment.

Finally, the flexibility of generating wide range of different pulse repetition rates and pulse durations are explored in Fig. 9. With pulse duration of 10µs and repetition rate of 10 kHz, Fig. 9a shows the generated train of pulses with zoomed-view for individual pulse at Fig. 9b. Additionally, Figs. 9c and 9d explore the train of pulses with the same 10 kHz repetition rate and 2.5µs pulse durations. Figs. 9e and 9f show pulses with 5 kHz repetition rate and 10µs pulse duration, while Figs. 9g and 9h show pulses with 5 kHz repetition rate and 2.5µs pulse duration. The experimental prototype is shown in Fig. 10.

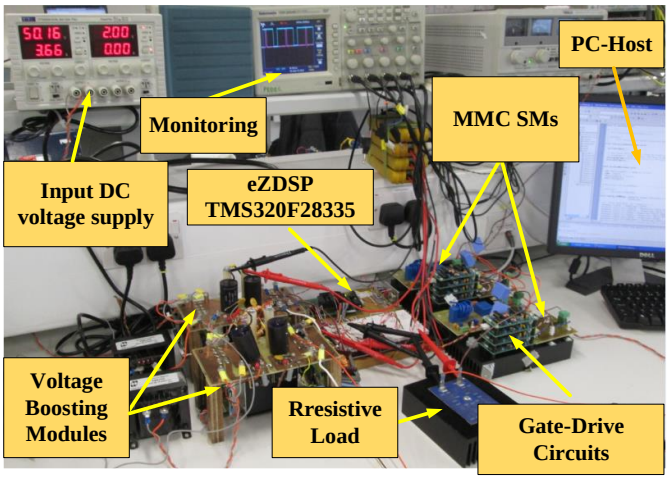


Fig. 10. The scaled-down experimental set-up.

VII. Conclusion

This paper proposed a new HV pulse generator topology for electroporation applications. The topology employs input-parallel/output-series boosting modules in order to permit the use of a low voltage dc input supply. The amplified HV voltage is chopped with two MMC arms incorporating small clamping capacitors. Unlike many step-up HV generators in the literature, the boosting module capacitors of the proposed topology are charged simultaneously, allowing operation with a wide range of pulse widths and repetition rates. The simultaneous charging and discharging of VBMs implies that their switch gate signals are common to controller, consequently the control burden is low. The carried out simulation results showed the operation of the proposed topology, where the input LVDC is amplified by one hundred times using only five VBMs. Scaled-down experiment confirmed the feasibility of the proposed topology when the LVDC input is amplified by ten times using only two VBMs. Despite the obtained high amplification gains, the stresses on the utilised components are equal and acceptable. Thus, the proposed modular configuration allows the use of the market-available voltage and current ratings semiconductors. Moreover, the proposed topology can be extended to generate bipolar voltage pulses, which may be required for some irreversible electroporation applications, with two additional MMC arms across the treatment chamber.

Finally, the main contribution of the proposed SUPG topology can be summarized as:

- It achieves an HV pulse voltage by employing a three-folded stepping-up technique (VBMs duty ratio, step-up transformers turns ratio and series connection of the VBMs) from the LVDC input supply.
- It avoids using HV switches and series connection of switches to chop the generated HVDC voltage.
- It has the ability of generating unipolar/bipolar rectangular pulses with flexible voltage peak, repetition rate and pulse duration.
- It does not require voltage sensors.
- Its MMC SM capacitors, of small capacitance, are charged swiftly and simultaneously.
- It provide redundancy, modularity and scalability by employing several identical VBMs and MMC SMs.
- It allows the use of market-available components.

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