

Switching-Cell Arrays – An Alternative Design Approach in Power Conversion

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Abstract— The conventional design of voltage-source power converters is based on a two-level half-bridge configuration and the selection of power devices designed to meet the full application specifications (voltage, current, etc.). This leads to the need to design and optimize a large number of different devices and their ancillary circuitry and prevents taking advantage from scale economies. This paper proposes a paradigm shift in the design of power converters through the use of a novel configurable device consisting on a matrix arrangement of highly-optimized switching cells at a single voltage class. Each switching cell consists of a controlled switch with antiparallel diode together with a self-powered gate driver. By properly interconnecting the switching cells, the switching cell array (SCA) can be configured as a multilevel active-clamped leg with different number of levels. Thus, the SCA presents adjustable voltage and current ratings, according to the selected configuration. For maximum compactness, the SCA can be conceived to be only configurable by the device manufacturer upon the customer needs. For minimum cost, it can also be conceived to be configurable by the customer, leading to field-configurable SCAs. Experimental results of a 6x3 field-configurable SCA are provided to illustrate and validate this design approach.

Index Terms— Active-clamped, field-configurable, multilevel, switching-cell array.

I. INTRODUCTION

THE power stage of a power converter is typically conceived combining elementary power semiconductor devices (such as transistors and diodes) with capacitors, inductors, and transformers [1]–[4]. Power semiconductor devices operate in commutation as controlled or uncontrolled switches. Capacitors, inductors, and transformers act as filters, energy storage elements, scale voltage and current, or provide galvanic isolation. A basic building block for the semiconductor-component part of voltage-source power converters is the two-level half-bridge topology presented in Fig. 1(a). It consists of an arrangement of two controlled

switches with antiparallel diodes. From a mathematical system perspective, the block receives as inputs the dc voltage v_{dc} across its dc-link terminals and the current through the leg pole terminal i_p . The block provides as outputs voltage v_p , current i_{dc1} , and current i_{dc2} . The two switches operate with complementary states to connect the leg pole terminal p to either dc_1 or dc_2 dc-link terminals (see Fig. 1(b) and Fig. 1(c)). Thus, the half-bridge leg is functionally equivalent to a single-pole double-throw switch. For a given switching state, current i_p , shown in red, flows through the on-state switch or its antiparallel diode or both, depending on the current direction and the switch technology. For $i_p > 0$, switching losses concentrate on the turn-on and off of the blue switch. For $i_p < 0$, switching losses concentrate on the turn-on and off of the orange switch. Voltage v_p is a two-level waveform, as depicted in Fig. 1(d). Thus, Fig. 1(a) is regarded as a two-level configuration.

Using one or more units of the basic building block of Fig. 1(a) it is possible to configure all types of conversion systems: dc-dc converters with bidirectional power-flow capability and with or without galvanic isolation (a popular example of the former is the single-phase or three-phase dual active bridge), single-phase or multiphase dc-ac converters with bidirectional power-flow capability (i.e., capable of operating as inverters or rectifiers), and ac-ac converters with bidirectional power-flow capability (through the back-to-back connection of two dc-ac converters).

However, the power semiconductor devices in Fig. 1(a) have to be designed with a proper voltage rating to be able to block the required application operating voltage v_{dc} . In addition, for a given voltage rating, since the devices in Fig.

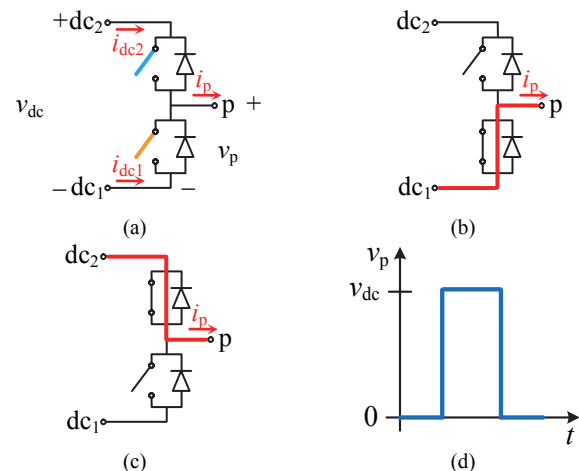


Fig. 1. Two-level half-bridge leg. (a) Topology. (b) Switching state of connection to terminal dc_1 . (c) Switching state of connection to terminal dc_2 . (d) Pole terminal voltage pattern.

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1(a) withstand both conduction and switching losses, the power device design tradeoffs have to be explored to produce a competitive device with a proper balance of conduction and switching performance, according to the application operating conditions; i.e., current level and switching frequency. All the above has led to the need to design many different power devices with different voltage ratings and different combinations of conduction-switching performance, and has motivated the exploration of several device technologies (metal-oxide-semiconductor field-effect transistors (MOSFET), insulated-gate bipolar transistors (IGBT), etc.), and several semiconductor materials (Si, SiC, GaN). Furthermore, each specific power device may require a different gate driver and gate driver power supply. The specific features of some power devices may also lead to the modification of the power circuit topology to accommodate the device peculiarities. In summary, a power converter design approach based on the two-level basic building block of Fig. 1(a) leads to a great dispersion in power devices, ancillary circuits, and even main power circuit topologies, at the expense of great engineering efforts and cost, unable to take advantage of scale economies, and lacking a proper level of standardization to obtain highly optimized converter designs.

One then wonders if it would not be more advisable and efficient to find a technical path to build power converter legs from single highly-optimized power-device switching cells at a given voltage rating. A possible path to achieve this goal is to introduce multilevel converter topologies [5]–[9]. Although they involve a higher number of devices and a higher control complexity, multilevel technology allows building power converters with different V_{dc} ratings from a single set of power devices (switch and diode) at a specific voltage rating, by simply adjusting the number of levels. In addition, multilevel topologies offer additional benefits compared to the traditional two-level case:

- 1) Better overall system performance, since the availability of multiple voltage levels at the dc-link may allow a more efficient control of the power flow between systems [10], [11].
- 2) Inherent reduction of output voltage harmonic distortion, leading to lower converter filter size, weight, and filter losses.
- 3) Inherent reduction of switching losses, because switching transitions take place at lower blocking voltage levels and with lower-voltage-rated devices featuring better relative switching performance.
- 4) Wider loss spreading among devices, leading to reduced global heat sink requirements.
- 5) Better leg fault-tolerance capacity, since the failure of one device does not necessarily lead to a full leg shutdown, as is the case with the topology of Fig. 1(a).
- 6) Lower pole voltage dv/dt .
- 7) Lower common-mode voltage.
- 8) Lower electromagnetic noise.

In general, power converters can benefit from these advantages even in low-power and low-voltage applications [12]–[14]. Although it is not strictly the case of a multilevel topology, the work in [15] clearly illustrates some of these advantages by replacing 600-V IGBTs by a carefully designed series connection of sixteen automotive 30-V MOSFETs in a domestic induction heating application.

However, despite their benefits, the current use of

multilevel topologies in industry is often limited to applications where the power converter can only be designed with such technology. For instance, in high-voltage applications, where the lack of a competitive power switch at the proper voltage rating for the two-level topology of Fig. 1(a) forces the use of multilevel techniques. Compared to a two-level topology, the large number of discrete components required to configure the multilevel converter, together with an inefficient use of space due to the lack of a proper level of integration, is seen as a major drawback. In addition, the lack of a proper level of integration also leads to parasitics that degrade the circuit performance and reliability.

To pave the way for the aforementioned possible paradigm shift in power converter design, this paper proposes the introduction of a new device hinging on multilevel technology: the so-called switching-cell array. It consists of a matrix arrangement of highly-optimized switching cells that can be easily reconfigured to produce converter legs with different voltage and current ratings. The aim of the paper is to present this new research line to foster the exploration of this design approach.

The paper is organized as follows. Section II presents the extended multilevel active-clamped (MAC) topology, derived from the MAC topology proposed in [10]. The extended MAC topology serves as the basis to propose a configurable switching-cell array, in Section III, where the switching cell content, switching-cell terminals, and possible switching-cell array configurations are discussed. Section IV presents experimental results on a 6x3 switching-cell array to illustrate and validate this design approach. Finally, Section V presents the conclusions.

II. EXTENDED MULTILEVEL ACTIVE-CLAMPED TOPOLOGY

There are a number of different multilevel topologies [5]–[9]. The basic families are the neutral-point-clamped (NPC), the flying capacitor (FC), and the cascaded H-bridge (CHB). Other topologies have been proposed as a modification or combination of these. In particular, in recent years, there have been significant research efforts to develop topologies with the goal of maximizing the number of levels per number of power semiconductor devices, such as in [16] and [17].

Table I presents a comparison of a few representative topologies in terms of the components they require to implement a five-level three-phase inverter from an available dc bus with voltage V_{dc} . The typical passive NPC (PNPC) topology, also known as diode clamped (DC), is considered for the NPC family. The parameters considered for comparison are the number of voltage-unidirectional and current-bidirectional switches (N_s), the per unit blocking voltage of switches (V_s) (i.e., the blocking voltage divided by V_{dc}), the number of clamping diodes (N_{CD}), the per unit blocking voltage of clamping diodes (V_{CD}), the number of capacitors (N_C), the per unit voltage of capacitors (V_C), the number of independent voltage dc sources (N_{VDC}), the voltage value of the independent dc sources (V_{VDC}), and the number of groups of independent dc sources that require isolation among each other (N_{GIVDC}). Whenever a value applies to only a subset of elements, the number of elements is indicated beside within parenthesis.

TABLE I
COMPARISON OF COMPONENTS REQUIRED TO IMPLEMENT
A FIVE-LEVEL THREE-PHASE INVERTER

Parameter	CHB	[16]	[17]	FC	PNPC
N_S	24	18	18	24	24
V_S	1/4	1/4 (6) 2/4 (12)	1/4 (12) 2/4 (6)	1/4	1/4
N_{CD}	0	0	0	0	18
V_{CD}	---	---	---	---	1/4 (6) 2/4 (6) 3/4 (6)
N_C	0	0	0	9	4
V_C	---	---	---	1/4 (3) 2/4 (3) 3/4 (3)	1/4
N_{VDC}	6	6	6	0	0
V_{VDC}	1/4	1/4	1/4	---	---
N_{GIVDC}	6	3	6	---	---

The CHB topology, the topology from [16], and the topology from [17] require several isolated and regulated dc voltage sources. To implement these dc sources it is necessary to introduce additional custom power converters, involving a number of additional power semiconductor devices and passive components. In particular, transformers are usually necessary to provide galvanic isolation and/or to step down the voltage. In addition, these converters introduce additional power losses to the system. The CHB and especially the topologies in [16] and [17] can produce a remarkably high number of levels by a relatively small increase in N_S . However, this is achieved at the expense of increasing N_{VDC} , the dispersion in V_{VDC} values, the dispersion in the independent dc source power rating values, and the dispersion in V_S values. Note that the voltage rating of the selected devices must be as close as possible to the blocking voltage to minimize the conduction and switching losses. A wide range of V_S values implies the need of employing a wide range of switches with different voltage ratings. In addition, since the number of different voltage rating values of commercial devices is limited, the final selection will probably be suboptimal from the conduction and switching loss point of view. Therefore, in summary, although these topologies can be interesting in specific applications requiring a very high number of levels, it seems difficult to conceive a systematic approach using these topologies together with a few standard components to implement integrated, compact, and economic converters for a wide range of applications and operating conditions.

As for the FC topology, it does not require independent dc voltage sources, but needs a large number of bulky capacitors within each converter leg.

As for the PNPC topology, it also does not require independent dc voltage sources. It only needs power semiconductor devices to implement the converter legs. Four dc-link capacitors are needed to generate the five voltage levels from the dc bus, but these capacitors are shared by all converter legs and can be very small if the converter is properly operated. Thus, NPC-type topologies offer the potential for a highly integrated implementation.

Among the different NPC topologies, the MAC topology,

shown in Fig. 2, is particularly interesting because it is built from only a pyramidal connection of power switches with antiparallel diode, all at the same voltage rating. It represents a natural extension and replacement of the two-level topology of Fig. 1(a) without the need to introduce internal passive components (capacitors or inductors), thus with a potential for a high-level of integration and compactness. The leg presents one pole terminal (p) and n dc-link terminals (dc₁, dc₂, ..., dc_n), where n is the number of converter levels. A capacitor or a voltage source is connected across every two adjacent dc-link terminals, being the dc voltage of each of these components typically the same ($v_{dc}/(n-1)$). The leg behaves as a single-pole n -throw switch allowing the connection of the leg pole terminal to each of the n dc-link terminals. The topology operating principle and features have been presented in [10]. It is guaranteed that each device blocking voltage is equal to the voltage across adjacent dc-link terminals, the pole terminal current (i_p) typically flows through several parallel paths reducing and distributing conduction losses, and there is certain degree of freedom to distribute switching losses among devices. The transitions between adjacent switching states (between the connection to dc_k and the connection to dc_{k+1}) require changing the state of n switches: k diagonal switches turn on (or off) and $n-k$ diagonal switches turn off (or on). If $i_p > 0$, switching losses concentrate on the first blue device turning on or the last blue device turning off, with reference to Fig. 2. If $i_p < 0$, switching losses concentrate on the first orange device turning on or the last orange device turning off.

The feasibility of configuring power converters from MAC legs has been experimentally demonstrated in dc-dc converters with and without galvanic isolation [10], [18], and in single-phase and multiphase dc-ac converters [10], [19]. In case the dc-link is formed by a simple series-connection of capacitors, keeping their voltage balanced is feasible if a proper pulsewidth modulation and closed-loop control is used [10], [18], [19]. Thus, MAC legs can be used to build all types of power converters: dc-dc, dc-ac, and ac-ac, with and without galvanic isolation, and with bidirectional power flow.

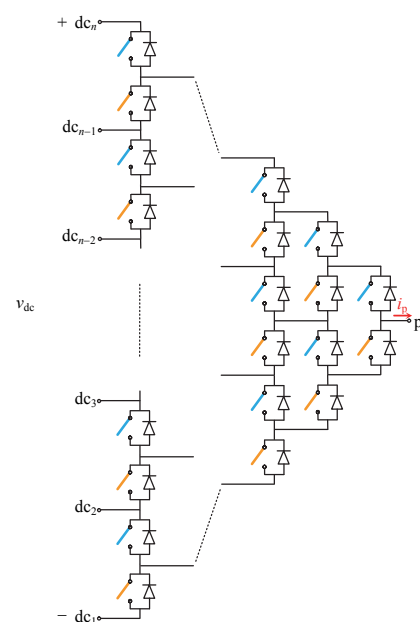
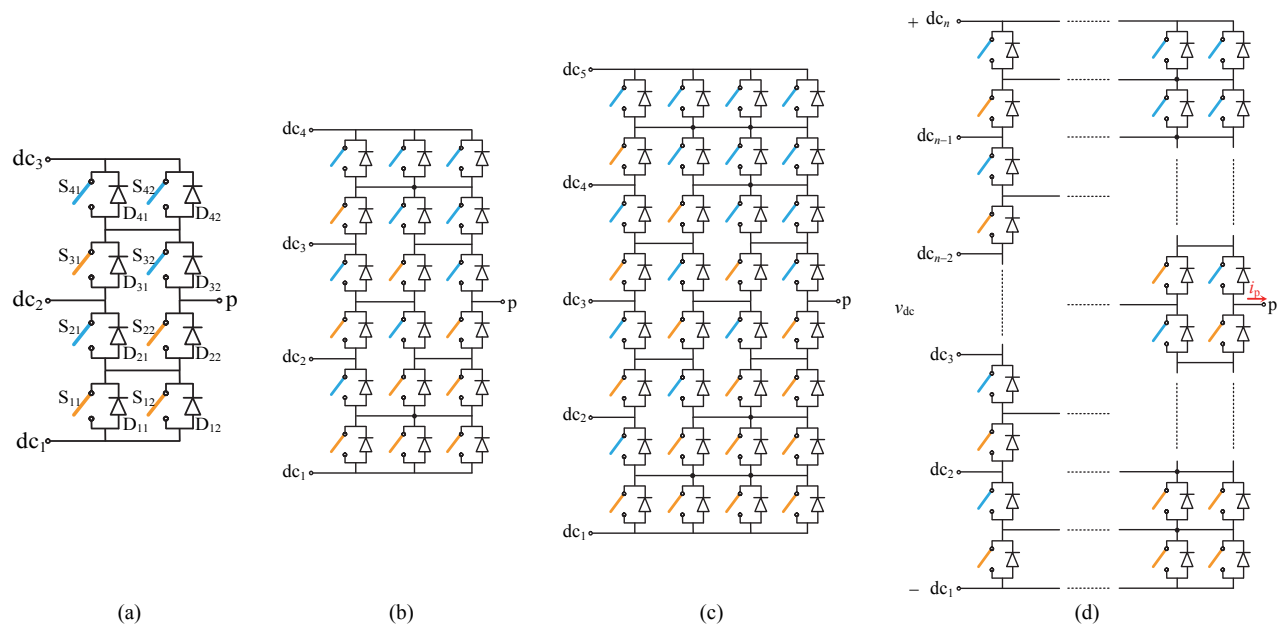
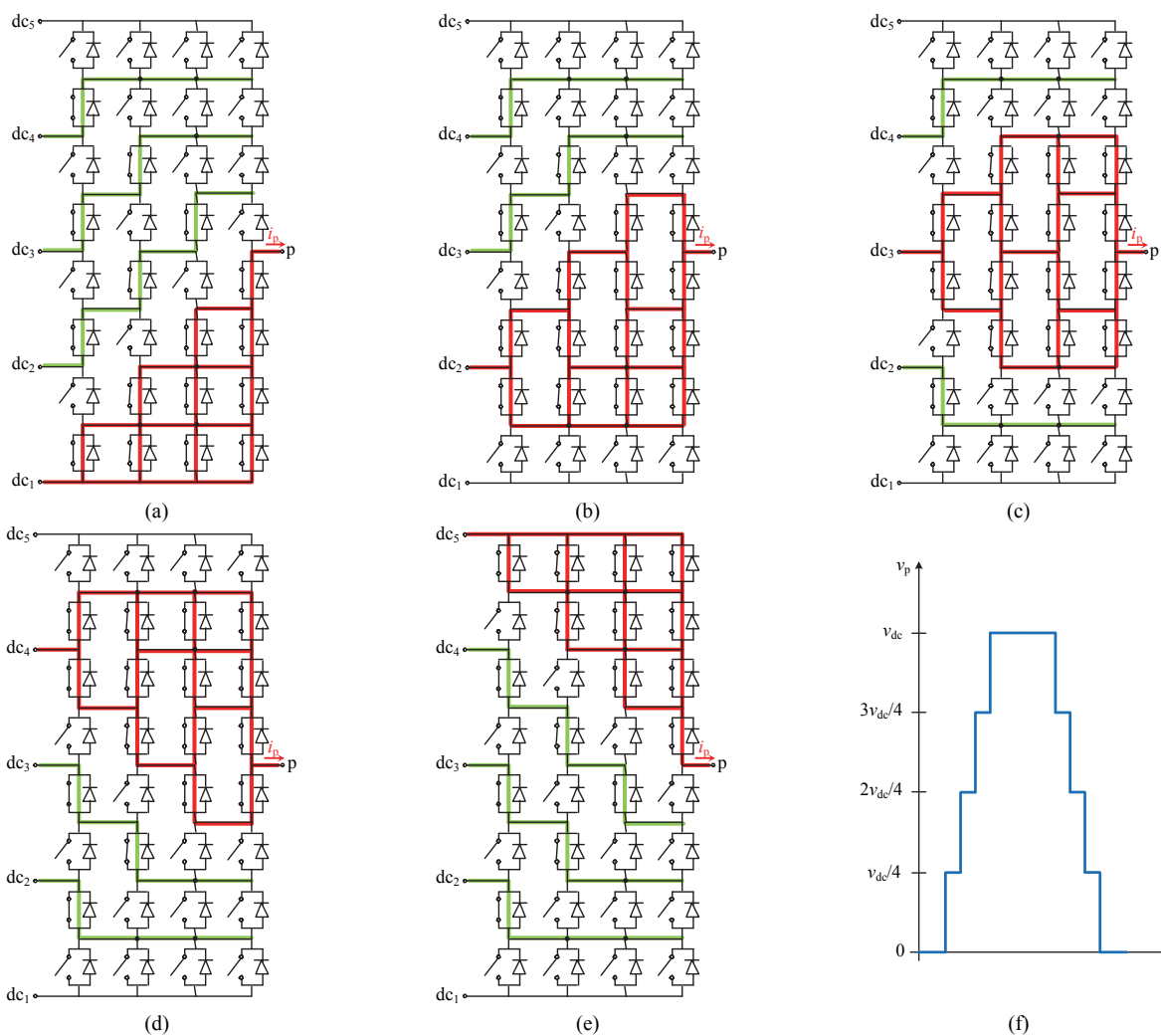


Fig. 2. MAC topology (n levels) [10].

Fig. 3. Extended MAC topology. (a) Three level. (b) Four level. (c) Five level. (d) Generalization to n levels.Fig. 4. Switching states of a five-level extended MAC leg. (a) Connection to terminal dc_1 . (b) Connection to terminal dc_2 . (c) Connection to terminal dc_3 . (d) Connection to terminal dc_4 . (e) Connection to terminal dc_5 . (f) Pole terminal voltage pattern.

With the aim to overcome the limitations of the basic MAC topology, an extension of this topology is proposed in Fig. 3. The extension consists in incorporating additional devices in parallel with the outermost devices of Fig. 2. This reduces the conduction losses in the connection to the outer dc-link terminals, which are typically the connections with the highest duty ratio, and increases the degree of freedom to distribute the switching losses.

Fig. 4 illustrates the switching states of the five-level case. Red lines indicate the paths followed by the pole terminal current i_p . Green lines indicate the connections enforced by the on-state switches that guarantee a proper blocking voltage of the off-state devices. It can be observed that all connections of the pole terminal to the dc-link terminals present more than one path to conduct the pole current. This will produce lower conduction losses compared to the basic MAC topology.

It can also be observed that the transitions between adjacent switching states now require changing the state of $2n-2$ switches: $n-1$ switches turn on and $n-1$ switches turn off. As before, switching losses will concentrate on the first device turning on or the last device turning off, depending on the i_p direction. This increases the degree of freedom to distribute switching losses, especially in transitions involving the connection of the leg pole to the outer dc-link terminals, enabling a better distribution of switching losses.

III. SWITCHING-CELL ARRAYS

The extended MAC topology serves as the basis to conceive a flexible device from which converter legs with a range of voltage and current ratings can be obtained. The device, referred here as a switching-cell array (SCA) and depicted in Fig. 5, consists of a matrix arrangement of axb isolated switching cells (SCs) on a common package designed to efficiently transfer heat to a common heat sink. Each SC presents an interface with at least two power terminals (pt_1 and pt_2) and an input switch control signal (scs). The features and versatility of the SCA defined above are presented and discussed in the following subsections.

A. The Switching Cell

The SC is defined with the aid of the basic block diagram of Fig. 6(a). The SC contains a controlled switch with antiparallel diode, an isolated gate driver (GD), and a gate-driver power-supply (GDPS) circuit. The switch and diode should have the same voltage rating. The GDPS circuit should provide the power required by the GD at a suitable voltage level from the voltage across and current through the SC power terminals (pt_1 and pt_2). In its most basic form it is a unipolar power supply, although some devices may require or benefit from a bipolar power supply. Fig. 6 considers the unipolar case. The GD should receive as input the switch control signal (scs) that determines the desired state of the controlled switch. Thus, the interface of each SC should at least consist of two main power terminals and an input signal to command the switch state. Additional input signals could be sent to the SC; e.g., to enable the SC operation. Additional output signals could be sent from the SC informing of its operating status. All input and output signals could be delivered through optical or electrical means. If they are delivered electrically, SC internal isolation through an optocoupler or other means is necessary.

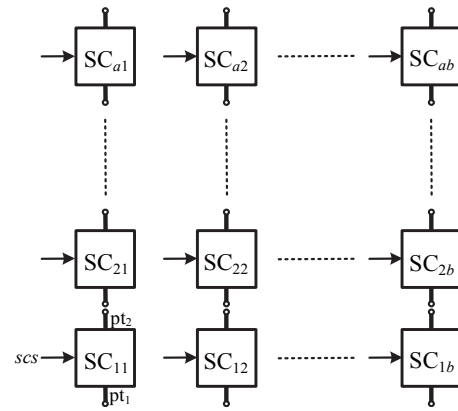


Fig. 5. An axb SCA.

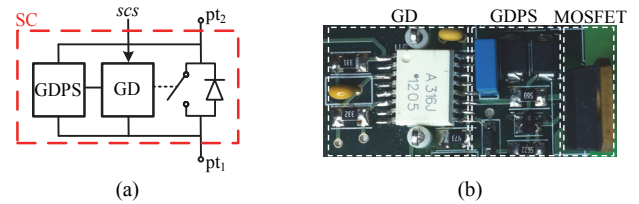


Fig. 6. Switching cell. (a) Basic block diagram. (b) Example of a 100-V-rated SC built with commercial discrete components on a printed circuit board.

Fig. 6(b) shows an example of a possible SC circuit built with commercial discrete components around a 100-V MOSFET. Most of the components involved are semiconductor components, with a potential to be highly integrated and produce compact SCs. In fact, the monolithic integration of Fig. 6(b) GDPS circuit within the MOSFET die has already been demonstrated in [20]. Further discussion on these integrable GDPS circuits can be found in [21]–[23]. On the other hand, the monolithic integration of a GD and a GaN transistor is already a reality and it is feasible to integrate multiple power devices together with their GD and ancillary circuitry on a single chip thanks to the lateral structure of GaN transistors [24].

B. Switching-Cell Array Configurations

Let us assume the simplest scenario where a $(2n-2) \times (n-1)$ SCA is to be used to implement a single converter leg. Through establishing proper connections among the SCs power terminals, the SCA can be configured to operate with a number of levels from 2 to n . Thus, the leg voltage rating can be adjusted to match the dc-link voltage of the application. Fig. 7 shows an example of the possible configurations of an 8×4 SCA, with 32 SCs. Each elementary SC is designated with a two-digit number specifying its position (row-column) within the matrix arrangement. Fig. 7(a) shows the required SC power-terminal connections to produce a five-level leg. Through establishing the parallel connections of SCs indicated with blue stripes in Fig. 7(a), and then rearranging the SC power-terminal connections, the four-level configuration of Fig. 7(b) is achieved. In Fig. 7(b), some of the new aggregated SCs (square boxes) are conformed by several elementary SCs in parallel. In particular, this is the case of the SCs involved in the connection of the pole terminal to the outer dc-link terminals. Since these connections usually present the highest duty ratio, the paralleling of elementary SCs will help increase

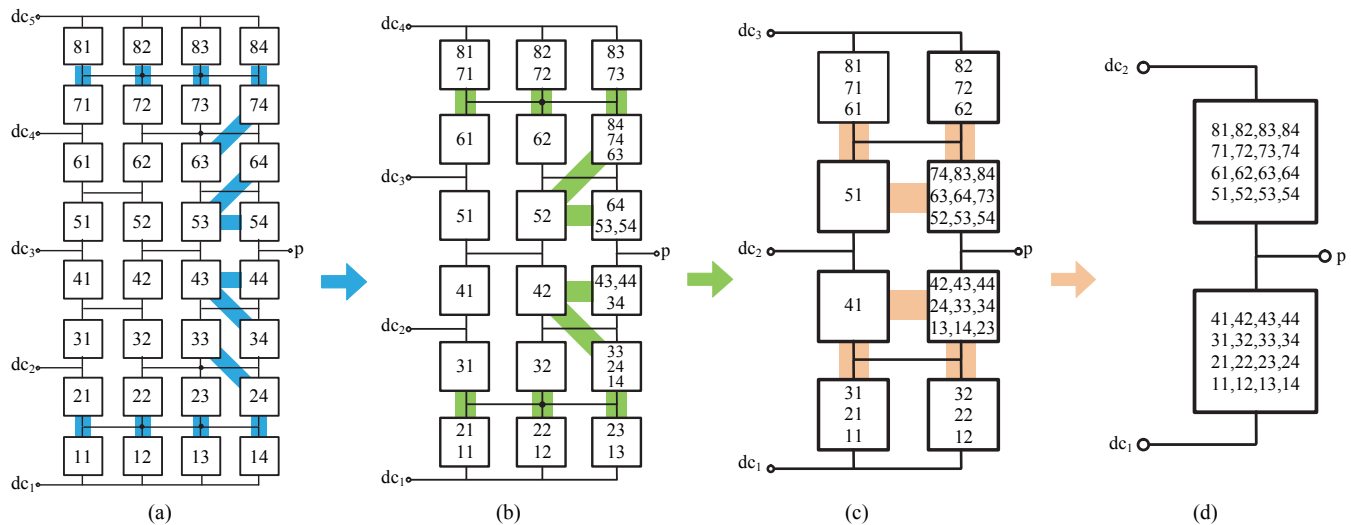


Fig. 7. Possible configurations of an 8x4 SCA. All SCs within a square box are connected in parallel. (a) Five-level leg. (b) Four-level leg. (c) Three-level leg. (d) Two-level leg.

the leg current rating compared to Fig. 7(a). Therefore, in summary, the transition from the configuration of Fig. 7(a) to the configuration of Fig. 7(b) produces a decrease of leg voltage rating and an increase of leg current rating. The reconfiguration to three and two levels follows a similar approach and is illustrated in Fig. 7(c) and Fig. 7(d). Note that the parallel connections of SCs indicated with colored stripes in Figs. 7(a)-(c) follow a specific pattern and are always established among nearby SCs.

Other approaches different from the one shown in Fig. 7 to establish the parallel connections among SCs to transition to a lower number of levels are also possible. The optimum approach will depend on the leg operating conditions determined by the application. For instance, in Fig. 7(c), SC₄₁ and SC₅₁ do not present other SCs in parallel because it is assumed that the duty ratio of the leg connection to dc₂ is small and that the leg is operated to force soft-switching transitions in SC₄₁ and SC₅₁. Thus, these two SCs will experience low average conduction losses and no significant switching losses, presenting a low thermal stress. Under this scenario, the probability of a failure of these switching cells is low. In addition, if either SC₄₁ or SC₅₁ fail in open circuit, the leg can continue operating as normal connecting the pole terminal to any of the three dc-link points, thanks to the redundant paths that the topology offers. However, if the fault tolerance capacity of the positions occupied by SC₄₁ and SC₅₁ in Fig. 7(c) is of concern for any reason, other SCA configurations can be implemented to produce a three-level leg with two, three, or more SCs in parallel in these two positions.

C. Discussion

A $(2n-2) \times (n-1)$ SCA is therefore a configurable device that allows implementing single-pole multiple-throw converter legs with adjustable voltage and current ratings. As n increases, the leg power rating, the leg dc-link voltage rating range, and the leg output current rating range increase.

Companies involved in the design of power converters often accumulate a large experience using a given transistor and associated auxiliary circuitry (gate driver, etc.). This transistor

may have an excellent merit factor per cost. Their expertise in using such transistor and auxiliary circuitry allows the designer to quickly generate new designs using this circuitry with a high degree of confidence that the expected results regarding performance, robustness, and reliability will be met in very few iterations. In addition, since the company acquires these devices in large quantities, their cost is very low. In this context, the SCA, conceived from the extended MAC topology, enables a systematic approach to build power converters from a single transistor. Compared to other multilevel topologies such as the modular multilevel (MM) or the flying capacitors, the advantage of the extended MAC topology is that the converter legs only contain power semiconductor devices with no internal inductors or capacitors. Thus, highly compact leg implementations can be achieved. This leads to a very compact implementation of the complete conversion stage, particularly in applications with inherent filtering, such as in motor-drive inverters, where the stator winding inductance already acts as a filter and only a series-connection of a reduced set of small capacitors is required to form the dc-link, shared by all converter legs. In addition, the converter control is simpler than in a MM converter, from the point of view that there is no need to balance the multiple leg internal capacitor voltages and control the leg circulating currents. The converter core is formed by a set of single-pole multiple-throw switches and the control only needs to determine the position of each leg at every point in time to synthesize the desired leg pole voltages while keeping the dc-link capacitors balanced.

In general, at a conversion stage level, the proposed design approach allows the decoupling of the power converter switching function and the power converter energy storage/filtering/scaling/isolation function into only two or three separate homogeneous physical blocks. The SCA allows implementing the switching block with an array of switching cells implemented on semiconductor material. At each side of the switching block there could be a passive block in charge of implementing the energy storage/filtering/scaling/isolation functions combining magnetic, dielectric, and conductor materials. The current technology allows achieving a high

level of integration and compactness in the implementation of both types of blocks (e.g., monolithic chips in the semiconductor block and integrated inductor-capacitor-transformer structures in the passive block). In addition, a minimum number of interconnections between blocks of different nature are required, thus saving space and cost. Multilevel converter topologies such as the MM need to mix power semiconductor devices and passives into the converter legs. In this case, the achievable level of integration and compactness is typically lower because significant space must be employed and significant empty spaces must be left in the multiple interconnections among heterogeneous components. Therefore, the proposed approach offers the potential of a higher converter power density.

However, in a MM converter, the number of power semiconductors increases linearly with the number of levels, while in the proposed approach the number of power semiconductors increases quadratically. Therefore, for a high number of levels, if the complexity regarding the number of transistors is to be kept at a reasonable level, the MM topology is the most competitive.

On the other hand, the proposed converter design approach may also easily bring additional advantages at a system level in several applications; e. g., in battery-powered systems. Using only several instances of two different components (a battery pack with a nominal voltage of x V and an SCA with SCs rated at $1.5x$ V), we can configure different systems with different dc-link and load voltage ratings. Compared to a conventional two-level converter design, this avoids the need of designing non-standard battery packs with nominal voltages $2x$, $3x$, etc., where the battery management system would be more complex (in particular, the subsystem in charge of balancing the internal series-connected battery cells). In the system configurations of Fig. 8(a), a standard x -V battery pack can be used in all cases, and the charge balancing among battery packs can be controlled very efficiently by the SCA-based converter itself, through simply extracting more energy from those battery packs with a higher state of charge in battery-discharging mode and through delivering more energy to those battery packs with a lower state of charge in battery-charging mode. In addition, the system in Fig. 8(a) also benefits from the inherent advantages of multilevel conversion: low harmonic distortion, low switching losses, small heat sink, low common-mode voltage, fault-tolerance capacity, etc. Another example of applications where the proposed SCA-based converter design approach can be especially beneficial is in photovoltaic systems. As illustrated in Fig. 8(b), a range of possible system configurations can be arranged from several instances of two components (a photovoltaic array with a nominal voltage of x V and an SCA with SCs rated at $1.5x$ V) in order to match the load voltage rating. Here, besides the possibility of configuring several systems at different voltage ratings from only two components, the multilevel converter structure allows operating each photovoltaic array at its maximum power point, even at different solar irradiance levels among photovoltaic arrays. This is not possible if all photovoltaic arrays were connected in series in a conventional two-level converter configuration.

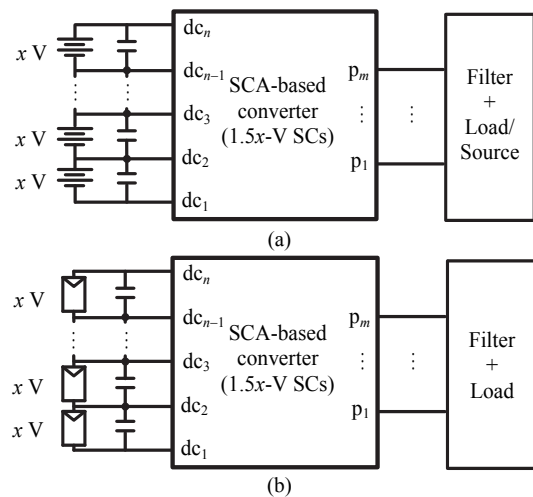


Fig. 8. Configurations of a battery-powered system and a photovoltaic system for applications with different voltage ratings. (a) Battery-powered system, built upon several instances of an x -V battery pack and an SCA with SCs rated at $1.5x$ V. (b) Photovoltaic system, built upon several instances of an x -V photovoltaic array and an SCA with SCs rated at $1.5x$ V.

According to the extended MAC topology, the number of SCs required by an SCA to be able to implement a converter leg with n levels is $2 \cdot (n-1)^2$. Thus, the maximum number of levels should be limited to keep the number of SCs at a reasonable value. In order to be able to implement converter legs for a wide dc-link voltage range with a reasonable number of levels, SCs could be developed at a few different voltage ratings. Popular voltages classes (30 V, 100 V, 600 V, etc.) could be selected to take advantage of the existing expertise and produce optimized SCs at these ratings. For example, assuming that the number of levels is limited to five and that cell voltage rating must exceed 50% of its blocking voltage, Fig. 9 presents a plot indicating the most appropriate SC and number of levels for a range of application dc-link voltages up to 1600 V.

According to the extended MAC operation described in Section II and the SCA configurations described in Section III.B, the SC should have good paralleling features and should ideally fail as an open-circuit, to maximize the leg fault-tolerance capacity.

An SCA could be produced from a single SC with a good balance of conduction and switching performance or it could be produced from two SCs: one optimized for switching and one optimized for conduction. In the former case, the cost of fabricating the SCA will be expected to be the minimum, but a proper switching strategy should be designed to conveniently

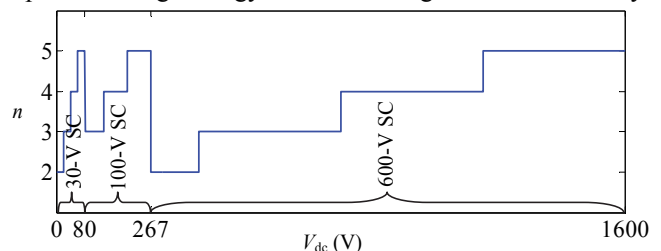


Fig. 9. Optimum SC selection and number of levels for a range of possible application dc-link voltages V_{dc} . It is assumed that 30V-, 100V-, and 600V-SCs are available, that the maximum practical number of levels is five, and that the SC voltage rating must exceed 50% of its blocking voltage.

distribute the switching losses among the SCs. In the latter case, the first SCA column could be populated with SCs optimized for switching while the rest of SCs would be optimized for conduction. This configuration, together with a switching strategy that concentrates the switching losses in the SCs of the first SCA column, would produce the highest efficiency, although it could lead to an unbalanced SC thermal stress.

A large number of SCs implies a large number of switch control signals. However, some SCs may share the same control signal. In the simplest control strategy of an n -level extended MAC leg, only $2n-2$ independent control signals are required. In the most complex control, $(2n-2) \cdot (n-1)$ independent control signals are required, one for each SC. In any case, the management and processing of the multiple SC control and monitoring signals can be easily performed with a field-programmable gate array (FPGA).

Finally, two different SCA implementation approaches can be envisioned. In a first approach, the SCA could be prefabricated and stored by the device manufacturer and then, at a later stage, configured with an additional metallic layer upon the customer needs, and packaged so that only the switch control signal pins and main leg power terminals are accessible to the user. This approach would lead to a high compactness. In a second approach, the device manufacturer could produce a module with all the SC power terminals and control pins accessible, so that the user can configure the SCA with proper connections among SC power terminals. This approach would lead to low device manufacturing cost due to scale economies and the resulting device could be referred as a field-configurable SCA (FCSCA).

From all the above, it can be concluded that the design of power converter legs based on SCAs offers several degrees of freedom and opens a range of research topics to explore the potential of this approach: optimal SC design, optimal diversity of SCs, optimal SCA configuration options, optimal switching strategy for homogeneous loss distribution, etc.

IV. EXPERIMENTAL RESULTS

The extended MAC topology presented in Section II contains higher number of semiconductor devices than conventional multilevel topologies. This increases the control complexity but brings some advantages, as discussed in Section II. To illustrate one of these advantages, the thermal performance of a three-level three-phase IGBT-based dc-ac inverter operating at unity power factor under the PNPC (DC), active-NPC (ANPC), and the extended MAC topology has been compared. The leg switch and diode nomenclature is defined in Fig. 3(a).

Table II presents the three pairs of 600-V-rated TO-220-package IGBTs and diodes considered for the implementation of the inverters, together with their characteristic parameters at a reference current of 15 A: the IGBT collector-to-emitter voltage drop V_{CE} , the diode forward voltage drop V_F , and the total switching loss E_{sw} (hard turn-on loss plus hard turn-off loss under inductive load). The first pair of devices presents a balanced conduction and switching performance. They are classified as standard devices (stn). The second pair of devices presents a good switching performance at the expense of a

degraded conduction performance. They are classified as devices optimized for switching (ops). The third pair of devices presents a good conduction performance at the expense of a degraded switching performance. They are classified as devices optimized for conduction (opc). The PNPC and ANPC topologies have been configured with the stn IGBT and diode. Instead, the extended MAC topology has been configured with a combination of ops and opc devices: ops devices for the first column (S_{11} , S_{21} , S_{31} , S_{41}) and opc devices for the second column (S_{12} , S_{22} , S_{32} , S_{42}). According to the discussion of Section III.C, the three-level extended MAC leg is then operated to concentrate hard-switching losses on the first column, while the devices in the second column mainly experience only conduction losses.

Fig. 10 presents the thermal image of one converter leg of each topology at the same operating conditions in steady state. The IGBTs and diodes are each attached to an individual heat sink, so that the heat sink temperature reveals the device individual losses. Fig. 10(a) corresponds to the popular PNPC case. All four IGBTs present a high temperature. Introducing two additional IGBTs (S_{21} and S_{31}) in the ANPC topology helps reduce the losses and thermal stress of S_{22} and S_{32} . However, the stress of the most critical devices (S_{11} and S_{41}) cannot be relieved by the introduction of S_{21} and S_{31} . In Fig. 10(c), the introduction of two additional IGBTs (S_{12} and S_{42}) helps relieve S_{11} and S_{41} , so that all devices present a moderate loss and thermal stress. This brings a better loss distribution and allows a significant increase of the leg power rating compared to the PNPC and ANPC case.

Fig. 10 also presents the loss breakdown per switching cell of the three topologies. The average power loss of each switching cell is defined as the combined loss of the corresponding IGBT and diode, which have been calculated from the measured values of the heat sink temperature, ambient temperature, and the value of the heat-sink-to-ambient thermal resistance ($R_{th,h-a}$). The average loss for a full leg, calculated from the measured leg input and output voltage and current values following the procedure explained in [25], is 32 W for the PNPC topology, 30 W for the ANPC topology, and 22 W for the extended MAC. Overall, the extended MAC topology features a lower loss and thermal stress of the critical switching cells, and lower total losses.

Table III presents the leg current rating, obtained through simulation, under the following conditions: $V_{dc} = 600$ V, $V_{p,1} = 212$ V_{rms}, unity power factor, $f_s = 28$ kHz, $R_{th,h-a} = 2$ K/W, $T_{amb} = 25$ °C, and a maximum IGBT junction temperature of 175 °C. The simulations have been performed in PLECS, where the relevant power device datasheet curves have been introduced to compute conduction and switching losses [25]. Although the extended MAC topology presents a larger

TABLE II
SELECTED IGBTs AND DIODES

Code	IGBT	V_{CE} (V) ^a	E_{sw} (mJ) ^a	Diode	V_F (V) ^b	E_{sw} (mJ) ^b
stn	IGP15N60T	1.75	0.82	IDP15E60	1.45	0.206
ops	IGP20N60H3	2.00	0.65	IDH12SG60C	3.10	0.004
opc	IGP50N60T	1.10	1.22	IDP45E60	1.05	0.262

^a At $I_C = 15$ A and $T_J = 175$ °C

^b At $I_A = 15$ A and $T_J = 125$ °C

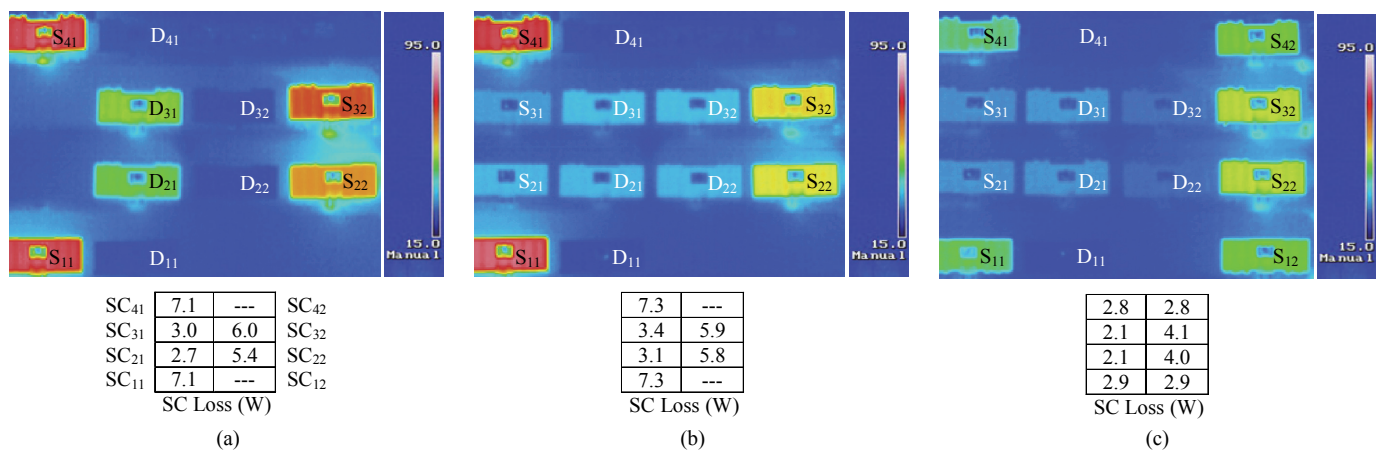


Fig. 10. Experimental device loss and thermal stress in a leg of a three-level three-phase IGBT-based dc-ac inverter under the following conditions: $V_{dc} = 600$ V, fundamental component of the leg output voltage $V_{p,1} = 170$ V_{rms}, unity power factor, leg output power $P_p = 1.23$ kW, $f_s = 30$ kHz, and $T_{amb} = 22$ °C. (a) PNPC (DC) topology, leg power loss $P_{loss} = 32$ W. (b) ANPC (MAC) topology, $P_{loss} = 30$ W. (c) Extended MAC topology, $P_{loss} = 22$ W.

number of IGBTs per leg and a larger total leg power semiconductor area (the total chip area of IGBTs and diodes), the topology features a higher leg current rating per switch and a higher leg current rating per unit of semiconductor area. The values of these merit factors suggest that the extended MAC topology grants a better use of the semiconductor devices.

To illustrate the proposed design approach, a 6x3 FCSCA has been designed and implemented. The main design goal was to produce a prototype to conveniently investigate the device electro-thermal performance under several configurations in a laboratory environment, rather than to produce a device to be used in practice. Fig. 11(a) shows the top of the SC, with the selected 100-V MOSFET (IRFR4510) in a DPAK package. The drain is attached to a 10 cm² (1.5 in²) 70 μm (2 oz) copper surface for heat sinking purposes under natural convection. This surface will also allow the measurement of the case temperature through an infrared camera. Both the drain (D) and the source (S) are connected to power pins. Fig. 11(b) shows the bottom of the SC, with the self-powered GD circuit. Two GDPS circuits are available. GDPS1 generates the positive GD power supply voltage to turn on the device, while GDPS2 generates a negative GD power supply voltage to turn off the device. Since the selected MOSFET can be safely turned off with a zero gate voltage, GDPS2 has been disabled in the experiments. Figs. 11(c) and 11(d) show the top and bottom views of the 6x3 FCSCA board, with a matrix arrangement of 18 isolated SCs. The 18 switch control signals are provided through two IDC connectors on the right of Fig. 11(d). These control signals will be generated with two DS5101 digital waveform output boards, each containing an FPGA, from a dSpace control platform. The SCA can be configured to operate as a two-, three-, and four-level leg through the three base boards in Figs. 11 (e)-(f) equipped with power pin sockets. Figs. 11(h)-(i) show the top and bottom views of the SCA assembled into the four-level base board. In Fig. 11 (i), the 10 mm x 15 mm rectangular holes in the base board, located right above each drain copper surface, conveniently allow the simultaneous measurement of the SCs temperature with an infrared camera. All presented thermal images correspond to the view depicted in Fig. 11(i).

The FCSCA has been successively assembled into the two-, three-, and four-level base boards and then tested with 50 V dc power supplies across adjacent dc-link terminals, a series R-L load connected between p and dc₁ terminals, the same duty-ratio of connection to all available dc-link points, and a switching frequency of 20 kHz. In addition, the load resistance has been adjusted in every test to produce a constant average leg output power (P_p) approximately equal to 300 W. The resulting leg pole voltage and current is shown in Fig. 12 for the three cases. With reference to Fig. 1(a) and Fig. 3, since $i_p > 0$, blue devices will have to withstand switching losses. For the sake of simplicity, the test results presented in Fig. 12 have been obtained alternating in every switching cycle the device that takes the switching losses among all possible candidates. The thermal images after five minutes of continuous operation are also presented in Fig. 12. It can be observed that the average ($T_{SC,av}$) and maximum ($T_{SC,max}$) SC temperatures are similar in all three cases, despite operating at different leg voltage and current levels. Thus, operation at a given power rating with a range of voltage and current ratings and with a similar thermal performance is feasible. However, certain dispersion in SC temperature values can be observed ($T_{SC,\sigma}$ indicates the standard deviation of the SC temperatures). This is partly due to the fact that switching losses must occur in blue devices, while orange devices are free from switching losses. But through a proper distribution of switching losses, a more homogeneous temperature distribution of SCs could be achieved. The optimal distribution will depend on several factors: direction and value of i_p current, duty-ratio values, circuit layout, thermal conditions, etc. To prove the capability of distributing switching losses among SCs, Fig. 13 presents

TABLE III
TOPOLOGY COMPARISON

	PNPC (DC)	ANPC (MAC)	Extended MAC
Number of switches per leg	4	6	8
Leg current rating (A_{rms})	17	17	55
Leg current rating per switch (A_{rms})	4.25	2.83	6.88
Leg current rating per unit of power semiconductor area (A_{rms}/mm^2)	0.29	0.24	0.33

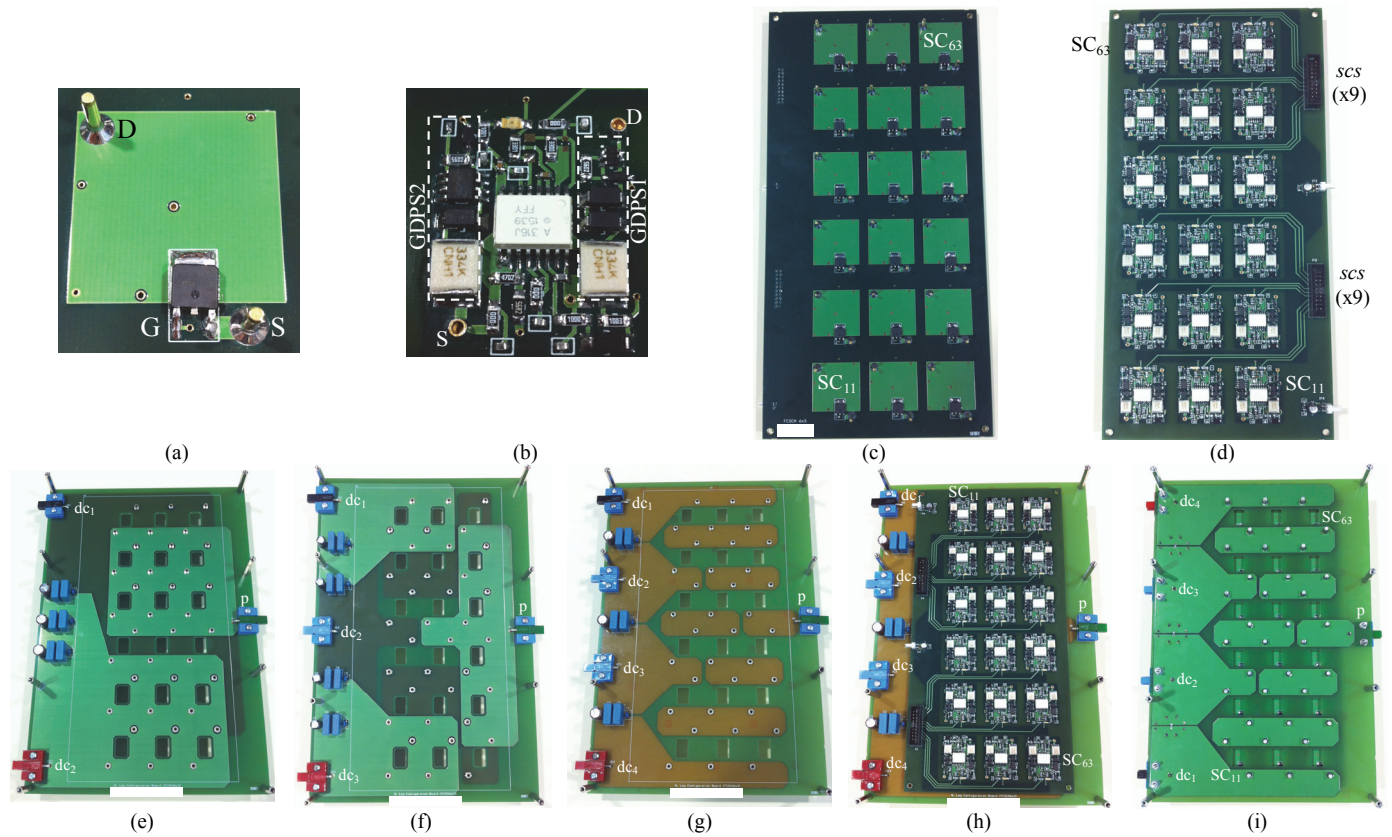


Fig. 11. Experimental prototype. (a) SC top. (b) SC bottom. (c) 6x3 FCSCA top. (d) 6x3 FCSCA bottom. (e) Base board to configure the SCA as a two-level leg (top). (f) Base board to configure the SCA as a three-level leg (top). (g) Base board to configure the SCA as a four-level leg (top). (h) The SCA plugged into the four-level base board (top). (i) The SCA plugged into the four-level base board (bottom).

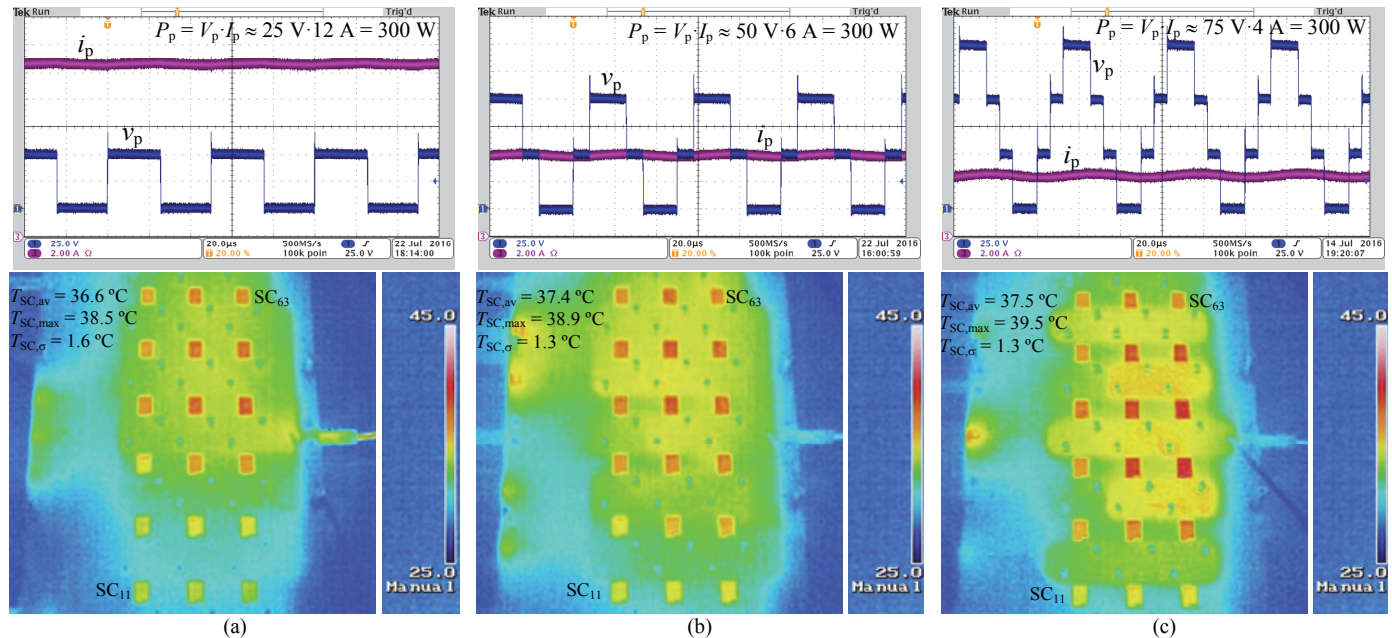


Fig. 12. Experimental results under the following conditions: $V_{dc,k+1} - V_{dc,k} = 50$ V, $P_p = 300$ W, $f_s = 20$ kHz, and $T_{amb} = 27$ °C. (a) Two-level leg configuration. (b) Three-level leg configuration. (c) Four-level leg configuration.

the results in a four-level configuration when the switch control signals are generated so as to concentrate switching losses in the left column of switching cells. Compared to Fig. 12(c), some of the devices from the right and center columns are less stressed, while the temperature of the blue devices in the left column (SC_{21} , SC_{41} , and SC_{61}) has increased.

V. CONCLUSION

This paper has proposed a novel device, an SCA, to enable a possible paradigm shift in the design of voltage-source power converters. The SCA consists of a matrix arrangement of highly-optimized switching cells at a specific voltage rating

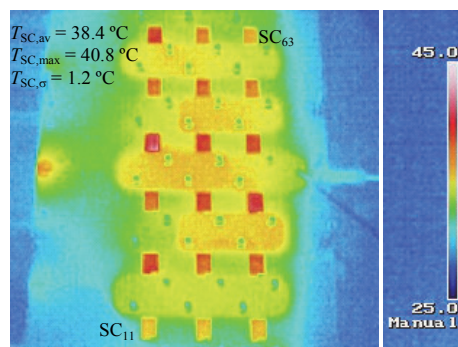


Fig. 13. Experimental results under the same conditions of Fig. 12(c), but concentrating switching loss in the left column of SCs (SC_{21} , SC_{41} , and SC_{61}).

and can be configured to produce converter legs with different voltage and current ratings, hinging on multilevel technology. The SCA allows replacing the conventional two-level legs, which rely on different devices, GDs, and GDPs tailored to the leg voltage rating and specific operating conditions. It is potentially capable of taking advantage of scale economies to reduce the leg cost, and takes advantage of the inherent benefits of multilevel technology. The underlying concept is analogous to the concept that led to the advent of GA and FPGA in microelectronics: a device with multiple isolated basic building blocks that can be later configured (interconnected) in different ways to perform different functions. While GAs and FPGAs allow building different information processing circuits, SCAs and FCSCAs would allow building power converter legs with different voltage and current ratings.

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