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Modelling phase interactions in the dualinterleaved buck converter using samplerdecomposition

Alejandro Villarruel-Parra, and Andrew J. Forsyth, Senior Member, IEEE.

Abstract— The averaged small-signal model of the dualinterleaved buck converter is extended to include the phase interaction effects that arise from the interleaved sampling of the phase currents. Sampler decomposition techniques are used to extend the averaged model, revealing a slow-scale instability that can place significant restrictions on the choice of controller parameters. The model is confirmed by simulations and measurements using a 60kW dual-interleaved prototype with Inter-Phase Transformer (IPT), however the analysis is equally applicable to interleaved converters without magnetic coupling.

Index Terms— Average current, control, DC-DC converters, interleaved converters, modelling, small-signal.

I. INTRODUCTION

NTERLEAVING in DC-DC converters is a well-established Ltechnique to increase input and output ripple frequencies, reduce passive component size and spread the thermal load. This technique is used in many applications ranging from low voltage power supplies to the high power converters within an electric vehicle power train [1]–[4]. Individual average phase current feedback is often used to balance the phase-currents in interleaved systems [5]-[8], but can result in phase interaction and instability, which is not predicted by standard averagevalue modelling techniques. The instabilities can be at quite low frequencies, around 1 kHz, and can place significant limitation on the parameters for the phase-current controllers. One approach to analyse these effects is through the extension of the standard average-value model using sampler decomposition techniques [9]. This approach, which was generalized for converters with two or more phases and demonstrated for a dual-interleaved boost converter, has the

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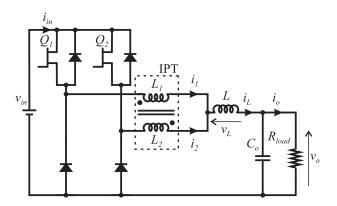


Fig. 1. Dual-interleaved buck converter with inter-phase transformer.

advantage of being more straightforward than the highly detailed sampled-data methods. This papers builds on the work in [9] to show that the modelling technique proposed for the dual-interleaved boost converter can also be applied successfully to the interleaved buck converter in continuous conduction mode, revealing a slow-scale instability that restricts the choice of control parameters. The analysis is presented for a converter with interphase transformer, but is equally applicable to uncoupled converters where similar slow-scale instabilities can arise.

II. SMALL-SIGNAL MODELLING OF INTERLEAVED CONVERTERS WITH AVERAGE-CURRENT MODE CONTROL

A.Small-signal averaged model of the dual-interleaved buck converter

Fig. 1 shows the dual-interleaved buck converter with Interphase transformer (IPT). Assuming continuous conduction operation, then by substitution of the converter switch networks with the averaged PWM switch model [10], the averaged DC and small-signal model shown in Fig. 2 is obtained, where the IPT has been modelled using the windings' self-inductances (L_1 and L_2) and mutual inductance (L_m) [11]. The upper case variables in Fig. 2 denote steady-state components whilst the lower case variables are the small-signal components. D_1 and D_2 are the duty-ratios of Q_1 and Q_2 . Neglecting the DC components of Fig. 2 and under the assumption that the components comprising the converter phases are identical, $L_1 = L_2 = L_c$, the small-signal variations

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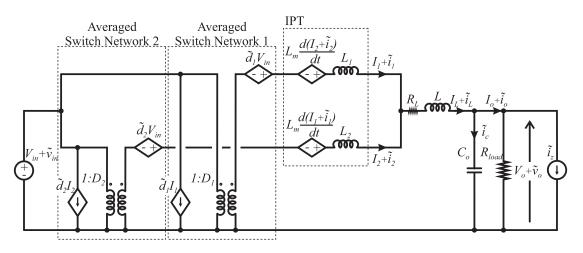


Fig. 2. DC and small-signal model of the dual-interleaved buck converter with IPT.

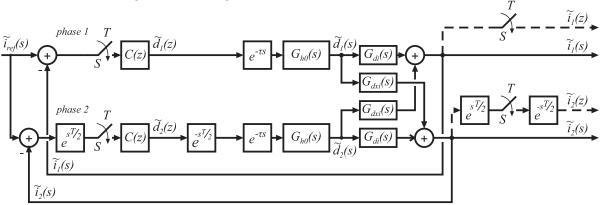


Fig. 3. Block diagram of the dual-interleaved buck converter with IPT with digital average-current mode control.

of the converter phase-currents $\tilde{i}_1(s)$ and $\tilde{i}_2(s)$ can be expressed in terms of the control inputs $\tilde{d}_1(s)$ and $\tilde{d}_2(s)$ as:

$$\tilde{i}_{1}(s) = G_{di}(s)\tilde{d}_{1}(s) + G_{dxi}(s)\tilde{d}_{2}(s)$$
(1)

$$\tilde{i}_{2}(s) = G_{dxi}(s)\tilde{d}_{1}(s) + G_{di}(s)\tilde{d}_{2}(s)$$

$$\tag{2}$$

where $G_{di}(s)$ and $G_{dxi}(s)$ are the converter duty ratio-to-phase current and the converter duty ratio-to-opposite phase current transfer functions which are defined in the Appendix.

B.Small-signal model of the converter with digital average current feedback control

The closed-loop, small-signal model of the dual-interleaved buck converter with digital average-current mode control is shown in Fig. 3. The sampling of the average phase current is represented by the samplers, *S*. Given the symmetry of the converter waveforms in continuous conduction mode, the average phase current can be obtained by sampling once in the middle of the corresponding transistor conduction interval at any point of operation [9, 12, 13]. The phase-shifted operation of the phase-2 sampler with respect to the phase-1 sampler, *S*, is modelled by means of the time delay and advance units, $e^{sT/2}$ and $e^{-sT/2}$ according to the sampler decomposition method [9]. The controllers are represented by C(z), and the computational delay of the control algorithms is modelled by e^{-ts} where $\tau = t_{comp}/T$ and t_{comp} and *T* are the computational delay and the converter switching period respectively. The digital PWM operation is modelled using the zero-order-hold extrapolator transfer function $G_{h0}(s) = (1 - e^{-sT})/s$. The closed-loop reference-to-phase current transfer functions of this system can be found to be:

$$G_{iliref}(z) = \frac{i_{l}(z)}{\tilde{i}_{ref}(z)} = \frac{C(z)G_{di}(z) + C(z)G_{dxi\phi}(z) + C^{2}(z)\left[G_{di}^{2}(z) - G_{dxi\phi}(z)G_{dxi\theta}(z)\right]}{1 + 2C(z)G_{di}(z) + C^{2}(z)\left[G_{di}^{2}(z) - G_{dxi\phi}(z)G_{dxi\theta}(z)\right]}$$
(3)

$$G_{i2iref}(z) = \frac{\tilde{i}_{2}(z)}{\tilde{i}_{ref}(z)} = \frac{C(z)G_{di}(z) + C(z)G_{dxi\theta}(z) + C^{2}(z) \Big[G_{di}^{2}(z) - G_{dxi\phi}(z)G_{dxi\theta}(z) \Big]}{1 + 2C(z)G_{di}(z) + C^{2}(z) \Big[G_{di}^{2}(z) - G_{dxi\phi}(z)G_{dxi\theta}(z) \Big]}$$
(4)

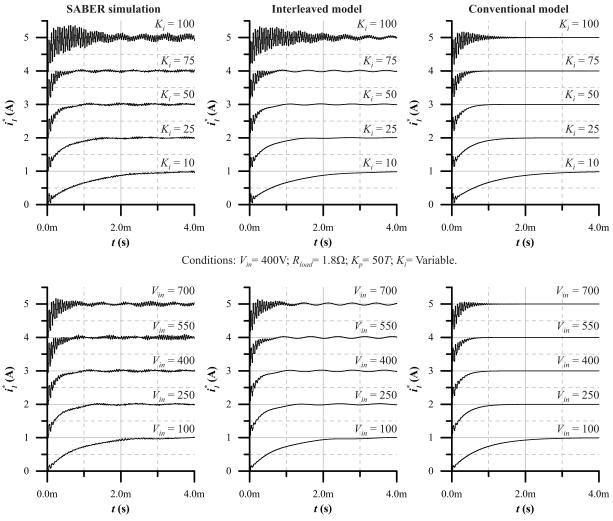
where the z-domain transfer functions $G_{di}(z)$, $G_{dxi\phi}(z)$ and $G_{dxi\theta}(z)$ are obtained using the modified z-transform to account for the fractional time-delay:

$$G_{di}\left(z\right) = \mathcal{Z}_{m}\left\{G_{h0}\left(s\right)G_{di}\left(s\right)\right\}\Big|_{m=1-\left(\frac{\tau}{\tau}\right)}$$
(5)

$$G_{dxi\phi}(z) = \mathcal{Z}_m \left\{ G_{h0}(s) G_{dxi}(s) \right\}_{m=1-\left(\frac{1}{2} + \left(\frac{\tau}{2}\right)\right)}$$
(6)

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Conditions: V_{in} = Variable; R_{load} = 1.8 Ω ; K_n = 25T; K_i = 50.

Fig. 4. Time-domain response of the phase-1 current to small step-increments in the reference input obtained using: the SABER switched model (first column), the interleaved small-signal model (second column) and the conventional small-signal model (third column).

$$G_{dxi\theta}\left(z\right) = z \,\mathcal{Z}_{m}\left\{G_{h0}\left(s\right)G_{dxi}\left(s\right)\right\}_{m=\left(\frac{1}{2},-\left(\frac{\tau}{2},-\right)\right)} \tag{7}$$

The closed-loop reference-to-phase current transfer functions may also be derived assuming non-delayed operation of the samplers in the control-loops, which is the conventional modelling approach [5, 7, 8], resulting in identical transfer functions for each phase since the phases are assumed to have the same component values:

$$G_{i1iref}(z) = G_{i2iref}(z) = \frac{C(z) \left[G_{di}(z) - G_{dxi}(z) \right]}{1 + C(z) \left[G_{di}(z) - G_{dxi}(z) \right]}$$
(8)

where $G_{dxi}(z) = \mathcal{Z}_m \{G_{h0}(s)G_{dxi}(s)\}\Big|_{m=\tau}$.

III. COMPARISON BETWEEN THE INTERLEAVED AND THE CONVENTIONAL MODELS

A. Performance of the phase current to step changes

The set of unit step responses of the phase current, Fig. 4, is used to illustrate the difference between the predictions of the

TABLE I	AND PARAMETER	RS
Component	Symbol	Value
Output inductor	L	5.4 µH
Output inductor stray resistance	R_L	0.029 Ω
IPT self-inductance	L_1, L_2	185.4 μH
IPT mutual inductance	L_m	184.4 µH
IPT coupling coefficient	k	0.995
Output capacitance	C_o	26 µF
Switching frequency	f	75 kHz
Switching/sampling period	Ť	13.33 µs
Computational delay	τ	T/2

interleaved model and the conventional model. The first column of Fig. 4 shows SABER simulation results using a switched model that includes the interleaved sampling of the phase currents in the digital controller. The sample times and sample period (13.33 μ s) were identical in the model and simulations. The second and third columns show the transfer-function predictions from the interleaved, (3), and the

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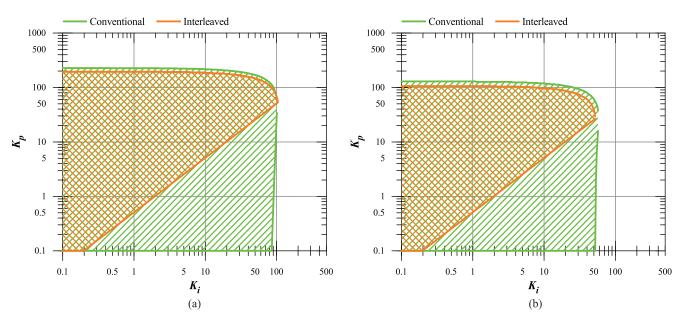


Fig. 5. Comparison of the stability-range predicted by the conventional/non-interleaved model and the interleaved when a digital PI compensator is used to regulate the current-feedback control-loops at (a) $V_{in} = 400 \text{ V}$, $R_{load} = 1.8 \Omega$; (b) $V_{in} = 700 \text{ V}$, $R_{load} = 2.7 \Omega$.

TABLE II					
COMPARISON OF POLES AND ZEROS FROM THE CLOSED-LOOP, REFERENCE-TO-PHASE CURRENT TRANSFER FUNCTIONS*					

Poles		Zeros		
Conventional $G_{iliref}(z)\&G_{i2iref}(z)$	Interleaved $G_{iliref}(z)\&G_{i2iref}(z)$	Conventional $G_{iliref}(z)\&G_{i2iref}(z)$	Interleaved $G_{iliref}(z)$	Interleaved $G_{i2iref}(z)$
0.189±0.864j (16.2 kHz)	0.180±0.872j (16.4 kHz)		0.991±0.095j	0.994±0.098j
0.945	0.993±0.097j (1.16 kHz)	0.760	0.7369	0.752
0.138	0.943	0.5	0.5	0.5
	0.109		0.028	0.061
	0.0510	-0.927	-2.664	-0.472

*Point of operation: $V_{in} = 400 \text{ V}$, $R_{load} = 1.8 \Omega$ with PI controller gains $K_p = 50(T)$ and $K_i = 50$.

conventional, (8), models respectively. SABER and smallsignal models exclude all losses except R_L , the series resistance of the output inductor. The converter parameters are listed in Table I. PI compensators were used to regulate the phase currents. In the first row in Fig. 4, the PI integral gain, K_i , is varied from 10 to 100, and in the second row the input voltage is varied from 100 V to 700 V.

The results from the transfer functions show a close correspondence with the simulation results with virtuallyidentical rise time, natural frequency (16.66 kHz) and damping ratio. However a lower lightly damped natural frequency (ranging from 1 kHz to 1.6 kHz) is evident in many of the responses from the interleaved model, but is completely absent in the conventional model results. The same natural frequency is also observable in the SABER results. The additional high-frequency oscillations that occur in the simulation results were attributed to PWM quantization and current-sampling effects.

B. Pole-zero locations of the system and stability

To illustrate the difference between the conventional and interleaved model transfer functions, the values of the poles and zeros predicted by both models are compared in Table II. The converter parameters used to obtain these results are listed in Table I.

It can be observed that the conventional and the interleaved models have four poles situated in similar locations: two real poles at ≈ 0.94 and ≈ 0.1 , and a pair of high-frequency complex poles at $\approx 0.18 \pm 0.87j$ (≈ 16 kHz). The high-frequency oscillations observed in the step responses are attributed to the latter. Furthermore, the interleaved model contains an additional pair of complex poles, 0.993+0.097j, which are almost cancelled by a pair of complex zeroes present in both the reference-to-phase current transfer functions. These poles are responsible for the low-frequency oscillations observed in the transient responses (≈ 1.1 kHz) and become unstable when the controller gain is chosen to be at least two times larger than the proportional gain.

Finally, the K_p / K_i controller design spaces shown in Fig. 5 are used to illustrate the difference in the stability range predicted by the interleaved model and the conventional model. The dark shaded areas indicate the stable combinations of K_p and K_i predicted by the interleaved model whilst the lighter shaded areas are the additional regions where

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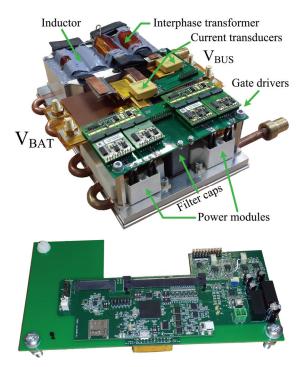


Fig. 6. 60 kW, 75 kHz SiC MOSFET-based dual-interleaved converter and control platform including Texas Instruments TMS320F28377 digital signal controller to regulate the converter phase-currents.

the conventional model suggests that the system operation will be stable. These regions were generated numerically by calculation of the system poles over a systematic sweep of the controller parameters. The patterns are similar to those found in [9] for the dual-interleaved boost converter, and are consistent with the fact that the conventional model over predicts the system stability limits.

IV.EXPERIMENTAL VALIDATION

The experiments were undertaken using a 60 kW, 75 kHz SiC MOSFET-based dual-interleaved converter with input and output voltages up to 700 V and 350 V respectively, Fig. 6. The semiconductor modules used for the prototype power stage are CAS300M12BM2 from Wolfspeed (1200V@300A). The prototype passive component values are listed in Table I.

Two single-sample, average current-mode control-loops were implemented on a Texas Instruments TMS320F28377 digital signal controller to regulate the converter phase-currents, [14]. The sampling instants of each control-loop are strategically positioned in the middle of the transistor on-state intervals to acquire the phase current average value. The controller gains were selected as a compromise between rise-time, overshoot percentage and settling-time, the values used were 0.5 ms, <5% and 2 ms respectively.

To verify the accuracy of the model, the measured response of the converter phase-1 current to a 15 A step-change in the

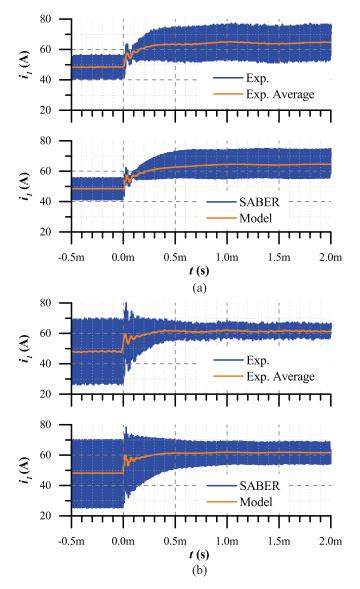


Fig. 7. Experimental and simulated response of i_l to a 15 A step increase in i_{ref} going from 48 A to 63 A for (a) $V_{in} = 400$ V, $R_{load} = 1.8 \Omega$, $K_p = 50(T)$, $K_i = 50$; and (b) $V_{in} = 700$ V, $R_{load} = 2.7 \Omega$, $K_p = 50(T)$, $K_i = 30$. Compensator

gains were selected to achieve $t_{r(10-90)} = 500 \ \mu s$ and overshoot $< 5 \ \%$.

reference was compared to that obtained from switched simulations and the interleaved model, Fig. 7. The waveforms in the top plot, correspond to the measured phase-current and its instantaneous moving average value, whilst the waveforms in the bottom plot are from the SABER simulation and the interleaved model. Fig. 7(a) shows the phase-current response when $V_{in} = 400$ V, $R_{load} = 1.8 \Omega$ and $K_p = 50(T)$ and $K_i = 50$ whilst Fig. 7(b) corresponds to $V_{in} = 700$ V, $R_{load} = 2.7 \Omega$ and $K_p = 50(T)$ and $K_i = 30$. These results show that the model is able to predict the phase current behavior correctly.

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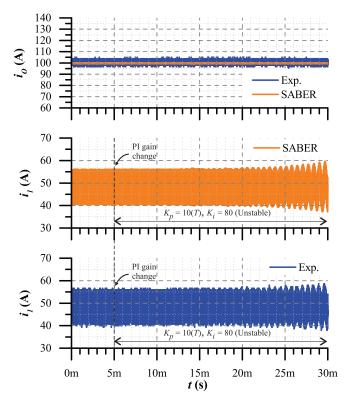


Fig. 8. Experimental response of i_o and i_l to a 15 A step increase in i_{ref} going from 48 A to 63 A using an unstable set of K_p and K_i gains predicted by the interleaved model. $V_{in} = 400 \text{ V}$, $R_{load} = 1.8 \Omega$, $K_p = 1(T)$, $K_i = 30$.

Fig. 8 shows the simulation and experimental results of output current i_0 and phase current i_1 when the converter is switched into an unstable operating condition with $V_{in} = 400 \text{ V}$ and $R_{load} = 1.8 \Omega$. Initially, a stable combination of K_i and K_p were used, later at t = 5 ms the gains were changed to $K_p =$ 10(T) and $K_i = 80$ for both phases. These gain values are predicted to be unstable by the interleaved model for this point of operation, but stable by the conventional model, Fig. 5(a). Notably, the converter output current appears stable despite the instability observed in the phase current. The unstable oscillations appear in both phase currents with the same magnitude, but are out of phase, therefore they are not observable in the converter output current. The converter output voltage was also stable. This suggests phase-current estimation algorithms using a single current sensor, [15]–[17], might not be suitable for interleaved converters with this form of phase current control as they may not detect these phase current instabilities.

V. CONCLUSION

Enhanced averaged modelling using sampler decomposition has been shown to be applicable to the dual-interleaved buck converter with inter-phase transformer using digital averagecurrent control. The predictions of the enhanced model were verified experimentally and by simulation. The analysis showed that a low-frequency natural mode is present in the system that is not predicted by standard average-value models. The natural mode is attributed to the interaction between the phases and can result in low frequency oscillations in the phase currents that are unobservable in the converter input and output currents. K_p / K_i controller design-space plots were generated to aid in the visualization of the stability of the system and with the PI parameter selection. These plots are similar to those presented for the interleaved boost converter in that the conventional model over predicts the stability range of the system [9].

Finally, this modelling technique can be further applied to converters with more than two phases by appropriately modelling the phase-delayed sampling of the individual current control loops using the time delay and time advance units, $e^{snT/N}$ and $e^{snT/N}$, where N is the total number of phases and $n = 1 \dots N$ the phase index.

APPENDIX

The duty ratio-to-phase current transfer function is defined as:

$$G_{d1i1}(s) = G_{d2i2}(s) = G_{di}(s) =$$

$$= \frac{(L+L_c)V_{in}}{L_{Tot}} \frac{\left(s^2 + a_{d1}s + a_{di0}\right)}{s(s^2 + b_1s + b_0)} , \qquad (A.1)$$

where:

$$L_{Tot} = 2L(L_c + L_m) + (L_c^2 - L_m^2),$$
 (A.2)

 $a_{di1} =$

$$=\frac{(L+L_{c})L_{Tot}+C_{o}(2L+L_{c}-L_{m})(L_{c}+L_{m})R_{in}R_{load}}{(L+L_{c})C_{o}L_{Tot}R_{load}},$$
 (A.3)

$$a_{di0} = \frac{(2L + L_c - L_m)(L_c + L_m)(R_{in} + R_{load})}{(L + L_c)C_oL_{Tot}R_{load}},$$
(A.4)

$$b_1 = \left(\frac{2L_c R_{in} + 2L_m R_{in}}{L_{Tot}} + \frac{1}{C_o R_{load}}\right), \text{ and}$$
(A.5)

$$b_{0} = \frac{2(L_{c} + L_{m})(R_{in} + R_{load})}{L_{Tot}C_{o}R_{load}}$$
 (A.6)

The duty ratio-to-opposite phase current transfer function is defined as:

$$G_{d1i2}(s) = G_{d2i1}(s) = G_{dxi}(s) =$$

$$= \frac{(L_m - L)V_{in}}{L_{Tot}} \frac{\left(s^2 - a_{dxi1}s - a_{dxi0}\right)}{s(s^2 + b_1s + b_0)} , \qquad (A.7)$$

where

$$a_{dxi0} = \frac{(2L + L_c - L_m)(L_c + L_m)(R_{in} + R_{load})}{(L_m - L)C_o L_{Tot} R_{load}}, \text{ and}$$
(A.8)

 $a_{dxi1} =$

$$=\frac{(L-L_m)L_{Tot}+C_o(2L+L_c-L_m)(L_c+L_m)R_{in}R_{load}}{(L_m-L)C_oL_{Tot}R_{load}} .$$
 (A.9)

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REFERENCES

- B. C. Barry, J. G. Hayes, and M. S. Rylko, "CCM and DCM Operation of the Interleaved Two-Phase Boost Converter with Discrete and Coupled Inductors," in *IEEE Transactions Power Electronics*, vol. 30, DOI 10.1109/TPEL.2014.2386778, no. 12, pp. 6551–6567, 2015.
- [2] M. Pavlovsky, G. Guidi, and A. Kawamura, "Assessment of coupled and independent phase designs of interleaved multiphase buck/boost DC-DC converter for EV power train," in *IEEE Transactions Power Electronics*, vol. 29, DOI 10.1109/TPEL.2013.2273976, no. 6, pp. 2693–2704, 2014.
- [3] G. Calderon-Lopez and A. J. Forsyth, "High Power Density DC-DC Converter with SiC MOSFETs for Electric Vehicles," in *Proc. 7th IET International Conference on Power Electronics Machines and Drives* (*PEMD 2014*), DOI 10.1049/cp.2014.0463, p. 1.4.01-1.4.01, 2014.
- [4] H. Lim, M. Jang, and V. Agelidis, "A phase shedding technique for PV system based on interleaved boost converter," in *Proc.* 2nd IEEE International Future Energy Electronics Conference (IFEEC 2015), DOI 10.1109/IFEEC.2015.7361504, 2015.
- [5] C. Klumpner, K. Ponggorn, M. Rashed, D. De, C. Patel, and G. Asher, "Modelling and control of a multi-stage interleaved DC–DC converter with coupled inductors for super-capacitor energy storage system," in *IET Power Electronics*, vol. 6, DOI 10.1049/iet-pel.2012.0529, no. 7, pp. 1360–1375, 2013.
- [6] M. Ilic and D. Maksimovic, "Digital average current-mode controller for DC-DC converters in physical vapor deposition applications," in *IEEE Transactions Power Electronics*, vol. 23, DOI 10.1109/TPEL.2008.920880, no. 3, pp. 1428–1436, 2008.
- [7] B. C. Barry, J. G. Hayes, R. T. Ryan, M. S. Rylko, R. Stala, A. Penczek and A. Mondzik, "Small-signal model and control of the interleaved two-phase coupled-inductor boost converter," in *Proc. 2016 IEEE Energy Conversion Congress and Exposition (ECCE 2016)*, DOI 10.1109/ECCE.2016.7855447, pp. 1-6, 2017.
- [8] O. F. Ruiz and I. Cervantes, "Averaged modeling of transformercoupled interleaved boost converters," in *Proc. 38th Annual Conference* on *IEEE Industrial Electronics Society (IECON 2012)*, DOI 10.1109/IECON.2012.6388637, pp. 256–261, 2012.
- [9] A. Villarruel-Parra and A. J. Forsyth, "Enhanced Average-Value Modeling of Interleaved DC – DC Converters Using Sampler Decomposition," in *IEEE Transactions Power Electronics*, vol. 32, DOI 10.1109/TPEL.2016.2559449, no. 3, pp. 2290–2299, 2017.
- [10] R. W. Erickson and D. Maksimović, Fundamentals of power electronics, ch. 7, pp. 235-241, 2nd ed., 223 Spring Street, New York, NY 10013, USA, Springer Science + Business Media, LLC, 2004.
- [11] D. Maksimović, R. W. Erickson, C. Griesbach, "Modeling of crossregulation in converters containing coupled inductors", *in IEEE Transactions Power Electronics*, vol. 15, DOI: 10.1109/63.849030, no. 4, pp. 607-615, 2000.
- [12] S. Buso and P. Mattavelli, *Digital Control in Power Electronics*, San Rafael, CA, USA, Morgan & Claypool, 2006, pp.39-40. DOI: 10.2200/S00047ED1V01Y200609PEL002.
- [13] Jingquan Chen, A. Prodic, R. W. Erickson and D. Maksimovic, "Predictive digital current programmed control," in *IEEE Transactions Power Electronics*, vol. 18, DOI: 10.1109/TPEL.2002.807140, no. 1, pp. 411–419, 2003.
- [14] G. Calderon-Lopez, A. Villaruel-Parra, P. Kakosimos, S. K. Ki, R. Todd, and A. J. Forsyth, "Comparison of digital PWM control strategies for high power interleaved DC-DC converters," in *IET Power Electronics*, vol. 11, DOI 10.1049/iet-pel.2016.0886, no. 2, pp. 391-398, 2018.
- [15] H. Kim, M. Falahi, T. M. Jahns, and M. W. Degner, "Inductor current measurement and regulation using a single DC link current sensor for interleaved DCDC converters," in *IEEE Transactions Power Electronics*, vol. 26, DOI 10.1109/TPEL.2010.2084108, no. 5, pp. 1503–1510, 2011.
- [16] L. Ni, D. J. Patterson, and J. L. Hudgins, "High power current sensorless bidirectional 16-phase interleaved DC-DC converter for hybrid vehicle application," in *IEEE Transactions Power Electronics*, vol. 27, DOI 10.1109/TPEL.2011.2165297, no. 3, pp. 1141–1151, 2012.
- [17] Y. Cho, A. Koran, H. Miwa, B. York, and J. S. Lai, "An active current reconstruction and balancing strategy with DC-link current sensing for a multi-phase coupled-inductor converter," in *IEEE Transactions Power Electronics*, vol. 27, DOI 10.1109/TPEL.2011.2170590, no. 4, pp. 1697–1705, 2012.



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