DTU Library

# Resonant Push-pull Converter with Flyback Regulator for MHz High Step-Up Power Conversion 

Wang, Chang; Li, Mingxiao; Ouyang, Ziwei; Wang, Gang

Published in:
IEEE Transactions on Industrial Electronics

Link to article, DOI:
10.1109/tie.2020.2969109

Publication date:
2020

Document Version
Peer reviewed version

Link back to DTU Orbit

Citation (APA):
Wang, C., Li, M., Ouyang, Z., \& Wang, G. (2020). Resonant Push-pull Converter with Flyback Regulator for MHz High Step-Up Power Conversion. IEEE Transactions on Industrial Electronics, 68(2), 1178-1187.
https://doi.org/10.1109/tie.2020.2969109

[^0]
# Resonant Push-pull Converter with Flyback Regulator for MHz High Step-Up Power Conversion 

Chang Wang, Student Member, IEEE, Mingxiao Li, Student Member, IEEE, Ziwei Ouyang, Senior Member, IEEE, and Gang Wang, Member, IEEE


#### Abstract

With the trend towards achieving high efficiency, high power density and high operating frequency in power converters, a galvanic isolated circuit architecture is proposed in this paper for high step-up applications with wide input-voltage range. This converter consists of a current-fed resonant push-pull converter (PP) as a DC transformer (DCX) dealing with most of power with high efficiency and an active clamp flyback converter (ACF) as a regulator within a large conversion range. As a single-stage converter, the ACF regulator is paralleled with PP converter to share the total power and regulates the high output voltage. An experimental prototype with an input voltage range of $24 \mathrm{~V}-32 \mathrm{~V}$ and output $400 \mathrm{~V} / 400$ $W$ is built under 1 MHz switching frequency. A peak efficiency of $97.1 \%$ and a power density of $210 \mathrm{~W} / \mathrm{in}^{3}$ (or 13 W/cm ${ }^{3}$ ) are achieved. Experimental result validates the correctness of the analysis and proves the feasibility of the proposed converter for MHz high step-up DC-DC conversion.


Index Terms-Current-fed resonant push-pull, active clamp flyback, high step-up dc-dc converter, wide inputvoltage range, MHz, high efficiency, high power density.

## I. INTRODUCTION

Renewable energy has developed rapidly recent years due to its renewable and freely available characters. For example, the photovoltaic (PV) system plays an important role in many applications. As the energy dragged from PV panels mainly depends on the continuously changed solar radiation, it leads to the problem that the output voltage of a PV module is usually low and unregulated. At the meantime, medium high level of DC voltages (hundreds of volts) are needed in many applications such as electric vehicles, data center, communication satellites, DC microgrid, etc [1]. A front-end dc-dc converter is needed to boost and regulate the PV voltage to DC bus voltage [2]. The design consideration of such high step-up converter includes many aspects such as high

[^1]efficiency, low electro-magnetic interference (EMI), reduction in mass, volume and cost, long lifetime and reliability, etc. Among which efficiency and volume are prior consideration.

There has been considerable research regarding the wide input range and high step-up DC-DC conversion. Theoretically, the conventional boost converter with extreme duty cycle can be employed due to its simple structure and different circuit architectures are introduced in [3]-[6]. However, it results in large current ripple, high switching loss and high voltage stress on semiconductors. Converters with coupled inductors are also simple and more flexible solutions introduced in [7]. Switched-capacitor is demonstrated in [8], the quasi-resonant push-pull converter with high efficiency was described in [9] and the quasi-Z source network was applied in [10]. They all provide innovative high voltage gain solutions with fairly high efficiency and soft-switching techniques, but less work was emphasized on achieving high-power density. Converters with advanced function are introduced in [11]-[14], which indicate more possibility in achieving bi-direction, multi-output and higher voltage. However, the desire for small current ripple, smaller switching loss, lower voltage stress on power semiconductors and simpler driving circuit still exists. Multistage solution is demonstrated and compared with singlestage solution in [15]. It is revealed that the multistage solutions increase the number of components which add to the increase in complexity and cost, also decrease the efficiency and power density by transferring power through more stage.

A single-stage high step-up dc-dc converter with galvanic isolation is proposed in this paper. The circuit architecture is composed of two converters, where a current-fed resonant push-pull converter operates as a DC transformer dealing with most of the power with high efficiency and an active clamp flyback converter operates as a regulator stabilizing the output voltage with the wide input voltage range. Their input is connected in parallel to share the large input current as well as reduce the current ripple, while their output is connected in series to increase the output voltage gain. For PP converter, the integration of leakage inductance into resonant tank is used to reduce the switching losses. Also, the symmetric structure and performing stages give a lower voltage stress on each semiconductor, thus, it's able to deal with higher power compared with other single switch converters. For ACF converter, it's operating close to critical conduction mode (CRM) and in either buck or boost type with the variation of input voltage. It's designed to reach highest efficiency with maximum power distributed. All switches are operating with zero-voltage-switching (ZVS). Experimental results illustrate the proposed converter is capable to achieve high efficiency and high-power density with high operating frequency.

## II. Proposed Circuit Architecture

The given specification is shown in TABLE I where the input voltage varies from 24 V to 32 V , output voltage is 400 V , power scale is from 100 W to 400 W . The other designed parameters are also listed such as the 1 MHz switching frequency which will be illustrated in the later section. The proposed circuit architecture is shown in Fig.1. The top part is a current-fed resonant push-pull converter (PP). It works as a DCX under a fixed switching frequency 1 MHz and fixed voltage transfer ratio $1: 12$. The PP realizes soft switching in both main switches $S_{1}, S_{2}$ and deals with most power of the whole system under the normal operating conditions. The bottom part is an active clamp flyback converter (ACF). It works in both buck and boost modes according to the variation of the input voltage. The ACF switches $S_{3}, S_{4}$ work under the ZVS due to the negative magnetizing current and the active clamp characteristics. The ACF dealing with a small portion of power is to regulate the output voltage, playing a role of the control circuit. Under the full load condition, the consequent power distribution with the two extreme input voltages is shown in Fig.2. In order to achieve comprehensive high efficiency within the whole input voltage range, the parameters design of both the PP and the ACF converters aim to obtain the highest efficiency when they handle the largest power, which are 384 W for PP and 112 W for ACF.

TABLE
SPECIFICATIONS

| SPECIFICATIONS |  |  |
| :---: | :---: | :---: |
| Symbol | Quantity | Value |
| $V i n$ | Input voltage | $24 \mathrm{~V} \sim 32 \mathrm{~V}$ |
| $V o$ | Output voltage | 400 V |
| $P$ | Output power | $100 \mathrm{~W} \sim 400 \mathrm{~W}$ |
| $f s$ | Switching frequency | 1 MHz |
| $D$ | Fixed Push-pull Duty Cycle | 0.45 |
| $N_{p} / N_{s}$ | Push-pull Turns Ratio | $1: 12$ |
| $D_{A C F}$ | Flyback Duty Cycle Range | $0.14 \sim 0.61$ |
| $N_{P A C F} / N_{S A C F}$ | Flyback Turns Ratio | $2: 6$ |



Fig.1. Proposed Circuit Architecture


- Push-pull $\quad$ Flyback


Fig.2. Power distribution under Two Working Conditions


Fig.3. Current-fed Resonant Push-pull Converter


Fig.4. Main Theoretical Waveforms of 8 Stages

## III. Current-fed Resonant Push-pull Converter

## A. Circuit and Operating Principles

The current-fed resonant push-pull converter is shown in Fig. 3 where the integrated leakage inductance $L_{d 1}$ and $L_{d 2}$ are used in the resonant tank. There are 8 operating stages during one period illustrated below and the main theoretical waveforms are shown in Fig. 4.

Stage 1 [ $\left.t_{0}-t_{l}\right]$ : When the switch $S_{l}$ is turned on, the current flows through the primary winding $L_{p I}$ to transfer the energy to the secondary part. The voltage on $L_{p l}$ is clamped by the output voltage. And the resonance current $i_{r}$ going through the switch's drain-source is resonated between the leakage inductance $L_{d l}$ and the resonance capacitor $C_{r}$. The parasitic capacitance of the transformer joins the resonance but it's negligible due to the small value compared with $C_{r}$. The input inductor $L_{i n}$ also joins the resonance but it's negligible due to the large value compared with leakage inductance $L_{d l}$. The magnetizing inductance $L_{m l}$ is charged and the magnetizing current $i_{m}\left(i_{m l}\right)$ is rising linearly. At the end of this stage $\left(t_{1}\right), i_{r}$ and $i_{m}\left(i_{m l}\right)$ intersect to a certain value $I_{m m a x}$, where energy transferred from primary winding to secondary winding stops.


Stage $2\left[\boldsymbol{t}_{1}-\boldsymbol{t}_{2}\right]$ : At the moment of $t_{1}$, the magnetizing current $i_{m}$ ( $i_{m l}$ ) begins to decrease at the meantime $i_{m}\left(i_{m 2}\right)$ begins to increase. Based on the Kirchhoff's current law (KCL), the resonance current $i_{r}$ equals to the difference between $i_{m l}$ and $i_{m 2}$. Due to the transformer flux balance relation [16], at the end of this stage $\left(t_{2}\right), i_{m 1}$ and $i_{m 2}$ intersect to a medium value which is around half of $I_{\operatorname{mmax}}$. The resonance current $i_{r}$ decreases to zero, the switch $S_{l}$ is turned off. The period of this stage is relatively short and can be regarded as a transient.


Stage $3\left[\boldsymbol{t}_{2}-\boldsymbol{t}_{3}\right]$ : After the resonance is finished, the magnetizing currents $i_{m}\left(i_{m 1}, i_{m 2}\right)$ remain to charge the parasitic capacitance of switch $C_{s l}$ and discharge the $C_{s 2}$. Thus, the voltage on the switch $S_{l}$ is charged to around twice of the resonant capacitor voltage and the voltage on the switch $S_{2}$ reduces to zero if there is enough energy stored in the magnetizing inductance.


Stage $4\left[t_{3}-t_{t}\right]$ : After the parasitic capacitance $C_{s 2}$ of the switch $S_{2}$ is fully discharged, the $S_{2}$ is turned on immediately when the body diode of the $S_{2}$ is forward biased. At the end of this stage, $S_{2}$ is turned on under ZVS.


Due to the symmetric operation, Stage 5 - Stage $8\left[\boldsymbol{t}_{4}-t_{8}\right]$ is similar as Stage 1 - Stage $4\left[t_{0}-t_{t}\right]$.

## B. Circuit Design Consideration

a) Soft Switching - ZVS Realization

The analysis of charging and discharging of parasitic capacitance $C_{s}$ of the switch during state 3 and state 7 are needed to realize the ZVS. The relative time domain equations are shown in (1),

$$
\begin{align*}
& v_{d s 1}(t)=\frac{1}{C_{s 1}} \int_{t_{2}}^{t_{3}} \frac{1}{2} i_{m}(t) d t, \\
& v_{d s 2}(t)=2 v_{c r}\left(t_{2}\right)-\frac{1}{C_{s 2}} \int_{t_{2}}^{t_{3}} \frac{1}{2} i_{m}(t) d t \tag{1}
\end{align*}
$$

where the resonance capacitor voltage: $v_{c r}\left(\mathrm{t}_{2}\right)=V_{i n}$. During stage 1 and stage 5 , the linearly rising magnetizing current $i_{m}$ can be expressed as below,

$$
\begin{equation*}
i_{m}(t)=i_{m}\left(t_{0}\right)+\frac{V_{n}}{L_{m}} t \tag{2}
\end{equation*}
$$

where from stage 2 and stage $6: i_{m}\left(\mathrm{t}_{0}\right)=-1 / 2 I_{\text {mmax }}$. The clamping voltage $V_{n}$ on windings can be derived from turns ratio and output voltage which also equals to the input voltage due to the DCX operating mode: $V_{n}=V_{o} N_{p} / N_{s}=V_{i n}$. And the period $t$ of stage 1 and stage 5 can be approximated as switch-on time $T_{\text {on }}$ using the duty cycle of main switches over switching frequency: $T_{o n}=D / f_{s}$. Giving us the maximum value of magnetizing current $I_{m \text { max }}$ at the moment $t_{l}$ or $t$,

$$
\begin{equation*}
I_{\max }=\frac{2 V_{i n} D}{3 L_{m} f_{s}} \tag{3}
\end{equation*}
$$

Due to a short time period of stage 3 and stage 7, it is assumed that magnetizing current $i_{m}\left(i_{m 1}, i_{m 2}\right)$ keeps constant during this period. The energy stored in the magnetizing inductance $L_{m l}$ or $L_{m 2}$ must be sufficient to cause a voltage swing across the switch equal to twice of the center tap voltage [17],

$$
\begin{equation*}
L_{m}\left(\frac{I_{m \max }}{2}\right)^{2} \geq C_{s}\left(2 V_{i n}\right)^{2} \tag{4}
\end{equation*}
$$

Larger $L_{m}$ leads to a smaller energy stored in the magnetizing inductance which is not conductive to the realization of ZVS. Therefore, one maximum value for $L_{m}$ can be described according to (3) and (4):

$$
\begin{gather*}
L_{\max }\left(\frac{V_{i n} D}{3 L_{\max } f_{s}}\right)^{2}=4 C_{s} V_{i n}^{2} \\
L_{\max }=\frac{D^{2}}{36 f_{s}^{2} C_{s}} \tag{5}
\end{gather*}
$$

## b) Resonant Tank Analysis

The analyses of main switches drain-source current in stage 1 and stage 2 (stage 5 and stage 6) are needed to reduce the switch loss for main switches. It can be written as two parts, one part is the resonance current $i_{r}$ in sinusoidal waveform written in (6) [16], the other one is the magnetizing current $i_{m}$ in linear waveform written in (2). A point of the intersection is described by the value of $I_{\text {maxax }}$.

$$
\begin{align*}
i_{r}(t) & =\left[\sqrt{\frac{L_{i n}\left(C_{r}+C_{p}\right)}{L_{r}\left(L_{i n}+L_{r}\right)}}\left(v_{c r}\left(t_{0}\right)-V_{n}\right)-\frac{1}{L_{i n}+L_{r}}\right. \\
& \left.\cdot \sqrt{\frac{L_{i n} L_{r}\left(C_{r}+C_{p}\right)}{L_{i n}+L_{r}}}\left(V_{i n}-V_{n}\right)\right] \sin \left(\omega_{r} t\right) \\
& +\frac{V_{i n}-V_{n}}{L_{i n}+L_{r}} t+\frac{i_{i n}\left(t_{0}\right) L_{i n}}{L_{i n}+L_{r}}\left(1-\cos \left(\omega_{r} t\right)\right) \tag{6}
\end{align*}
$$

Where the resonance inductor $L_{r}$ is leakage inductance of the transformer: $L_{r}=L_{d l}=L_{d 2}$. The input inductor $L_{i n} \gg L_{r}$, and thus, can be ignored from the resonant tank. The equivalent parasitic capacitor $C_{p}$ of windings is much smaller than the resonant capacitor: $C_{p} \ll C_{r}$, which can also be neglected from the resonance. The initial capacitor voltage: $v_{c r}\left(\mathrm{t}_{0}\right)=V_{i n}$; the initial input current equals to the average input current which can be estimated: $i_{i n}\left(\mathrm{t}_{0}\right)=I_{\text {inavg }}=P N_{s} / V_{o} N_{p}$; the clamping voltage on windings equals to the input voltage due to the DCX operating mode: $V_{n}=V_{i n}$. So (6) can be simplified as (7). By choosing the proper $C_{r}$, the resonant frequency $\omega_{r}$ is tuned to be around twice of switching frequency to form a half sinusoidal current waveform during switch-on time. Thus, it can minimize the current root mean square (RMS) value to enable a lower conduction loss and reduce the circulating loss.

$$
\begin{equation*}
i_{r}(t)=\frac{P N_{s}}{V_{o} N_{p}}\left(1-\cos \left(\omega_{r} t\right)\right) \tag{7}
\end{equation*}
$$

$$
\begin{equation*}
\omega_{r}=\frac{1}{\sqrt{L_{r} C_{r}}} \approx \frac{2 \pi f_{s}}{D} \tag{8}
\end{equation*}
$$

Magnetizing current $i_{m}$ is described in (2). Smaller $L_{m}$ gives a higher value of $I_{\operatorname{mmax}}$, thus leading longer time period of stage 2 and stage 6 and forming a higher current intersection point, which is not conductive to the reduction of switching-off loss. Maximum value of magnetizing current $I_{m \max }$ below $25 \%$ of resonance current peak value $i_{r(\max )}$ can be regarded as reasonable choice, which gives us $I_{\max } \leq i_{r(\max )} / 4=P N_{s} / 2 V_{o} N_{p}$. Therefore, the minimum limit of $L_{m}$ can be described,

$$
\begin{equation*}
L_{m \min }=\frac{4 V_{i n} V_{o} D N_{p}}{3 f_{s} P N_{s}} \tag{9}
\end{equation*}
$$

c) Magnetizing Inductance and Switching Frequency Combining (5) and (9), the limit of $L_{m}$ can be determined,

$$
\begin{equation*}
\frac{4 V_{\text {in }} V_{o} D N_{p}}{3 f_{s} P N_{s}} \leq L_{m} \leq \frac{D^{2}}{36 f_{s}^{2} C_{s}} \tag{10}
\end{equation*}
$$

the Gallium Nitride (GaN-FET) EPC2032 is selected as the main switch whose output capacitance is 800 pF due to the manufacturer datasheet [18]. The magnetizing inductance $L_{m}$ range as a function of switching frequency $f_{s}$ is plotted in Fig. 5 where the solution space of $L_{m}$ is between the two limits defined in (10). Due to Faraday's law, higher frequency helps to shrink the size of magnetic components. Given the consideration of certain tolerance and the acceptable core loss, $f_{s}=1 \mathrm{MHz}$ is chosen for the switching frequency and the above range can be quantified: $1.6 \mu \mathrm{H} \leq L m \leq 4.7 \mu \mathrm{H}$. The $L_{m}$ is chosen to be at the minimum accepted value $1.6 \mu \mathrm{H}$ for fully achieving ZVS in this case:

$$
\begin{equation*}
L_{m}=\frac{4 V_{i n} V_{o} D N_{p}}{3 f_{s} P N_{s}} \tag{11}
\end{equation*}
$$



Fig.5. Solution Space for $L_{m}$ by $f_{s}$

## d) Input Current Ripple

Based on the Kirchhoff's current law (KCL), the input current going through the input inductor $i_{i n}$ equals to the sum of resonant current $i_{r}$ and the current going into the resonant capacitor $i_{\text {cr }}$. Regarding the design for the input inductor is to provide a small input ripple, the resonant capacitor current $i_{C r}$ can be derived from (7) assuming a constant input current $I_{\text {inavg }}$ :

$$
\begin{equation*}
i_{C r}(t)=I_{\text {inavg }}-i_{r}(t)=\frac{P N_{s}}{V_{o} N_{p}} \cos \left(\omega_{r} t\right) \tag{12}
\end{equation*}
$$

Based on the Kirchhoff's voltage law (KVL), the input voltage $V_{\text {in }}$ equals to the sum of voltage on input inductor $v_{\text {Lin }}$ and
voltage on resonant capacitor $v_{C r}$. Recalling that the average of inductor voltage in a switching period is zero in steady-state operation. Combing with (8) and (12), the resonant capacitor voltage $v_{C r}$ and input inductor voltage $v_{\text {Lin }}$ can be expressed as,

$$
\begin{gather*}
v_{C r}(t)=\frac{1}{C_{r}} \int i_{C r}(t) d t=L_{r} \frac{2 \pi f_{s} P N_{s}}{D V_{o} N_{p}} \sin \left(\omega_{r} t\right)+V_{i n}, \\
v_{L i n}(t)=V_{i n}-v_{C r}(t)=-L_{r} \frac{2 \pi f_{s} P N_{s}}{D V_{o} N_{p}} \sin \left(\omega_{r} t\right) \tag{13}
\end{gather*}
$$

where the leakage inductance $L_{r}$ is estimated to be $5 \%$ of the designed magnetizing inductance $L_{m}$ empirically [19]: $L_{r}=5 \%$ $L_{m}$. The input inductor $L_{i n}$ should be designed to provide small input current ripple and $10 \%$ ripple is taken for design. The maximum voltage on input inductor is chosen for calculation:

$$
\begin{equation*}
L_{i n}=v_{L i n(\max )} \frac{\Delta t}{\Delta I}=\frac{5 \%}{10 \%} \cdot \frac{4 \pi V_{i n} V_{o} N_{p}}{3 f_{s} P N_{s}} \tag{14}
\end{equation*}
$$

## e) Circuit Design Flowchart

The above circuit design can be summarized as a flowchart shown in Fig.6. With the given specification and the desired properties, the key parameters can be derived.


Fig.6. Circuit Parameters Design Flow

## C. Magnetics Design

For large turns ratio $N_{p} / N_{s}=1: 12$, one single turn is used for the primary winding, and 12 turns for the secondary windings to reduce the winding losses and parasitic capacitances
[20][21]. The magnetic core material ML91S has been proved to be an excellent material for high frequency transformer design [22], which is chosen for 1 MHz frequency. To produce adequate value of magnetizing inductance $L_{m}=1.6 \mu \mathrm{H}$ in one single turn according to (11), the core type E32/6/20 with an air gap of 0.06 mm on the center leg is chosen for the design. It can be seen from (13) and circuit operating principles that the leakage inductance $L_{d}$ should be minimized in transformer design in order to provide low voltage stress for the relevant passive components and the main switches. Since planar print circuit board (PCB) windings are chosen for the transformer design, ac resistance is aimed to be reduced [23]. Thus, interleaving structure is adopted for this case [24][25]. As is discussed in [21], the stray capacitance cannot be ignored in planar transformer design. Fully interleaving winding structure contributes to the reduction of the leakage inductance as well as the ac resistance, but it adds up to a large stray capacitance which affects the normal operation of the designed circuit. After a comprehensive trade-off analysis, the designed winding layout is shown in Fig. 7 (Only one part of the primary windings is considered due to the symmetric working states). Two 1-turn primary windings are connected in parallel to share the large primary current thus reducing the winding loss. Four groups of two parallel connected 3-turns secondary windings are laid symmetrically one both sides of the primary windings which are connected in series to form 12 turns. The transformer parameters are shown in TABLE II.


Fig.7. Interleaving Structure


Fig.8. MMF Distribution
TABLE II
Push-pull Transformer Parameters

| Quantity | Parameters |
| :---: | :---: |
| Core / material / air gap | E32/6/20 $/$ ML91S $/ 0.06 \mathrm{~mm}$ |
| Winding type | $3^{*} 4$ layers planar PCB winding |
| Winding material | $2 \mathrm{oz}(70$ um $)$ copper |
| Structure of pri-winding | 1 turn $/ 2^{*} 1$ turn in parallel |
| Structure of sec-winding | 12 turns $/ 2 * 3$ turns in parallel $/ * 4$ in series |

## D. Losses Calculations

## a) Conduction Loss

The Gallium Nitride (GaN-FET) EPC2032 is chosen for its low conduction loss and small size. The main switches drainsource current in stage 1 and stage 2 (stage 5 and stage 6) can be approximated as resonant current written in (7). The total conduction loss of two switches $S_{l}$ and $S_{2}$ can be calculated referring to the drain-to-source on resistance provided by the manufacturer datasheet [18],

$$
\begin{equation*}
P_{\text {cond }}=2 i_{r(R M S)}^{2} \cdot R_{D S(o n)} \tag{15}
\end{equation*}
$$

b) Winding Loss

Based on Dowell's assumptions and the general field solutions for the distribution of current density in a single layer, the ac resistance of $m^{t h}$ layer is derived as [21],
$\frac{R_{a c, m}}{R_{d c, m}}=\frac{\xi}{2}\left[\frac{\sinh \xi+\sin \xi}{\cosh \xi-\cos \xi}+(2 m-1)^{2} \cdot \frac{\sinh \xi-\sin \xi}{\cosh \xi+\cos \xi}\right]$
where $\xi=h / \delta, h=70 \mu \mathrm{~m}$ is the copper thickness for the PCB windings and $\delta=0.075 / \sqrt{n \cdot f_{s}}$ is the skin depth of $n^{\text {th }}$ order frequency in conductor, and $m$ is defined as a ratio,

$$
\begin{equation*}
m=\frac{F(h)}{F(h)-F(0)} \tag{17}
\end{equation*}
$$

where $F(0)$ and $F(h)$ are the magneto-motive force (MMF) at the limits of a layer [26][27], as shown in Fig.8.

For both primary windings working in symmetric stages, the winding current can be analyzed using Fast Fourier Transform Algorithm (FFT). The $R_{a c, p, n} / R_{d c, p, n}$ ratio of each frequency order can be calculated according to (16). And dc resistance: $R_{d c, p}=\rho \cdot l / A$, where $\rho=2.3 \cdot 10^{-8} \Omega \cdot \mathrm{~m}$ is the resistivity of copper at $100^{\circ} \mathrm{C}, l$ and $A$ are the length and cross section area of the wire which can be calculated based on the geometry of the core. After the calculation of ac resistance $R_{a c, p, n}$, the winding loss for both primary windings is:

$$
\begin{equation*}
P_{\text {priwind }}=\sum_{1}^{n} 2 i_{r(R M S), n}^{2} \cdot R_{a c, p, n} \tag{18}
\end{equation*}
$$

With the similar calculation method as mentioned above, the secondary winding loss is,

$$
\begin{equation*}
P_{\text {secwind }}=\sum_{1}^{n} 2\left(\frac{i_{r(R M S), n} N_{p}}{N_{s}}\right)^{2} \cdot R_{a c, s, n} \tag{19}
\end{equation*}
$$

and the total winding loss is: $P_{\text {wind }}=P_{\text {priwind }}+P_{\text {secwind }}$.
c) Core Loss

Steinmetz equation is used for calculating core loss,

$$
\begin{equation*}
P_{v}=K \cdot f_{s}^{\alpha} \cdot\left(\frac{\Delta B}{2}\right)^{\beta} \tag{20}
\end{equation*}
$$

where $K, \alpha, \beta$ are constants provided by the core manufacturer. And $\Delta B$ is the peak-to-peak flux density which can be calculated from Faraday's law,

$$
\begin{equation*}
\Delta B=\frac{V_{n} \cdot \Delta t}{N_{p} \cdot A_{e}} \tag{21}
\end{equation*}
$$

where $A_{e}$ is the effective area of the core. Thus, the core loss
can be calculated:

$$
\begin{equation*}
P_{\text {core }}=P_{v} \cdot V_{e} \tag{22}
\end{equation*}
$$

where $V_{e}$ is effective volume of the core.

## IV. Buck-boost Active Clamp Flyback Converter

## A. Basic Operation Principles

The active-clamp flyback circuit is used to regulate the output voltage, which is connected with the push-pull converter in parallel in primary side and in series in secondary side as shown in Fig.1. Considering the input voltage at its minimum value, the ACF should transfer the maximum power as shown in Fig.2. The ACF should be designed to reach high efficiency under the maximum power, because it affects the total system efficiency more than the circumstance under the minimum power.

In traditional flyback converters, the main switch suffered from a large voltage spike and ringing due to leakage inductance when it turns off. Also, the transformer for flyback converter is a coupled inductor. No flux cancellation can be achieved and interleaving strategy cannot be used to reduce the ac resistance. Consequently, tradition flyback converter suffers from larger winding loss at high frequency [28].

For the ACF converter, the energy stored in the leakage inductance is utilized to achieve the ZVS. No voltage spike and ringing occur to the main switch. More importantly, the reverse primary current reduces the magnetic field strength and the total winding loss can be reduced by applying interleaving winding layout [28]-[30].

## B. Design Considerations for ACF

a) Clamp Capacitor

The turn-off current on auxiliary switch and secondary rectifier are small if the half resonant period formed by clamp capacitor $C$ and leakage inductance $L_{d}=L_{d 3}$ is close to the turnoff time of the main switch. However, the primary RMS current increases with the smaller clamp-capacitor. On the other hand, the larger clamp capacitor $C$ means smaller primary RMS current while larger turn-off current on auxiliary switch and secondary rectifier [31]. Therefore, the selection of clamp capacitor should be based on the converter total power loss. In this design, conduction loss is dominant because primary winding and switches suffers from large conduction current. The large clamp capacitor is selected to minimize the conduction power loss: $C=2 \mathrm{uF}$.

## b) Turns Ratio

Both winding loss and core loss should be considered for the transformer turns ratio selection. Core material ML91S and core type E22/6/16+PLT22/16/2.5 is used for the transformer magnetic core. The flux density for the magnetic core can be calculated same as (21), and the core loss can be similarly derived from (20) and (22). In this case, winding loss is dominant. A trade-off is made between core loss and winding loss, the turns ratio is determined to be 2:6.

## c) Magnetizing Inductance

This converter is built to operate close to CRM. The small reverse magnetizing current helps to achieve ZVS. The magnetizing inductance can be designed smaller than the
critical value between the DCM and CCM. Usual methods can be used to determine this critical value. The designed parameters for the ACF is $L_{m}=600 \mathrm{nH}, L_{r}=15 \mathrm{nH}$.

## V. Experiment Results

The $1 \mathrm{MHz}, 400 \mathrm{~W}, 24 \mathrm{~V}-32 \mathrm{~V} / 400 \mathrm{~V} 0$ experimental prototype is built and shown in Fig.9. The key components are listed in TABLE III. It can be seen that GaN-FET are used in both PP and ACF converters for achieving smaller volume. The power density of the prototype reaches $210 \mathrm{~W} / \mathrm{in}^{3}$ (or $13 \mathrm{~W} / \mathrm{cm}^{3}$ ) calculated from the box volume. The tested parameters from Precision Impedance Analyzer Agilent 4294A for the designed PP are: $L_{m}=1.6 \mu \mathrm{H}, L_{d}=8 \mathrm{nH}, R_{a c}=14 \mathrm{~m} \Omega$; for the designed ACF are: $L_{m}=644 \mathrm{nH}, L_{d}=14 \mathrm{nH}, R_{a c}=31 \mathrm{~m} \Omega$ The small value of leakage inductance of PP further proves the correctness of the designed interleaving structure and the small ac resistance of both PP and ACF windings validates the low loss design. Also, the value of magnetizing inductance is consistent with the design. Thus, the resonant capacitor $C_{r}$ of PP is tuned to be 447 nF to constitute the desired resonant tank.

The main switch drain-to-source current $i_{d s}$ and voltage $v_{d s}$ waveforms of PP converter under its maximum power condition ( $V_{i n}=32 \mathrm{~V}, P_{P P}=384 \mathrm{~W}$ ) are shown in Fig.10. As is seen, the desired resonant current waveform is obtained and the main switches are operating under ZVS. The main waveforms of ACF converter under its maximum power condition ( $V_{i n}=24 \mathrm{~V}, P_{A C F}=112 \mathrm{~W}$ ) are shown in Fig.11. The main switches of ACF converter are also operating under ZVS seen from drain-to-source voltage $v_{d s}$. Since the auxiliary switch $S_{4}$ is easier to achieve ZVS because of the ACF characteristics. A smaller dead time is applied for discharging the drain-to-source capacitance of $S_{4}$.

The efficiency of PP converter is shown in Fig.12. The peak efficiency reaches $97.8 \%$ at $240 \mathrm{~W}, 192 \mathrm{~W}$ and 168 W operating points. Within all the operating range (even under light load condition), the PP converter achieves high efficiency $\geq$ $95.6 \%$ which proves the effective analysis and design of DCX. The efficiency of ACF converter is shown in Fig.13. It reaches highest efficiency $93.1 \%$ with largest power 112 W , which is quite coherent to the analysis and design. The efficiency of the whole system is shown in Fig. 14 where the peak efficiency $97.1 \%$ occurs at 250 W and efficiency of $96.4 \%$ is attained at nominal operation point ( $V_{i n}=28 \mathrm{~V}, P=400 \mathrm{~W}$ ).

Under the nominal operation point ( $V_{\text {in }}=28 \mathrm{~V}, P=400 \mathrm{~W}$ ), the thermal image tested under $25^{\circ} \mathrm{C}$ ambient temperature after 10 minutes operation is shown in Fig. 15. The highest temperature is $51.3^{\circ} \mathrm{C}$ occurs on the primary device. The PP and ACF GaNFETs are $43.8^{\circ} \mathrm{C}$ and $50.6^{\circ} \mathrm{C}$ shown as Spot 1 and Spot 2 in the image. All devices operate within the safe temperature range which proves the excellent thermal performance and validates the high efficiency design. The corresponding losses breakdown is shown in Fig. 16 where the winding loss is calculated from the experimental result of ac resistance $R_{a c}$ and other losses are calculated from theoretical analyses.

Table IV provides a comprehensive comparison of proposed converter and similar works from recent studies in terms of circuit features. The two parts of the proposed converter stack up to a higher voltage gain, which is suitable
for the high step-up applications. Higher efficiency is achieved by practical power sharing and the optimum design. Under high operating frequency, high-power density is achieved. However, there is a small sacrifice on components counts.

|  | TABLE III <br> COMPONENT LIST |
| :---: | :---: |
| Component | Product Information |
| PP Core/material/air gap | $\mathrm{E} 32 / 6 / 20 / \mathrm{ML} 91 \mathrm{~S} / 0.06 \mathrm{~mm}$ |
| ACF Core/material/air gap | $\mathrm{E} 22 / 6 / 16+\mathrm{PLT} 22 / 16 / 2.5 / \mathrm{ML} 91 \mathrm{~S} / 0.2 \mathrm{~mm}$ |
| $\mathrm{GaN}-\mathrm{FET}$ of PP/ACF | $\mathrm{EPC} 2032 / \mathrm{EPC} 2001 \mathrm{C}$ |
| Gate driver of PP/ACF | $\mathrm{LM} 5114 \mathrm{BSD} / \mathrm{Si} 8273 \mathrm{~GB}-\mathrm{IS} 1$ |
| Input inductor | $\mathrm{PA} 4343.472 \mathrm{ANLT} / 4.7 \mathrm{uH} / 17 \mathrm{~A} / 8 \mathrm{~m} \Omega$ |
| Output diode | $\mathrm{C} 3 \mathrm{D} 04060 \mathrm{E} / \mathrm{Silicon} \mathrm{Carbide/600V/6A/10nC}$ |



Fig.9. Photo of Experimental Prototype


Fig.10. Main Switch Waveforms of Push-pull Converter (PP)


Fig.11. Main Waveforms of Flyback Converter (ACF)


Fig.12. Push-pull Converter (PP) Efficiency Curve

| Converters | Voltage Gain | Voltage <br> Stress of Main Switch | Voltage Stress of Output Diode | No. of Components S/D/C/I* | Input/Output <br> Voltage | Nominal Power | Switching <br> Frequency | Power <br> Density | Efficiency Range \& Nominal Efficiency |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Ref. [9] | $\frac{N}{1-D}$ | $\frac{V_{i n}}{1-D}$ | $V_{O}$ | 3/2/4/2 | $30 \sim 50 \mathrm{~V} / 350 \mathrm{~V}$ | 510W | 100 kHz | 1 | $\begin{gathered} 93.3 \sim 95.7 \% @ 60 \sim 510 \mathrm{~W} \\ 95.5 \% @ 510 \mathrm{~W} \end{gathered}$ |
| Ref. [10] | $\frac{N}{1-2 D}$ | $>\frac{V_{i n}(1-D)}{1-2 D}$ | $V_{O}$ | 4/5/12/4 | $10 \sim 60 \mathrm{~V} / 400 \mathrm{~V}$ | 300W | 50 kHz | 1 | $\begin{gathered} 87.5 \sim 95.3 \% @ 30 \sim 300 \mathrm{~W} \\ 94.2 \% @ 300 \mathrm{w} \end{gathered}$ |
| Ref. [16] | $2 N D$ | $V_{i n}+\frac{V_{O}}{N}$ | $V_{O}$ | 2/4/3/2 | 12V/400~420V | 400W | 65 kHz | 1 | $\begin{gathered} \text { 80~93\%@8~412W } \\ 93 \% @ 400 \mathrm{~W} \end{gathered}$ |
| Ref. [32] | $\frac{N}{1-D}$ | $\frac{V_{O}}{N}$ | $2 V_{o}$ | 3/2/5/4 | 48V/180V | 650W | 100 kHz | 1 | $\begin{gathered} \text { 89~94.5\% @ 50~650w } \\ 91 \% @ 650 \mathrm{~W} \end{gathered}$ |
| Ref. [33] | $N \frac{1+D}{1-D}$ | $\frac{V_{i n}}{1-D}$ | $\frac{V_{O}}{1+D}$ | 1/5/5/2 | 24V/120~200V | 200W | 50 kHz | 1 | $\begin{gathered} 93.8 ~ 96.2 \% @ 20 \sim 200 \mathrm{w} \\ 93.8 \% @ 200 \mathrm{w} \end{gathered}$ |
| Proposed | $N_{P P}+N_{\text {ACF }} \frac{D}{1-D}$ | $V_{\text {in }}+\frac{V_{O}}{N}$ | $V_{O}$ | 4/5/4/3 | 24~32V/400V | 400W | 1 MHz | 210W/in3 | $\begin{gathered} \text { 94~97.1\%@ 100~400W } \\ 96.8 \% @ 400 \mathrm{~W} \\ \hline \hline \end{gathered}$ |

Acronyms: S - Switches; D - Diodes; C - Capacitors (including input and output capacitors); I - Inductors (including coupled inductors).


Fig.13. Flyback Converter (ACF) Efficiency Curve


Fig.14. Proposed Converter Efficiency Curve


Fig.15. Thermal Image under Nominal Operation: 28V / 400W


Fig.16. Loss Breakdown under Nominal Operation: 28V / 400W

## VI. Conclusion

This study proposed, analyzed and quantified a high efficiency high power density isolated dc-dc converter with a practical circuit architecture for step-up renewable energy applications. A current-fed push-pull converter operating as a DCX converter and an active clamp flyback converter operating as a voltage regulator are connected with parallel input and series output, which is suitable for step-up dc-dc conversion from a unregulated low-voltage source to a highvoltage load. The circuit analysis and magnetic design of the proposed dc-dc converter is elaborated in this paper, which is verified by a $1 \mathrm{MHz}, 400 \mathrm{~W}, 24 \mathrm{~V}-32 \mathrm{~V} / 400 \mathrm{~V}$ experimental prototype. It can be concluded from the experimental results that all switches achieve soft switching (ZVS). The system peak efficiency reaches $97.1 \%$ at 250 W and efficiency of $96.4 \%$ is obtained at nominal operation point ( $V_{i n}=28 \mathrm{~V}, P=400 \mathrm{~W}$ ). The power density reaches at $210 \mathrm{~W} / \mathrm{in}^{3}$ (or $13 \mathrm{~W} / \mathrm{cm}^{3}$ ).

## Reference

[1] M. Forouzesh, Y. Siwakoti, S. Gorji, F. Blaabjerg and B.Lehman, "StepUp DC-DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications," IEEE Transactions on Power Electronics, 32(12), pp.9143-9178, 2017.
[2] M. Forouzesh, Y. Shen, K. Yari, Y. Siwakoti, and F. Blaabjerg, "HighEfficiency High Step-Up DC-DC Converter With Dual Coupled Inductors for Grid-Connected Photovoltaic Systems," IEEE Transactions on Power Electronics, 33(7), pp.5967-5982, Jul. 2018.
[3] P. Wang, L. Zhou, Y. Zhang, J. Li and M. Sumner, "Input-Parallel Output-Series DC-DC Boost Converter With a Wide Input Voltage Range, For Fuel Cell Vehicles," IEEE Transactions on Vehicular Technology, 66(9), pp.7771-7781, Sep. 2017.
[4] S. Chen, S. Yang, C. Huang and C. Lin, "Interleaved High Step-Up DCDC Converter With Parallel-Input Series-Output Configuration and Voltage Multiplier Module," 2017 IEEE International Conference on Industrial Technology (ICIT).
[5] Z. Ouyang, G. Sen, O. C. Thomsen and M. A. E. Andersen, "Analysis and Design of Fully Integrated Planar Magnetics for Primary-Parallel Isolated Boost Converter," in IEEE Transactions on Industrial Electronics, vol. 60, no. 2, pp. 494-508, Feb. 2013.
[6] Z. Ouyang, Z. Zhang, O. C. Thomsen and M. A. E. Andersen, "PlanarIntegrated Magnetics (PIM) Module in Hybrid Bidirectional DC-DC Converter for Fuel Cell Application," in IEEE Transactions on Power Electronics, vol. 26, no. 11, pp. 3254-3264, Nov. 2011.
[7] Q. Zhao and F. Lee, "High-Efficiency, High Step-Up DC-DC Converters.," IEEE Transactions on Power Electronics, 18(1), pp.65-73, Jan. 2013.
[8] C. Wei and M. Shih, "Design of a Switched-Capacitor DC-DC Converter With a Wide Input Voltage Range," IEEE Transactions on Circuits and Systems I: Regular Papers, 60(6), pp.1648-1656, Jun. 2013.
[9] Q. Wu, Q. Wang, J. Xu, H. Li and L. Xiao, "A High-Efficiency Step-Up Current-Fed Push-Pull Quasi-Resonant Converter With Fewer Components for Fuel Cell Application," in IEEE Transactions on Industrial Electronics, vol. 64, no. 8, pp. 6639-6648, Aug. 2017.
[10] A. Chub, D. Vinnikov, E. Liivik and T. Jalakas, "Multiphase Quasi-ZSource DC-DC Converters for Residential Distributed Generation Systems," IEEE Transactions on Industrial Electronics, 65(10), pp.8361-8371, 2018.
[11] Z. Zhang, Z. Ouyang, O. C. Thomsen and M. A. E. Andersen, "Analysis and Design of a Bidirectional Isolated DC-DC Converter for Fuel Cells and Supercapacitors Hybrid System," in IEEE Transactions on Power Electronics, vol. 27, no. 2, pp. 848-859, Feb. 2012.
[12] Z. Ouyang and M. A. E. Andersen, "Integrated Three-Port DC-DC Converter for Photovoltaic (PV) Battery Stand-alone Systems," PCIM Asia 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Shanghai, China, 2016, pp. 1-8.
[13] Bin Zhao, Gang Wang, W. G. Hurley and Z. Ouyang, "An interleaved structure for a high-voltage planar transformer for a Travelling-Wave Tube," 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), Hefei, 2016, pp. 3695-3701.
[14] Z. Ouyang and M. A. E. Andersen, "Wide input range power converters using a variable turns ratio transformer," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 2473-2478.
[15] I. Barbi and R. Gules, "Isolated DC-DC Converters With High-Output Voltage for TWTA Telecommunication Satellite Applications," IEEE Transactions on Power Electronics, 18(4), pp.975-984, Jul. 2003.
[16] C. Chu and C. Li, "Analysis and design of a current-fed zero-voltageswitching and zero-current-switching CL-resonant push-pull dc-dc converter," IET Power Electronics, 2(4), pp.456-465, Sep. 2008.
[17] A. Weinberg and L. Ghislanzoni, "A New Zero Voltage and Zero Current Power-Switching Technique," IEEE Transactions on Power Electronics, 7(4), pp.655-665, Oct. 1992.
[18] EPC2032 - Enhancement Mode Power Transistor, EPC, 2016.
[19] C. Wang, M. Li, Z. Ouyang and G. Wang, "High Efficiency High Stepup Isolated DC-DC Converter for Photovoltaic Applications," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 2019, pp. 1273-1280. doi: 10.1109/APEC. 2019.8721916
[20] Z. Ouyang and Michael A. E. Andersen. "Overview of Planar Magnetic Technology-Fundamental Properties." IEEE Transactions on Power Electronics, vol. 29, no. 9, 2014, pp. 4888-4900.
[21] Z. Ouyang, O. Thomsen and M. A. E. Andersen, "Optimal Design and Tradeoff Analysis of Planar Transformer in High-Power DC-DC Converters," IEEE Transactions on Industrial Electronics, 59(7), pp.2800-2810, Jul. 2012.
[22] C. Fei, F. Lee and Q. Li "High-Efficiency High-Power-Density LLC Converter With an Integrated Planar Matrix Transformer for HighOutput Current Applications," IEEE Transactions on Industrial Electronics, 64(11), pp.9072-9082, Nov. 2017.
[23] Y. Dou, Z. Ouyang, P. Thummala and M. A. E. Andersen, "PCB embedded inductor for high-frequency ZVS SEPIC converter," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 98-104.
[24] Z. Ouyang, J. Zhang and W. Hurley, "Calculation of Leakage Inductance for High-Frequency Transformers," IEEE Transactions on Power Electronics, 30(10), pp.5769-5775, Oct. 2015.
[25] B. Zhao, Z. Ouyang, M. Duffy, M. A. E. Andersen and W. Hurley, "An Improved Partially Interleaved Transformer Structure for High-voltage High-frequency Multiple-output Applications," IEEE Transactions on Industrial Electronics, pp.1-1, 2018.
[26] M. Li, Z. Ouyang and M. A. E. Andersen, "HighFrequency LLC Resonant Converter With Magnetic Shunt Integrated Planar Transformer," in IEEE Transactions on Power Electronics, vol. 34, no. 3, pp. 2405-2415, March 2019.
[27] J. Zhang, Z. Ouyang, M. C. Duffy, M. A. E. Andersen and W. G. Hurley, "Leakage Inductance Calculation for Planar Transformers With a Magnetic Shunt," in IEEE Transactions on Industry Applications, vol. 50, no. 6, pp. 4107-4112, Nov.-Dec. 2014.
[28] X. Huang, J. Feng, W. Du, F. C. Lee and Q. Li, "Design Consideration of MHz Active Clamp Flyback Converter with GaN Devices for Low Power Adapter Application," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 23342341.
[29] Y. K. Lo and J. Y. Lin, "Active-Clamping ZVS Flyback Converter Employing Two Transformers," IEEE Trans. on Power Electronics, vol. 22, no. 6, 2007, pp. 2416-- 2423.
[30] J. Zhang, X. Huang, X. Wu and Z. Qian, "A High Efficiency Flyback Converter With New Active Clamp Technique," IEEE Transactions on Power Electronics, vol. 25, no. 7, pp. 1775-1785, 2010.
[31] L. Xue and J. Zhang, "Highly Efficient Secondary-Resonant Active Clamp Flyback Converter," IEEE Transactions on Industrial Electronics, vol. 65, no. 2, pp. 1235-1243, 2018.
[32] W. Li and X. He, "A Family of Isolated Interleaved Boost and Buck Converters With Winding-Cross-Coupled Inductors," in IEEE Transactions on Power Electronics, vol. 23, no. 6, pp. 3164-3173, Nov. 2008. doi: 10.1109/TPEL.2008.200476
[33] J. Lee, T. Liang and J. Chen, "Isolated Coupled-Inductor-Integrated DCDC Converter With Nondissipative Snubber for Solar Energy Applications," in IEEE Transactions on Industrial Electronics, vol. 61, no. 7, pp. 3337-3348, July 2014. doi: 10.1109/TIE.2013.2278517


Chang Wang was born in Wuhan, China, in 1994. He received the B.S.E degree in School of Electronic Information and Electrical Engineering from Shanghai Jiao Tong University (SJTU), Shanghai, China, in 2017. He is currently a research assistant working towards Power Electronics in Department of Electrical Engineering, Technical University of Denmark (DTU), Kongens Lyngby, Denmark.
His research interests include high-frequency planar magnetics, high-density high-efficiency power converters, photovoltaic (PV) energy systems and wireless charging.


Mingxiao Li received the B.S degree in electrical engineering from Chongqing University, Chongqing, China, in 2016 and M.S. degree in electrical engineering in 2018 from Technical University of Denmark, Kongens Lyngby, Denmark, where he is currently working toward the Ph.D degree in electrical engineering.

His research interests include magnetics design, modeling and integration in power supplies, resonant converters and high frequency power conversion.


Ziwei Ouyang (S'07, M'11, SM'17) received the Ph.D. degree from the Technical University of Denmark (DTU), Kgs. Lyngby, Denmark, in 2011. From 2011 to 2013, he was a Postdoc Researcher with DTU. From 2013 to 2016, he was appointed as an Assistant Professor at DTU. Since April 2016, he has been an Associate Professor with DTU. His research areas focus on high-frequency planar magnetics modeling and integration, high-density high-efficiency power converters, PV battery energy storage system, and wireless charging etc. He is currently responsible for the Power Electronics course for both undergraduate and graduate students at DTU, and he also supervised more than 40 students' Postdoc, Ph.D., and Masters projects. He has more than 60 high impact IEEE journal and conference publications, and has coauthored a book chapter on Magnetics for the Handbook of Power Electronics and currently is the holder of 8 international patents.

Dr. Ouyang was the recipient of the Young Engineer Award at PCIMAsia 2014, and the Best Ph.D. Dissertation of the Year Award 2012 in Technical University of Denmark, and several Best Paper Awards in IEEE sponsored international conferences. He has served as the session Chair in some IEEE sponsored conferences and a Reviewer for the IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS.


Gang Wang received the B.E. degree in electronic engineering from the Harbin Shipbuilding Engineering Institute, Harbin, China, in 1992.

In 1992, he joined the Yangzhou Shipborne Electronic Instruments Institute, where he was involved in the development research on power transmitter based on microwave vacuum tube. From 2003 to 2007, he was involved in the development research on radar system. In 2007, he joined the Institute of Electronics, Chinese Academy of Science, Beijing, China, where he was involved in the development research on spaceborne traveling-wave tube amplifier. His current research interests include high-voltage power electronics, resonant converters, and microwave system integration.


[^0]:    General rights
    Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

    - Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
    - You may not further distribute the material or use it for any profit-making activity or commercial gain
    - You may freely distribute the URL identifying the publication in the public portal

    If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

[^1]:    Manuscript received April 10, 2019; revised August 15, 2019, October 20, 2019 and December 4 2019; accepted December 29, 2019. (Corresponding author: Ziwei Ouyang)
    C. Wang, M. Li and Z. Ouyang are with the Department of Electrical Engineering, Technical University of Denmark, Kgs. Lyngby 2800, Denmark (e-mail: chawa@elektro.dtu.dk; mingxli@elektro.dtu.dk; zo@elektro.dtu.dk).
    G. Wang is with the Institute of Electronics, Chinese Academy of Science, Beijing 100190, China. (e-mail: wanggang@ie.ac.cn).

