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***Abstract*—Beat phenomenon is an important issue for the practical application of electrolytic capacitorless motor drives. In this study, the characteristics of stator current harmonics caused by the voltage sampling delay are analyzed. Further, the beat phenomenon generated from the interaction between the harmonics and the fundamental currents is investigated, and the envelope feature of the stator current is derived mathematically. For the purpose of suppressing the beat phenomenon, a voltage reconstruction strategy is proposed to reduce the influence of DC link voltage sampling delay at the six times of grid frequency. By utilizing the reconstructed DC link voltage for calculation of PWM duty ratio, the beat phenomenon can be attenuated significantly. The proposed method can be integrated into motor control system easily. Experimental results show the effectiveness of the proposed strategy in a prototype of electrolytic capacitorless permanent magnet synchronous motor drive.**

***Index Terms*—Beat phenomenon, DC link voltage sampling delay, electrolytic capacitorless, motor drive, voltage reconstruction.**

I. INTRODUCTION

Permanent magnet synchronous motors (PMSMs) have been widely applied in white goods, transportation and other industrial applications [1]. The electrolytic capacitors in the DC link reduce the service lifetime of the motor drives especially in applications with extreme operational conditions such as high environment temperature [2]-[3]. Consequently, drives utilizing only film capacitors will improve the reliability and ultimately reduce the cost of ownership for drive system. Nowadays, the single-phase input electrolytic capacitorless

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motor drives have been successfully used in heating, ventilation and air conditioning (HVAC) system [4]-[5]. Three-phase input diode rectifier motor drives equipped with slim film capacitors also have gained attention in recent years [6]-[8].

Once the large volume electrolytic capacitors are replaced with slim film capacitors, the energy coupling between the grid side and motor side becomes significant. Issues can be classified into power quality of the grid side and performance of the motor side. From the point view of power quality of the grid side, the system may be unstable due to the *LC* resonance [9]-[12], and contributes to the power quality pollution of a grid. Considering performance of the motor side, the inverse proportional correlation can be seen between the DC link voltage utilization rate and the torque ripple constrains in high-speed region [13]-[15]. With the demand of practical applications, DC link overvoltage protection is a key issue that needs to be considered in electrolytic capacitorless motor drives [16]-[17]. Negative impact on the operation of motor drive, commonly referred as to beat phenomenon includes severe current distortion, additional noise and power losses, which must be addressed before such drives can deliver on the promise of lower cost of ownership.

Beat phenomenon is one of the primary problems for practical applications of the reduced DC link capacitance motor drives and other power electronic converters [18]-[21]. The power converters usually show low impendence at low frequency region, where even small low-frequency perturbations can cause significant waveform distortion. Currently, the researches of the beat phenomenon in motor drives are mainly focused on AC-fed railway traction drives. The low-frequency beat phenomenon is caused by the interaction of DC link voltage and inverter output voltage, when their frequencies get close to each other [22]-[23]. Solutions for beat phenomenon can be classified into class of hardware and class of control algorithm solutions. For hardware solutions, an additional *LC* resonant circuit can be employed and connected in parallel to the DC link capacitors where the resonant frequency is tuned to match the fluctuation frequency of the DC link voltage, absorbing energy of oscillation and dumping these at the same time. However, both the cost and volume of the system will obviously be negatively affected due to the additional capacitor and inductor.

The solution based on control algorithms are preferred

considering the system cost and practical application. By fast control of the motor current, the beat phenomenon can be effectively mitigated [24]. However, this kind of feedback control is difficult to achieve due to numerus system delay, such as the limited bandwidth of current and voltage loops. To address these shortcomings, several feedforward compensation methods have been proposed by extracting the fluctuating component in the DC link voltage and applying it inversely for the PWM process [25]. This kind of methods have been proved to be simple and effective. But the accurate and fast DC link voltage sampling/feedback is a critical issue.

In [26], a beat suppression method was proposed by compensating the DC link voltage using a repetitive predictor. It is an effective strategy for railway traction drives with PWM rectifier. However, in the electrolytic capacitorless motor dives with three-phase diode front end rectifier, the DC link voltage does not show ideal periodical characteristics, so the repetitive predictor is difficult to predict DC link voltage effectively. In [27], the beat phenomenon generated from the fluctuated DC link voltage and fluctuated motor load was investigated in single-phase AC input electrolytic capacitorless drives. The beat phenomenon was effectively suppressed by power balancing controller which led to significant reduction in audible noise of the drives. In [28], two kinds of beat phenomenon in PMSM drive during over-modulation were discussed. By modifying the carrier and shifting the modulation waves, these two kinds of beat phenomenon were restrained.

In this paper, a novel beat phenomenon suppression strategy with DC link voltage reconstruction is proposed for the electrolytic capacitorless motor drives. In general-purpose drives, the switching and sampling frequency of IGBT are set to several kHz and is the same i.e one sample of inputs per switching period. The stator current harmonics caused by the acquisition and sampling delay of DC link voltage feedback are investigated, which is seldom included in published researches. First of all, the mathematical description of beat phenomenon is first described quantitatively to explain the beat frequency. Then, in order to suppress the beat phenomenon caused by the interaction of stator current harmonics and its fundamental value, a DC link voltage reconstruction method is proposed for the calculation of the PWM duty ratio.

This paper proceeds as follows: the analysis of beat phenomenon in electrolytic capacitorless PMSM drives is presented in Section II. Section III introduces the proposed beat phenomenon suppression strategy. The experimental results verifying the proposed algorithm are discussed in Section IV.

II. ANALYSIS OF BEAT PHENOMENON IN ELECTROLYTIC CAPACITORLESS PMSM DRIVES

A. Stator Current Harmonics Caused by DC link Voltage

The three-phase diode rectifier PMSM drive with reduced DC link capacitance is shown in Fig. 1. For the electrolytic capacitorless PMSM drive, the DC link voltage cannot be maintained as a constant, due to the largely reduced DC link capacitance and can be expressed as [6]

$$u_{dc} = u_{dN}\left[1 - \sum_{n=1}^{\infty} \frac{2}{(6n)^2 - 1}\cos\left(6\omega_g nt\right)\right], \qquad (1)$$

$$u_{dN} = \frac{3\sqrt{3}}{\pi}u_{peak} \qquad (2)$$

where $n=1, 2, 3 \ldots$, ω_g is the grid frequency, u_{peak} is the peak value of grid phase voltage, and u_{dN} is the DC component of u_{dc}.

Figure 2 shows the typical time sequence of sampling, calculation and PWM output [29]. The algorithm takes a logical sequential step that yields the PWM signals after the execution of algorithm. For the nth sampling point, the DC link voltage is obtained at the peak of the carrier, and the control algorithm is executed between the nth and the $(n+1)$th sampling points, then the sampled DC link voltage (u_{dc_s}) is kept as a constant at the beginning of the $(n+1)$th sampling point. When applying the time sequence, the PWM output is inherently delayed by $0.5T_s$. Therefore, the total DC link voltage delay, which is the sum of calculation delay and PWM delay shown in Fig. 2, is $1.5T_s$ represented as equivalent sampled DC link voltage (u_{dc_e}). It should be notice that, this paper is carried out based on this typical modulation, and other modulation might have different consideration.
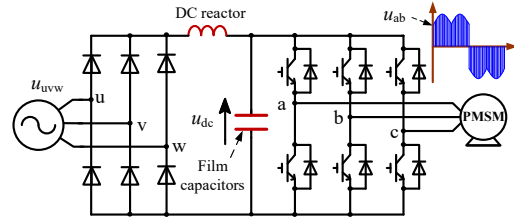

Fig. 1. Three-phase diode rectifier PMSM drive with reduced DC link capacitance.
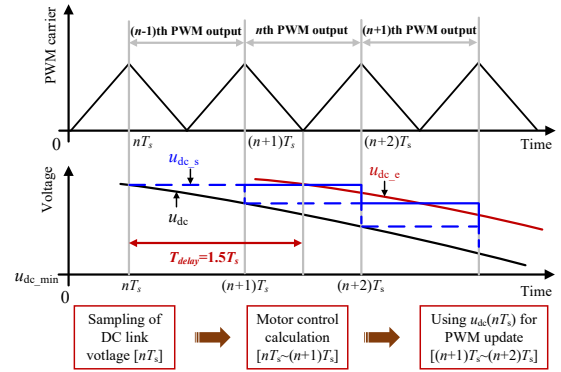
Fig. 2 Time sequence of sampling, calculation and PWM output.

Considering the influence of delay, the equivalent sampled DC link voltage can be expressed as

$$u_{dc\_e} = u_{dN}\left[1 - \sum_{n=1}^{\infty} \frac{2}{(6n)^2 - 1}\cos\left(6\omega_g nt - n\varphi_d\right)\right]. \qquad (3)$$

Compared to (1), (3) has an addition of phase delay, φ_d, which donates the DC link voltage sampling delay.

The DC link voltage contains different frequency components such as $6\omega_g$, and $12\omega_g$. In this study, the component of $6\omega_g$ is analyzed in detail, since it has significant influence on beat phenomenon. Considering (3), the output voltages of inverter can be expressed as [10],

$$\vec{u}_{abc} \doteq \frac{\left[1 - \frac{2}{35}\cos\left(6\omega_g t\right)\right]}{\left[1 - \frac{2}{35}\cos\left(6\omega_g t - \varphi_d\right)\right]}\vec{u}_{abc\_ref} \qquad (4)$$

where $\vec{u}_{\text{abc}}$ is the stator voltage vector using equivalent sampled DC link voltage signal, and $\vec{u}_{\text{abc\_ref}}$ is the reference of the stator voltage vector.

Then, (4) can be re-written as

$$\vec{u}_{\text{abc}} = \frac{1 + \frac{2}{35}\cos\left(6\omega_g t - \varphi_d\right) - \frac{2}{35}\cos\left(6\omega_g t\right)}{1 - \left(\frac{2}{35}\right)^2 \cos^2\left(6\omega_g t - \varphi_d\right)} \vec{u}_{\text{abc\_ref}} . \quad (5)$$

As quadratic terms in (5) have very small contributions, (5) could be simplified further by neglecting yielding

$$\vec{u}_{\text{abc}} = \left[1 + \frac{4}{35}\sin\left(\varphi_d\right)\sin\left(6\omega_g t - \frac{\varphi_d}{2}\right)\right]\vec{u}_{\text{abc\_ref}} . \quad (6)$$

As can be seen, $\vec{u}_{\text{abc}} = \vec{u}_{\text{abc\_ref}}$ if there is no sampling delay, i.e. $sin(\varphi_d)=0$.

Using Clark-Park transformation, the dq-axis synchronous reference frame voltages can be expressed as

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} |\vec{u}_{\text{abc\_ref}}|\left[1 + \frac{4}{35}\sin\left(\varphi_d\right)\sin\left(6\omega_g t - \frac{\varphi_d}{2}\right)\right]\sin(\varphi_e) \\ -|\vec{u}_{\text{abc\_ref}}|\left[1 + \frac{4}{35}\sin\left(\varphi_d\right)\sin\left(6\omega_g t - \frac{\varphi_d}{2}\right)\right]\cos(\varphi_e) \end{bmatrix} . \quad (7)$$

As can be seen in (7), $u_{d,q}$ not only contains a DC component, but also are influenced by the fluctuation of DC link voltage. Similarly, the currents of motor in dq-axis reference system can be expressed as following

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} i_{d0} + i_{d1}\sin\left(6\omega_g t - \frac{\varphi_d}{2} + \varphi_{id}\right) \\ i_{q0} + i_{q1}\sin\left(6\omega_g t - \frac{\varphi_d}{2} + \varphi_{iq}\right) \end{bmatrix} \quad (8)$$

where i_{d0}, i_{q0} are the steady state (i.e. DC) components of i_d and i_q, while i_{d1}, i_{q1} are the fundamental amplitudes of i_d and i_q caused by DC voltage fluctuations. The φ_{id} is the phase difference between u_d and i_d, φ_{iq} is the phase difference between u_q and i_q. Consequently, the a-phase current can be expressed as

$$i_a = i_{d0}\cos(\omega_e t) - i_{q0}\sin(\omega_e t) -$$

$$i_{d1}\begin{bmatrix} \frac{1}{2}\sin\left(\omega_e t + 6\omega_g t - \frac{\varphi_d}{2} + \varphi_{id}\right) \\ + \frac{1}{2}\sin\left(6\omega_g t - \omega_e t - \frac{\varphi_d}{2} + \varphi_{id}\right) \end{bmatrix} +$$

$$i_{q1}\begin{bmatrix} \frac{1}{2}\cos\left(\omega_e t + 6\omega_g t - \frac{\varphi_d}{2} + \varphi_{iq}\right) \\ -\frac{1}{2}\cos\left(6\omega_g t - \omega_e t - \frac{\varphi_d}{2} + \varphi_{iq}\right) \end{bmatrix} . \quad (9)$$

From (9), it can be seen that the phase current contains terms with three distinct frequencies. The additional two terms with frequencies $6\omega_g-\omega_e$ and $6\omega_g+\omega_e$ are result of a sampling delay of the DC link voltage. In Part B, the generation of the beat phenomenon will be presented.

B. Beat Phenomenon Caused by the Interaction of Harmonics and the Fundamental Currents

Any two sinusoidal signals with individual frequencies with no integer multiple, will result in beat phenomenon. Two terms in (9) can be expressed as,

$$i_{a\_p}(t) = F_1(t) + F_2(t)$$

$$= i_{d0}\cos(\omega_e t) + \frac{1}{2}i_{q1}\cos\left(\omega_e t + 6\omega_g t - \frac{\varphi_d}{2} + \varphi_{iq}\right) \quad (10)$$

where $F_1(t)$ is a component at the motor operation frequency, and $F_2(t)$ is a component caused by the DC link voltage fluctuation. In order to describe the beat phenomenon, it is important to estimate the amplitude envelope of $i_{a\_p}(t)$ expressed with (10), which is denoted as $i_{a\_pe}(t)$ and shown in Fig. 3(a).

Obtaining the generic expression for $i_{a\_pe}(t)$ is not trivial. Fig. 3 illustrates the beat phenomenon under different values of $|F_2(t)|/|F_1(t)|$, in which the angular frequency of $F_1(t)$ is $(2\pi*74)$ rad/s (ω_e) and the frequency of $F_2(t)$ is $(2\pi*(74+300))$ rad/s ($\omega_e+6\omega_g$), assuming that the grid frequency is 50Hz.

As shown in the zoomed view of Fig.3(a), $F_1(t)$ and $F_2(t)$ are the peak and the valley values respectively at the time point of $t=t_0=0.5$s, and the envelope still goes through the local maximum of $i_{a\_p}(t)$. Thus, it can be inferred that the envelope will go through $i_{a\_p}(t)$ at any time point of $t_0 \pm nT_1$, and this is the basis to derive the quantifiable function of $i_{a\_pe}(t)$. However, the envelope does not go through $i_{a\_p}(t)$ at the time point of $t=t_0$ since $i_{a\_p}(t)$ is not a local maximum value at this time point, while $|F_2(t)|/|F_1(t)|$ increases to 0.1 as shown in the zoomed Fig. 3(b). Therefore, it is hard to determine the function of $i_{a\_pe}(t)$ under this condition.

Hence, the precondition to obtain the function of $i_{a\_pe}(t)$ is that the 2nd derivative of $i_{a\_p}(t)$ should less than 0 at the time point of $t=t_0$,

$$i_{a\_p}(t_0)'' = -i_{d0}\omega_e^2\cos(\omega_e t_0)$$

$$-\frac{1}{2}i_{q1}\left(\omega_e + 6\omega_g\right)^2\cos\left(\omega_e t_0 + 6\omega_g t_0 - \frac{\varphi_d}{2} + \varphi_{iq}\right) . \quad (11)$$

$$< 0$$

considering (12),

$$\begin{cases} \cos(\omega_e t_0) = 1 \\ \cos\left(\omega_e t_0 + 6\omega_g t_0 - \frac{\varphi_d}{2} + \varphi_{iq}\right) = -1 \end{cases} . \quad (12)$$

Consequently, the envelope is formed by the local maximum value of $i_{a\_p}(t)$, when $F_1(t)$ and $F_2(t)$ meet the following constrain,

$$\frac{i_{q1}}{2i_{d0}} < \left(\frac{\omega_e}{\omega_e + 6\omega_g}\right)^2 . \quad (13)$$

Since the envelope will go through $i_{a\_p}(t)$ at time point of $t_0 \pm nT_1$, the next step is to investigate the periodic characteristics of $i_{a\_p}(t)$. In this analysis, the operation frequency ($\omega_e/2\pi$) is assumed to be an integer for easer understanding. The $i_{a\_p}(t)$ consists of two signals, the value of $i_{a\_p}(t)$ at $t=t_0$ will appear again at $t=t_0+1$s, since the state will repeat at the time point that the two signals go through integer

multiple periods, when $\omega_e/2\pi$ is higher than 1Hz. In other words, $F_1(t)$ and $F_2(t)$ will go through 74 periods and 374 periods respectively within 1s to repeat $i_{a\_p}(t)$, if the frequency of $F_1(t)$ and $F_2(t)$ are 74Hz and 374Hz. Thus, the period of $i_{a\_p}(t)$ can be expressed as

$$T_{a\_p} = \cfrac{1}{\left(\cfrac{\omega_e}{2\pi}, \cfrac{(\omega_e + 6\omega_g)}{2\pi}\right)} \qquad (14)$$

where (a, b) is the maximum common divisor operator.

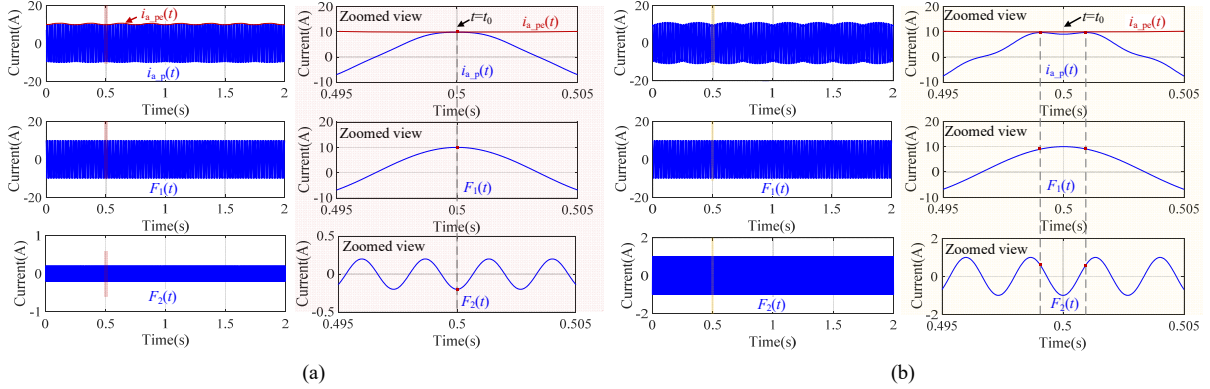Times of $F_1(t)$ appears in a period of $i_{a\_p}(t)$ can be denoted as

Fig. 3 Beat phenomenon under different values of $|F_2(t)|/|F_1(t)|$. (a) $|F_2(t)|/|F_1(t)|$=0.02. (b) $|F_2(t)|/|F_1(t)|$=0.1. Top row illustrates the sum of $F_1(t)$ and $F_2(t)$ while the middle and bottom row of figures shows $F_1(t)$ and $F_2(t)$ respectively.

$$p = \frac{T_{a\_p}}{T_1}. \qquad (15)$$

Thus, during a period of $i_{a\_p}(t)$, the envelope is made up of the following points

$$\begin{cases} i_{a\_p}(t_0 + T_1) = i_{d0} + \dfrac{1}{2} i_{q1} \cos\left[(t_0 + T_1)(\omega_e + 6\omega_g) - \dfrac{\varphi_d}{2} + \varphi_{iq}\right] \\[2mm] i_{a\_p}(t_0 + 2T_1) = i_{d0} + \dfrac{1}{2} i_{q1} \cos\left[(t_0 + 2T_1)(\omega_e + 6\omega_g) - \dfrac{\varphi_d}{2} + \varphi_{iq}\right] \\[2mm] \qquad\qquad\qquad\qquad ... \\[2mm] i_{a\_p}(t_0 + pT_1) = i_{d0} + \dfrac{1}{2} i_{q1} \cos\left[(t_0 + pT_1)(\omega_e + 6\omega_g) - \dfrac{\varphi_d}{2} + \varphi_{iq}\right] \end{cases}$$
$$(16)$$

A conclusion can be derived from (14), (15) and (16) that if the harmonic frequency is an integer multiple of the fundamental frequency, the beat phenomenon will not appear. The common divisor of $\omega_e/2\pi$ and $(\omega_e+6\omega_g)/2\pi$ is $\omega_e/2\pi$, and p=1 since $T_{a\_p}=T_1$. Thus, the envelope of $i_{a\_p}(t)$ is $i_{a\_p}(T_1)$, which is a constant value.

The envelope of $i_{a\_p}(t)$ can be approximately expressed as follows if considering (16),

$$i_{a\_pe} = i_{d0} + \frac{1}{2} i_{q1} \cos(\omega_{a\_pe} t + \varphi_{a\_pe}) \qquad (17)$$

where ω_{a_pe} is the frequency of the envelope, and φ_{a_pe} is the initial phase of the envelope.

As it can be seen in (17), the primary task is to obtain ω_{a_pe} for the description of beat phenomenon. For this purpose, it is important to figure out the rule of phase shift of $F_2(t)$ at time points of t_0+nT_1, since ω_{a_pe} is determined by the period of the phase shift. Defining the phase shift of $F_2(t)$=0 at $t=t_0$, then the proportion of the phase shift at t_0+T_1 can be denoted as

$$b_d = \left\{ \frac{\omega_e + 6\omega_g}{\omega_e} \right\} \qquad (18)$$

where $\{x\}$ is the decimal part function, b_d is the proportion of phase shift at $t= t_0+T_1$.

Considering the periodical character of $F_2(t)$, redefining the proportion of phase shift as

$$b = \begin{cases} b_d & 0 \le b_d \le 0.5 \\ 1 - b_d & 0.5 < b_d < 1 \end{cases}. \qquad (19)$$

Consequently, the phase shift of $F_2(t)$ at the time point of t_0+nT_1 can be expressed as

$$\varphi_s(t_0 + nT_1) = 2\pi n b. \qquad (20)$$

As the analysis shown above, the times of $F_1(t)$ appear in T_{a_p} is p, then the frequency of the envelope can be represented as

$$\omega_{a\_pe} = \frac{2\pi p b}{T_{a\_p}}. \qquad (21)$$

Since the beat phenomenon is related to the sampling delay of the fluctuated DC link voltage, the suppression method is designed accordingly in the next section.

III. PROPOSED BEAT PHENOMENON SUPPRESSION STRATEGY WITH VOLTAGE RECONSTRUCTION

The block diagram of the proposed beat phenomenon suppression strategy is shown in Fig. 4. The proposed compensation strategy is integrated with sensorless vector control, by modifying the sampled DC link voltage signal used for PWM generation. Since the strategy only relates to the DC link voltage and the PWM sampling period, it can be integrated into the motor control system easily.

A. DC Link Voltage Reconstruction

The beat phenomenon caused by the DC link voltage sampling delay mainly at the frequency of $6\omega_g$=1884rad/s, so the primary task is to minimize its sampling error.

Figure 5 shows the beat frequency considering the experimental prototype. When the motor frequency changes from 0 to 628rad/s (the rated frequency is 471rad/s), the beat

frequency will not exceed 282rad/s. The center frequency of the bandpass filter is designed at 1884rad/s to obtain the $6\omega_g$ frequency component in the DC link voltage, which is far away from the beat frequency.

Figure 6 shows the schematic diagram of the reconstruction of $6\omega_g$ component in DC link voltage. For the nth sampling point, the sampling signal of the $6\omega_g$ component in DC link voltage represented as $u_{dc\_s\_6\omega g}(z)$ is kept for two switching periods, which is used for the nth PWM output and the error can be described as the area of MNOP. If the average voltage during the nth PWM output is obtained, the error can be reduced effectively. Thus, obtaining the average value of the $6\omega_g$ component in DC link voltage during $(n+1)T_s$ and $(n+2)T_s$ at the nth sampling point is the purpose for the correction of DC link voltage.
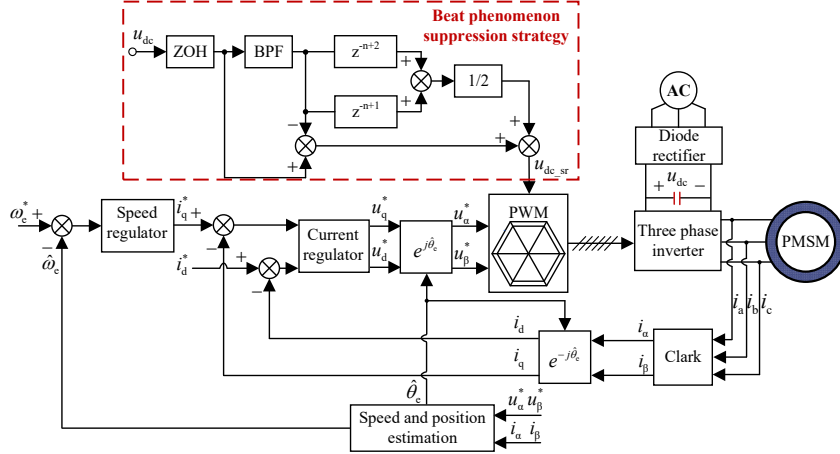

Fig. 4. Block diagram of vector control system based on the beat phenomenon suppression strategy.
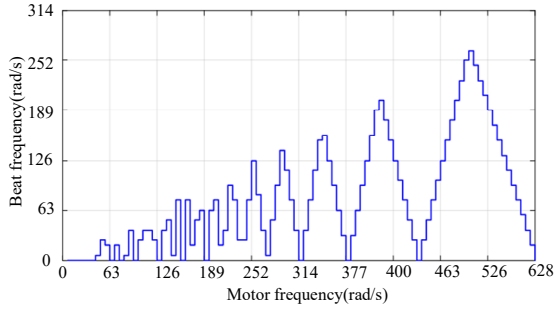

Fig. 5 Relationship between the motor frequency and the beat frequency.

Using the periodical characteristic of $u_{dc\_6\omega g}(z)$, the signals that one step and two steps ahead of $u_{dc\_6\omega g}(z)$ can be obtained as $u_{dc\_s\_6\omega g}(z)z^{-n+1}$ and $u_{dc\_s\_6\omega g}(z)z^{-n+2}$, respectively. Thus, the expected voltage at the time of $(n+1.5)T_s$ can be reconstructed using $u_{dc\_s\_6\omega g}(z)z^{-n+1}$ and $u_{dc\_s\_6\omega g}(z)z^{-n+2}$ at the time of nT_s, since the $u_{dc\_6\omega g}(t)$ can be regarded as a linear function during a switching period,

$$u_{dc\_s\_6\omega_g r}(z) = \frac{\left(u_{dc\_s\_6\omega_g}(z)z^{-n+2} + u_{dc\_s\_6\omega_g}(z)z^{-n+1}\right)}{2}, \quad (22)$$

$$n = \frac{kf_s}{6f_g} \quad (23)$$

where $u_{dc\_s\_6\omega g r}(z)$ is the reconstructed voltage at the frequency of $6\omega_g$, f_s is the switching frequency, k is a coefficient determined by f_s and f_g. The selection of k should ensure n as a minimum positive integer. For example, if f_s=6kHz, and f_g=50Hz, then k should be 1. If f_s=8kHz, k should be 3.

The $u_{dc\_s\_6\omega g}(z)$ is derived as

$$u_{dc\_s\_6\omega_g}(z) = B(z)u_{dc\_s}(z) \quad (24)$$

where B(z) is a bandpass filter, and its center frequency is $6\omega_g$. The $u_{dc\_s}(z)$ is the raw sampled DC link voltage.

Considering the experimental platform, B(z) is designed as

$$B(z) = \frac{0.0078z^2 - 0.0078}{z^2 - 1.9296z + 0.9844}. \quad (25)$$

Finally, the voltage used for the algorithm calculation and the PWM update can be obtained by replacing $u_{dc\_6\omega g}(z)$ with $u_{dc\_6\omega g r}(z)$.

$$u_{dc\_sr}(z) = u_{dc\_s}(z) - u_{dc\_s\_6\omega_g}(z) + u_{dc\_s\_6\omega_g r}(z) \quad (26)$$

where u_{dc_sr} is the reconstructed DC link voltage used in SVPWM calculation.

The realized duty ratio will be inaccurate due to the delay of the sampled DC link voltage, which causes the error in the output voltage of inverter. Figure 7 shows the relationship between the DC link voltage and the duty ratio in a PWM period. The volt-second integration of the inverter output voltage is equal to the volt-second integration of expected output phase voltage $u_a^*(t)$ which is denoted as S. Taking the voltage at the time of $(n+1.5)T_s$ to calculate the duty ratio, where the expression for S, i.e. volt-second integration of the inverter output voltage can be defined as (27), and it can be simplified to

$$S = u_{dc\_6\omega_g}\left[(n+1.5)T_s\right] \cdot \left(t_{on1} - 0.5T_s\right). \quad (28)$$
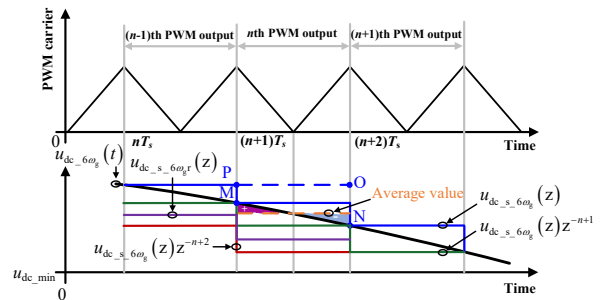

Fig. 6 Schematic diagram of the reconstruction of $6\omega_g$ component in DC link voltage.

$$S=\int_{(n+1)T_s}^{(n+2)T_s} u_a^*(t)\, dt = \int_{(n+1)T_s}^{t_1} -\frac{1}{2}u_{\text{dc}\_6\omega_g}\left[(n+1.5)T_s\right]dt + \int_{t_1}^{t_2}\frac{1}{2}u_{\text{dc}\_6\omega_g}\left[(n+1.5)T_s\right]dt + \int_{t_2}^{(n+2)T_s} -\frac{1}{2}u_{\text{dc}\_6\omega_g}\left[(n+1.5)T_s\right]dt . \quad (27)$$

$$t_{\text{on}1} = \frac{S}{u_{\text{dc}\_6\omega_g}\left[(n+1.5)T_s\right]} + \frac{1}{2}T_s = \frac{|u_s|\cos\left[\omega_e(n+1)T_s+\varphi_e\right] - |u_s|\cos\left[\omega_e(n+2)T_s+\varphi_e\right]}{\omega_e\cdot u_{\text{dc}\_6\omega_g}\left[(n+1.5)T_s\right]} + \frac{1}{2}T_s , \quad (29)$$

The ON duration can be expressed as (29), and it can be simplified as

$$t_{\text{on}1} \doteq \frac{|u_s|\cdot T_s\cdot \sin\left[\omega_e(n+1.5)T_s+\varphi_e\right]}{u_{\text{dc}\_6\omega_g}\left[(n+1.5)T_s\right]} + \frac{1}{2}T_s . \quad (30)$$

Similarly, the duty ratio can be also derived using the DC link voltage at the time of nT_s

$$d_2 = \frac{t_{\text{on}2}}{T_s} = \frac{|u_s|\cdot \sin\left[\omega_e(n+1.5)T_s+\varphi_e\right]}{u_{\text{dc}\_6\omega_g}(nT_s)} + \frac{1}{2} . \quad (32)$$

Considering (32) and (33), the error of the duty ratio can be obtained as

$$d_{\text{error}} = \frac{|u_s|\cdot \sin\left[\begin{array}{c}\omega_e(n+1.5)T_s\\ +\varphi_e\end{array}\right]\cdot\left[\begin{array}{c}u_{\text{dc}\_6\omega_g}(nT_s)\\ -u_{\text{dc}\_6\omega_g}(n+1.5)T_s\end{array}\right]}{u_{\text{dc}\_6\omega_g}(nT_s)\cdot u_{\text{dc}\_6\omega_g}\left[(n+1.5)T_s\right]} . \quad (33)$$
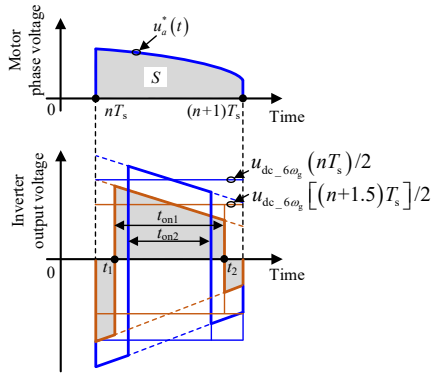

Fig. 7. Relationship between DC link voltage and duty ratio in a PWM period.

B. Discussion on the value of DC Link Capacitance Considering Switching Ripple

In practice, the choice of the value of DC link capacitance should consider the influence on the DC voltage ripple. The corresponding high-frequency model can be derived as shown in Fig. 8, and the state equation of the high frequency motor drive model can be described as

$$\begin{cases} i_{\text{inv}\_h} = i_{\text{dc}\_h} + i_{\text{g}\_h} \\ u_{\text{dc}\_h} = R_g i_{\text{g}\_h} + u_{\text{L}\_h} \\ i_{\text{dc}\_h} = C_{\text{dc}} s u_{\text{dc}} \\ u_{\text{L}\_h} = L_{\text{dc}} i_{\text{g}\_h} \end{cases} \quad (34)$$

where R_g is the line resistance, L_{dc} is the DC inductance, C_{dc} is the DC link capacitance, i_{inv_h} is the high frequency inverter input current, i_{dc_h} is the high frequency DC link current, i_{g_h} is the high frequency grid side current, u_{dc_h} is the high frequency DC link voltage, and u_{L_h} is the high frequency inductor voltage.

Then, the transfer function can be derived as

Consequently, the duty ratio can be derived using the DC link voltage at the time of $(n+1.5)T_s$.

$$d_1 = \frac{t_{\text{on}1}}{T_s} = \frac{|u_s|\cdot \sin\left[\omega_e(n+1.5)T_s+\varphi_e\right]}{u_{\text{dc}\_6\omega_g}\left[(n+1.5)T_s\right]} + \frac{1}{2} . \quad (31)$$

$$\frac{u_{\text{dc}\_h}}{i_{\text{inv}\_h}} = \frac{L_{\text{dc}}s + R_g}{L_{\text{dc}}C_{\text{dc}}s^2 + R_g C_{\text{dc}}s + 1} . \quad (35)$$

Figure 9 shows the Bode diagram of the transfer function corresponding to the parameters of the experimental platform. As can be seen, with the reduction of the DC link capacitance, the magnitude of the Bode diagram will increase. That means the switching harmonics in the DC link capacitor will increase along with the decrease of capacitance.
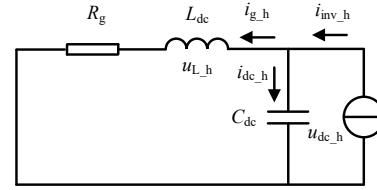

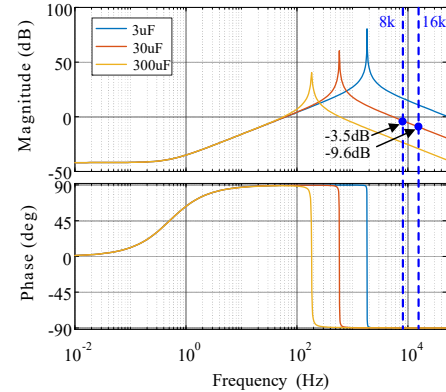Fig. 8 High frequency model of the motor drive system.

Fig. 9 Bode diagram of the high frequency model.

In this study, the DC link capacitance is chosen as 30uF, and the switching ripple in the DC link voltage can be ignored. Thus, the proposed beat suppression method can work effectively.

IV. EXPERIMENTAL RESULTS

The proposed beat phenomenon suppression strategy is verified on a 5.5-kW electrolytic capacitorless PMSM drive shown in Fig. 10. A 30uF film capacitor and a 2.5mH DC link reactor are used. The AC input of the inverter is 380-Vrms (50 Hz). The motor parameters of L_d, L_q, R_s are 7.5mH, 17.2mH and 0.265Ω, respectively. The rated power of the motor is 5.5kW, and the rated frequency is 75Hz. The load PMSM works as a generator with the output connected to the resistance. All algorithms are implemented in a DSP28335 chip. The inverter switching frequency is set to 8 kHz, the same as the current sampling frequency. The bandwidth of the current loop is designed as 300Hz, and the controller parameters are set as

kp=6, ki=80. The bandwidth of the hardware low pass filter is designed as 300kHz for DC link voltage sampling.

Figure 11 shows the experimental results at the operating frequency of 464rad/s and the motor output power of 5.5kW. As can be seen in Fig. 11(a), the a-phase current shows obvious beat phenomenon without suppression strategy. The beat frequency is 25rad/s, which is in accordance with the theoretical analysis presented in section II. After using proposed method, beat phenomenon is mitigated significantly. By comparing Fig. 11(b) and (c), the amplitude of fluctuating component at 1884rad/s in q-axis current is reduced after using the described method. Quantitatively, the harmonic peak-to-valley value is reduced from 3.5A to 1.5A. Fig. 11(d) and (e) compare the harmonic in the a-phase current quantitatively. After applying the control strategy, the harmonics at the frequency of 1420rad/s and 2348rad/s have been reduced from 0.72A and 0.43A to 0.24A and 0.13A, respectively.
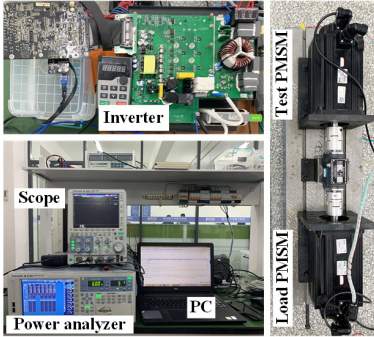

Fig. 10. Experimental setup of the 5.5-kW PMSM drive equipped with slim film capacitor.

The experimental results during acceleration process are shown in Fig. 12 to verify the effectiveness of the beat suppression strategy during transient. The q-axis current changes from 10A to 12.5A during 0.8s as shown in Fig. 12, and the motor current does not show beat phenomenon during transient process after applying the beat suppression strategy.

Figure 13 shows more experimental results when applying the proposed beat phenomenon suppression strategy. Figure 13(b) and (c) are the zoomed view of Fig. 13(a) before and after adopting the suppression strategy. As can be seen, the torque ripple can be reduced effectively after applying the suppression strategy. In Fig. 13(d) and (e), after applying the beat suppression strategy, the harmonic frequency in stator current at 1506rad/s and 2260rad/s can be reduced effectively. Fig. 13(g) and (h) show the FFT analysis of the motor speed. By applying the beat suppression strategy, the speed harmonics at the DC link voltage fluctuation frequency (1884rad/s) can be reduced to 20%. Also, the THD of the input current can be reduced slightly from 63% to 58%.
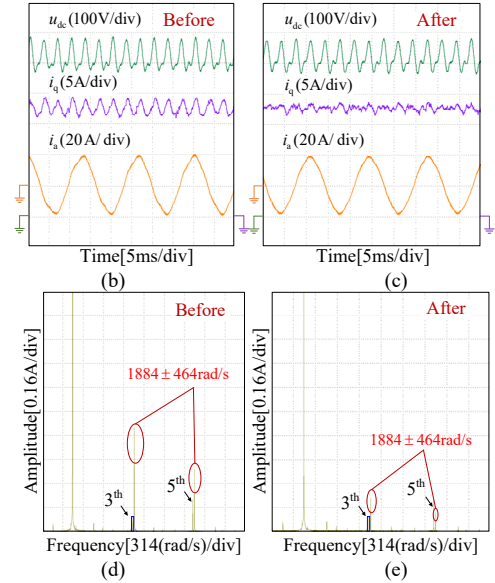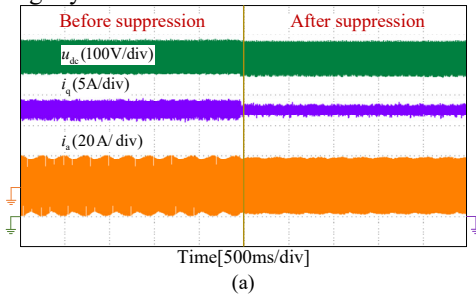

Fig. 11. Experimental results at the operating frequency 74Hz(5.5kW). (a) DC link voltge, q-axis current and a-phase current. (b) Zoomed view of (a) before applying suppression strategy. (c) Zoomed view of (a) after applying suppression strategy. (d) FFT analysis of a-phase current before applying suppression strategy. (e) FFT analysis of a-phase current after applying suppression strategy.
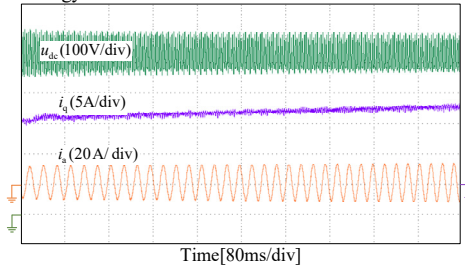

Fig. 12 Experimental results of dynamic process after applying beat suppression strategy.

The proposed beat phenomenon suppression strategy can achieve satisfactory effect in wide power range. Fig. 14 shows the experimental statistics of stator current harmonics at different motor output power. After applying the beat phenomenon suppression strategy, the current harmonics at the frequency of $6\omega_g-\omega_e$ and $6\omega_g+\omega_e$ can be reduced remarkably.
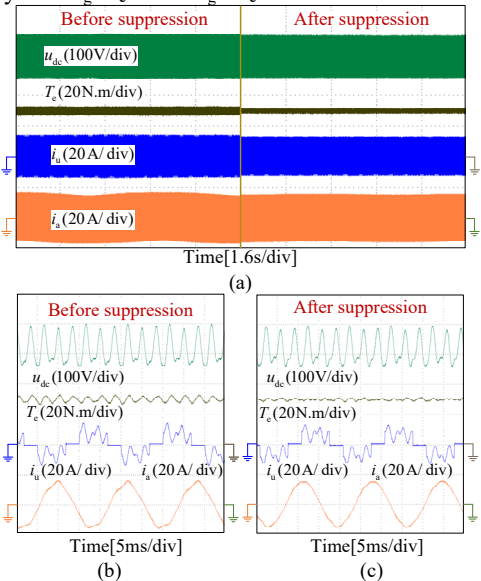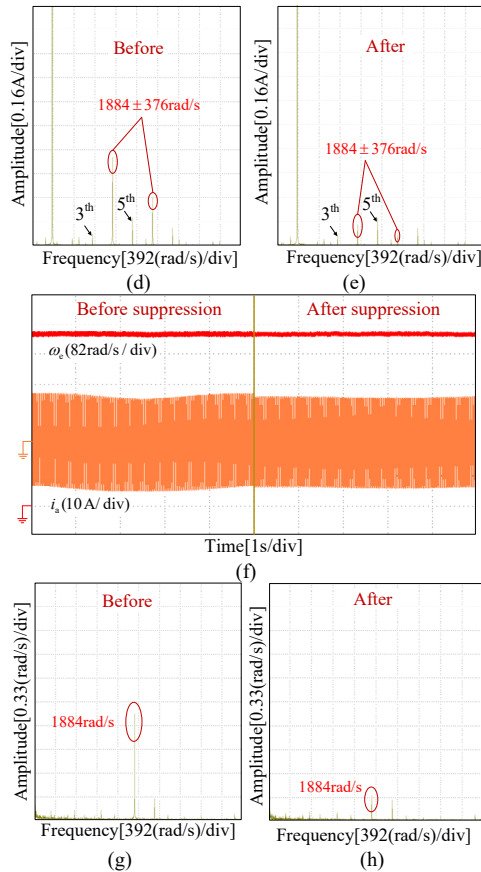
Fig. 13 Experimental results at the frequency of 60Hz. (a) DC link voltage, electromagnetic torque, u-phase input current, and a-phase motor current. (b) Zoomed view of (a) before applying suppression strategy. (c) Zoomed view of (a) after applying suppression strategy. (d) FFT analysis of a-phase current before applying suppression strategy. (e) FFT analysis of a-phase current after applying suppression strategy. (f) Motor speed. (g) FFT analysis of motor speed before applying suppression strategy. (h) FFT analysis of motor speed after applying suppression strategy.
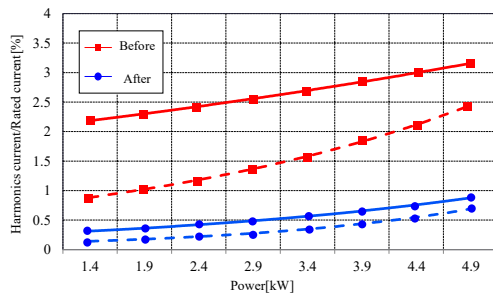

Fig. 14. Experimental statistics of stator current harmonics at different motor output power.

V. CONCLUSION

This paper focuses on the analysis and suppression of beat phenomenon in three-phase diode rectifier PMSM drives equipped with slim film capacitors. The sampling delay of the DC link voltage causes obvious beat phenomenon in stator currents. In this study, the envelope feature of the stator current is derived mathematically, which is a theoretical contribution. To tackle the beat phenomenon in electrolytic capacitorless PMSM drives, a DC link voltage reconstruction strategy is proposed by reducing the time delay of its main fluctuation component. By using the reconstructed voltage for the PWM

ratio duty calculation, the beat phenomenon is effectively reduced. The proposed method can work effectively when the grid frequency diverging is within small range. In the future, the frequency adaptive ability of the proposed method will be investigated when the grid is non-ideal.

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