Digital control of multiphase Series Capacitor Buck converter prototype for the powering of HL-LHC Inner Triplet magnets

Edorta Ibarra, Antoni Arias, Iñigo Martínez de Alegría, Alberto Otero, Louis de Mallac

***Abstract*—A major upgrade will be conducted in the Large Hardon Collider (LHC) at CERN. This high luminosity (HL) version of the LHC will increase the nominal luminosity by a factor of five. One of the key technologies of the HL-LHC are the new superconducting Inner Triplet (IT) magnets, responsible of producing high magnetic fields to focus particle beams. To power the IT magnets from the grid, a multi-stage power supply with an intermediate 24 V battery pack is being considered. In such topology, a low-voltage high-current DC/DC converter operating with a very high step down-ratio is required for the final conversion stage. In this work, an interleaved multiphase Series Capacitor Buck converter is proposed to feed the IT magnets from the battery pack. A novel voltage regulation approach that ensures the current balance between the paralleled Series Capacitor cells is also proposed, where one cell is responsible for the output voltage regulation, while the remaining cells are current regulated. A balanced current sharing between the Series Capacitor cells is achieved, when the current controlled cells are referenced by the actual current of the 1st one. The proposal is theoretically analysed and experimentally validated in a six cell 1000 A prototype unit.**

***Index Terms*—Control of multiphase DC/DC converters, Series Capacitor Buck converter, Large Hadron Collider**

I. Introduction

THE Large Hadron Collider (LHC) at CERN (Geneva, Switzerland) is the largest particle accelerator and one of the biggest research facilities in the world [1]. This 27 km long circular machine accelerates hadron (proton) beams to 99.99 % of the speed of light, generating new particles as a result of proton-proton collisions at high energies. To extend its discovery potential, a major upgrade named High Luminosity (HL)-LHC is being implemented at CERN. For mid 2027, it is planned to increase accelerator's nominal luminosity (rate of collisions) by a factor of five [2], [3]. This is a desirable feature, because proton colliders operate in a very challenging environment where interesting collision events have to be identified in the presence of a huge amount of uninteresting ones [1]. In this scenario, one of most important technological changes will be the introduction of more powerful large aperture Nb_3Sn superconducting quadrupole electromagnets in the final focusing triplet magnets. These Inner Triplet (IT) magnets will operate at a temperature of 1.9 K, generating a peak magnetic field of 11.4 T [4]. IT magnets are inductive loads with a total inductance of 255 mH.

A power supply rated to 18 kA DC and $\pm$10 V (Fig. 1) is being considered at CERN for IT powering [5]–[7]. In this work, authors propose, develop and validate a multiphase 1000 A prototype for the Buck stage of the power supply. This solution incorporates a novel digital control approach aimed to regulate the output voltage and ensure current balancing through all cells. Thanks to the provided decoupling, conventional SISO tools can be used to set the controller specifications.

In the power supply architecture depicted in Fig. 1, a low voltage battery pack (or, alternatively, a supercapacitor bank [8]) is first charged from the grid. Then, the load is powered from the battery using a high current low voltage two-quadrant multiphase DC/DC converter [6]. This approach provides the following benefits [5]:

(i) Without two-quadrant operation, the power-down time of the IT magnets is governed by the time constant of the free-wheeling path. Because extremely low resistance is required for the application, this time constant is in the order of hours. Recycling the current back to the battery pack enables a much faster discharge.

(ii) The bidirectional power flow also allows recovering the stored energy on the IT magnets (40 MJ), decreasing overall system losses.

(iii) The divided architecture enables independent optimization of the upstream and downstream converters in addition to provide robustness against grid perturbations.

(iv) Apart from power splitting, the multiphase DC/DC approach facilitates system maintenance. The 18 kA solution will be constituted by 18+2 rack units, each one rated at 1000 A. The two redundant units are included to re-establish operation in a fast and safe way under single

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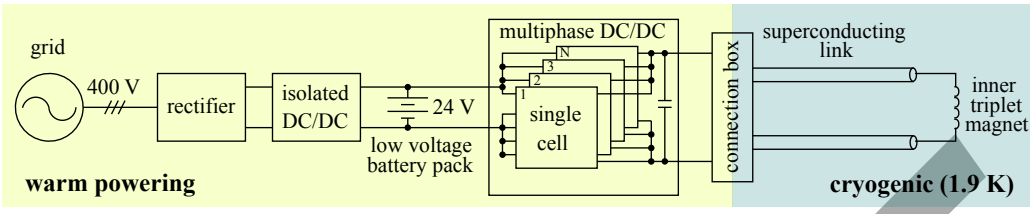


Fig. 1. General architecture of the stages of the investigated HL-LHC inner triplet magnet power supply.

unit faults (the exposure of technicians to radiation must be kept as low as possible).

Fig. 2 shows the electrical operation profile of the HL-LHC IT magnets during normal operation (the ±10 V range is considered for exceptional emergency situations where faster ramp-up or ramp-down operation is required), where a digital current controller tracks a parabolic linear parabolic (PLP) reference (Fig. 2(a)) by means of a decoupled RST regulator [9]. Such high precision controller determines the reference voltage v_{mag} to be followed by the multiphase DC/DC stage (Fig. 2(b)). This voltage depends on the resistance R_w between the power converter and the superconducting magnet, as:

$$v_{mag} = L_{mag}\frac{di_{mag}}{dt} + R_w i_{mag}, \tag{1}$$

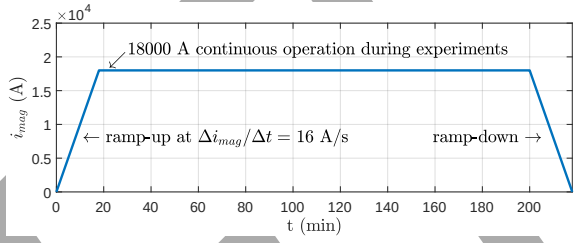
where L_{mag} and i_{mag} are the IT magnet inductance and current, respectively.

Recent advances in the superconducting link allow the installation of the connection box close to the power supply output. As a result, R_w becomes very small and it is expected that the converter maximum output voltage will get close to 4.08 V during ramp-up operation (Fig. 2(b)). Thus, the multiphase DC/DC converter will operate with a very high step-down conversion ratio during the plateau (Fig. 2(b)), where the multiphase DC/DC stage operates in Buck mode. This regime represents 10 hours or beyond of continuous operation.

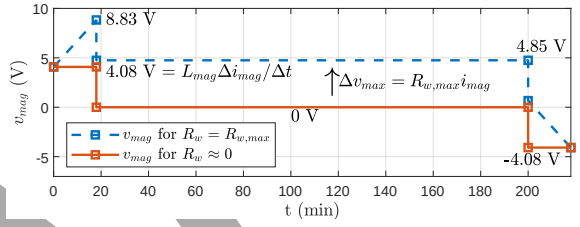
Interleaved DC/DC converters represent the most interesting alternative to achieve the required high output current with the lowest possible current ripple, thus reducing the output capacitor current rating, output voltage ripple and resistive losses. In this work, authors focus on the Buck operation (positive voltage application) of the power supply. In this sense, the double step-down two phase converter [10]–[12], also named interleaved Buck with voltage divider [13] (IBVD), or Series Capacitor Buck converter [14]–[20] has been considered as an alternative DC/DC topology to the conventional Buck converter due to the following reasons:

(i) For a given output voltage reference, duty cycle δ is doubled, as $v_{out} = \delta v_{dc}/2$. Thus, the performance of the converter under high step down operation (plateau) is improved, as the ratio of the combined and single cell output current ripples ($\overline{I}/I$) produced by the interleaving pattern is reduced (Fig. 3) [21]:

$$\frac{\overline{I}}{I} = \frac{mod(N\delta,1)\left[1 - mod(N\delta,1)\right]}{N\delta(1-\delta)}, \tag{2}$$



(a) Current profile of an LHC inner triplet magnet.



(b) Voltage profiles to be applied according to the initially estimated maximum and minimum wiring resistance values.

Fig. 2. Design profiles of LHC inner triplet magnets. Note that x-axis (time) has been scaled down to better represent the operation profile (16 A/s ramp rate, 10 hours or beyond of flat-top operation).

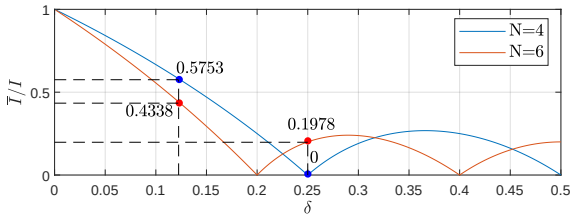


Fig. 3. Current ripple reduction vs duty-cycle for interleaved converters.

where N is the number of interleaved converters and mod is the modulo operator, i.e., $mod(x,m) = x - m\lfloor x/m \rfloor$.

A three level series capacitor Buck converter would further increase the duty cycle, as $v_{out} = \delta v_{dc}/3$, but a natural current sharing among inductors would not be achieved under the expected operation conditions.

(ii) Power semiconductors switch with half the input DC bus voltage applied at their terminals, thus reducing switching losses approximately by two. In addition, Si MOSFETs with blocking voltages of 40 V can be used instead of devices with blocking voltages of 75 V, whose ON resistances ($R_{DS,on}$) are of around 0.9 mΩ and 1.6 mΩ, respectively. This leads to an estimated reduction of

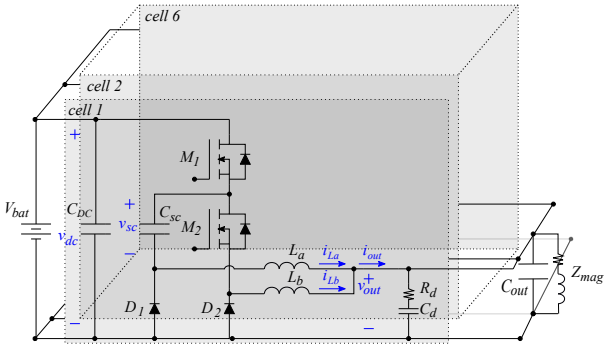


Fig. 4. Proposed six cell Series Capacitor Buck converter.

43.75 % in conduction losses.

(iii) Given that the converter will operate with $\delta < 0.5$, the output current of each cell is naturally shared between the two inductors ($i_{L_a} = i_{L_b}$), whereas for two interleaved Buck converters the current must be actively monitored. This divides by two the number of current sensors (and current regulation loops), reducing control complexity.

Considering all the previous, this paper proposes to use an interleaved multiphase Series Capacitor Buck converter for Buck operation of IT magnets powering. Fig. 4 shows the circuit diagram of the proposed 1000 A power supply prototype, which is constituted by six Series Capacitor Buck cells connected in parallel. Integrated circuit manufacturers are already providing products based on this topology, which means that its advantages have been proven in the field of point of load (POL) applications [14], [22]. However, to the best authors' knowledge, up to date no Series Capacitor Buck converters rated at such currents have been used for industrial applications. Additionally and considering the particularities of the application, a novel approach to regulate the power supply cells is proposed, where one cell is responsible for the output voltage regulation, while the remaining ones are current regulated. A balanced current sharing between the Series Capacitor cells is achieved, when the current controlled cells are referenced by the actual current of the first one. Experimental results that demonstrate the effectiveness of the proposal are finally presented.

II. Proposed Voltage Control Algorithm with Current Balancing Capabilities

A. Introduction

The multiphase nature of the power supply requires the incorporation of a current balancing control scheme. This topic has been studied in the scientific literature. For example, in [23] Abu-Qahoug proposes a solution where current balancing is perfectly achieved without deepening the decoupling issue. In [24], a decoupling continuous-time S domain average current balancing control is proposed. However, no compact and formal MIMO notation is addressed. In [25]–[27], comprehensive control approaches with decoupling in S-domain are proposed.

In contrast, the digital implementation (either in microcontrollers and/or FPGAs) of the control solution has been considered within this project. Therefore, the design of the controllers to fulfil the time specifications has been addressed using the zero-order-hold Z-transform [28]. This novel control solution has been developed bearing in mind the following:

(i) Its ease for digital implementation.

(ii) The internal converter dynamics (i.e., series capacitor voltage and inductors current ripples) can be neglected, as the dynamic requirements are sufficiently slow.

(iii) It incorporates an analytical decoupling which provides independent control of all cells.

(iv) As the controller has been designed using analytical methods, the determination of stability, dynamics and time response specifications becomes straightforward.

In the following, the theoretical fundamentals of the proposed control algorithm are described.

B. System Decoupling

Fig. 5 shows the equivalent circuit of the N-phase Series Capacitor Buck converter, where $L_j = L_a \parallel L_b$ and $C_j = C_{out}/N$ ($j = \{1, 2, 3 \cdots N\}$) are the per-cell equivalent inductances and capacitances, and $\overline{v}_j = \delta_j v_{dc}/2$ is the average output voltage synthesized by each Series Capacitor cell. Damping resistors $R_{d,j}$ have been physically placed in parallel with each cell to provide an adequate damping factor ζ around the resonance frequency of each LC circuit. Capacitors $C_{d,j}$ have been placed in series with damping resistors $R_{d,j}$ to minimize power losses at the DC component.

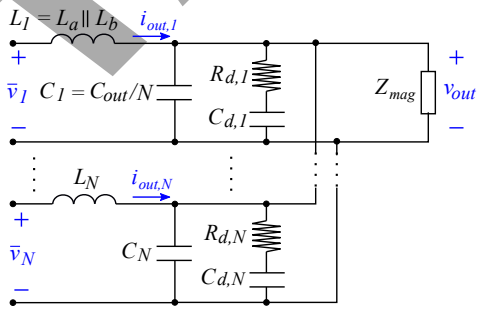


Fig. 5. Equivalent circuit of the Series Capacitor Buck converter with paralleled cells.

Assuming that the system is balanced, i.e., that $L_j = L$, $C_j = C$ and $NR_{d,j} = R$, the transfer function in the s-domain that relates the $\overline{v}_j$ cell voltages and v_{out} (Fig. 5) can be expressed as:

$$v_{out} = \frac{\alpha(s)}{sL + \alpha(s)} \sum_{j=1}^{N} \overline{v}_j, \tag{3}$$

where

$$\alpha(s) = \frac{sL}{N-1} \parallel \frac{1}{NsC} \parallel \frac{R}{N} = \frac{Ls/(N-1)}{\frac{NLC}{(N-1)}s^2 + \frac{NL}{(N-1)R}s + 1}.$$

In the proposed control approach, a given Series Capacitor cell (cell number 1 for simplicity) will be responsible for controlling the output voltage v_{out}. The remaining $N-1$ cells will control their corresponding output currents $i_{out,j}$. Thus,

the relationship between each $i_{out,j}$ and voltages $\overline{v}_j$ must be first determined, which leads to the following expression in the s-domain for the N-th cell:

$$i_{out,N} = \frac{1}{sL}\left[-\frac{\alpha(s)}{sL+\alpha(s)}\sum_{j=1}^{N-1}\overline{v}_j + \frac{sL}{sL+\alpha(s)}\overline{v}_N\right]. \quad (4)$$

The transfer function matrix $\mathbf{A}$ that relates the $\overline{v}_j$ voltages and the variables to be controlled is defined in (5).

$$\begin{bmatrix} v_{out} \\ i_{out,2} \\ i_{out,3} \\ \vdots \\ i_{out,N} \end{bmatrix} = \begin{bmatrix} F_1(s) & F_1(s) & F_1(s) & \cdots & F_1(s) \\ F_2(s) & F_3(s) & F_2(s) & \cdots & \vdots \\ F_2(s) & F_2(s) & F_3(s) & \cdots & \vdots \\ \vdots & \vdots & \vdots & \ddots & F_2(s) \\ F_2(s) & F_2(s) & \vdots & F_2(s) & F_3(s) \end{bmatrix} \begin{bmatrix} \overline{v}_1 \\ \overline{v}_2 \\ \overline{v}_3 \\ \vdots \\ \overline{v}_N \end{bmatrix}, \quad (5)$$

where

$$F_1(s) = \frac{\alpha(s)}{sL+\alpha(s)} = \frac{1/N}{LCs^2+(L/R)s+1}, \quad (6)$$

$$F_2(s) = \frac{-\alpha(s)}{sL\left[sL+\alpha(s)\right]} = \frac{-1/N}{L^2Cs^3+(L^2/R)s^2+Ls}, \quad (7)$$

$$F_3(s) = \frac{1}{sL+\alpha(s)} = \frac{LCs^2+(L/R)s+(N-1)/N}{L^2Cs^3+(L^2/R)s+Ls}. \quad (8)$$

The system represented by (5) is highly coupled. However, it can be decoupled by defining the adequate transformation matrices to obtain the eigenvalues of $\mathbf{A}$. As a first step of the diagonalization problem, the transformation matrix of (9) is defined to leave v_{out} only as a function of $\overline{v}_1$.

$$\mathbf{T}_1 = \begin{bmatrix} 1 & -1 & -1 & \cdots & -1 \\ 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & 0 \\ 0 & 0 & \vdots & 0 & 1 \end{bmatrix}, \quad (9)$$

whose application over $\mathbf{A}$ results in the following matrix:

$$\mathbf{A}' = \mathbf{A}\cdot\mathbf{T}_1 = \begin{bmatrix} F_1(s) & 0 & 0 & \cdots & 0 \\ F_2(s) & F_4(s) & 0 & \cdots & 0 \\ F_2(s) & 0 & F_4(s) & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & 0 \\ F_2(s) & 0 & \vdots & 0 & F_4(s) \end{bmatrix}, \quad (10)$$

where $F_4(s) = -F_2(s) + F_3(s)$.

Matrix $\mathbf{A}'$ can be completely diagonalized by applying the following transformation:

$$\mathbf{T}_2 = \begin{bmatrix} 1 & 0 & \cdots & 0 \\ \frac{F_2(s)}{F_2(s)-F_3(s)} & 1 & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ \frac{F_2(s)}{F_2(s)-F_3(s)} & 0 & 0 & 1 \end{bmatrix}, \quad (11)$$

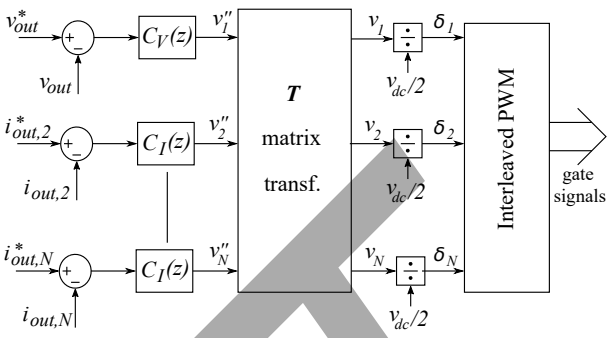


Fig. 6. Block diagram of the proposed IT magnet power supply controller.

whose application results in

$$\mathbf{A}'' = \mathbf{A}'\cdot\mathbf{T}_2 = \begin{bmatrix} \frac{1}{N(LCs^2+L/Rs+1)} & 0 & \cdots & 0 \\ 0 & \frac{1}{Ls} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & 0 & \frac{1}{Ls} \end{bmatrix}. \quad (12)$$

Thus, the transformation matrix $\mathbf{T}$ to be used for the proposed controller is:

$$\mathbf{T} = \mathbf{T}_1\cdot\mathbf{T}_2 = \begin{bmatrix} 1-\frac{(N-1)F_2(s)}{F_2(s)-F_3(s)} & -1 & \cdots & -1 \\ \frac{F_2(s)}{F_2(s)-F_3(s)} & 1 & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ \frac{F_2(s)}{F_2(s)-F_3(s)} & 0 & 0 & 1 \end{bmatrix}. \quad (13)$$

From (13) it can be observed that the basic decoupling transfer function is $T(s) = F_2(s)/\left[F_2(s)-F_3(s)\right]$. Its equivalent expression in the z-domain to achieve the compulsory digital implementation for a given sample-time T_s is:

$$T(z) = \frac{(1/N)(Az+B)z}{z^2-2ze^{-\mathrm{a}T_s}\cos(\mathrm{b}T_s)+e^{-2\mathrm{a}T_s}}, \quad (14)$$

where $\mathrm{a} = \zeta\omega_n$ and $\mathrm{b} = \omega_n\sqrt{1-\zeta^2}$ with $\omega_n = 1/\sqrt{LC}$ and $\zeta = \sqrt{L}/(2R\sqrt{C})$; $A = 1-e^{-\mathrm{a}T_s}\left[\cos(\mathrm{b}T_s)+\mathrm{a}/\mathrm{b}\sin(\mathrm{b}T_s)\right]$, and $B = e^{-2\mathrm{a}T_s}+e^{-\mathrm{a}T_s}\left[-\cos(-\mathrm{b}T_s)+\mathrm{a}/\mathrm{b}\sin(\mathrm{b}T_s)\right]$.

C. Proposed control scheme

From (12) it can be concluded that the initially coupled multiple input multiple output (MIMO) system has been successfully decoupled. Therefore, single input single output (SISO) tools can now be applied. In the proposed control strategy, whose scheme is illustrated in Fig. 6, cell number 1 is in charge of controlling the output voltage by following the reference v^*_{out} (Fig. 7). The remaining cells will add current to the output (Fig. 8). For the IT magnet regulation, a balanced current distribution along all cells is desirable to ensure a good thermal balance. If voltage drops within the power system are neglected, current references of the remaining $N-1$ cells can all be set to:

$$i^*_{out,j} = \frac{1}{N}\sum_{k=1}^{N} i_{out,k},\ j = \{2,3\cdots N\}, \quad (15)$$

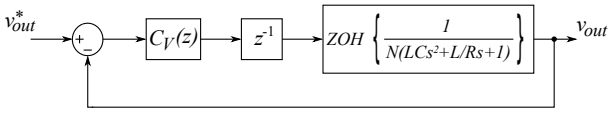


Fig. 7. Simplified diagram of the voltage control loop.

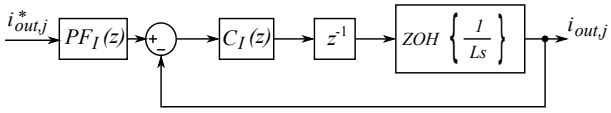


Fig. 8. Simplified diagram of the current control loops.

or, in a simpler way, current regulated cell references can be set to follow the current of the voltage regulated one, i.e., $i^*_{out,j} = i_{out,1}$, for $j = \{2, 3 \cdots N\}$. This way, current references are set with independence of the number of active cells.

Regarding the plant, just two types of transfer functions are obtained and therefore just two controllers must be designed (Figs. 7 and 8). Considering the data-sampled nature of the controllers, the well-known zero-order hold (ZOH) transformation method [29] has been used to obtain the plant transfer functions (16) and (17) in the z domain.

$$G_V(z) = (1-z^{-1})Z\left\{\frac{1}{s}\frac{1/N}{LCs^2+(L/R)s+1}\right\} = \\ = \frac{(1/N)(Az+B)}{z^2 - 2ze^{-aT_s}\cos(bT) + e^{-2aT_s}}, \quad (16)$$

$$G_I(z) = (1-z^{-1})Z\left\{\frac{1}{s}\frac{1}{Ls}\right\} = \frac{T_s}{L(z-1)}. \quad (17)$$

D. Voltage controller design in z domain

In order to guarantee the regulation capability of the voltage controller and minimize (or eventually cancel) any oscillation introduced by any poorly damped second order, the introduction of an integral term $1/(z-1)$ and the addition of two zeros $z^2 - 2ze^{-aT_s}\cos(bT_s) + e^{-2aT_s}$ in the complex conjugate plane is proposed. To ensure its real-time implementation, a proper controller transfer function with a relative degree equal or greater to zero is mandatory. Thus, the incorporation of an additional pole is required. Initially, the pole equal to $Az+B$ was envisaged to cancel the zero of the transfer function in (16). However, as such pole would be placed in the negative real axis of the z plane, its control action would contain an unacceptable transient response with an oscillation equal to one-half the sample frequency. Alternatively, an additional controller pole placed at the origin is proposed. Hence, the voltage controller transfer function is:

$$C_V(z) = K_V\frac{z^2 - 2ze^{-aT_s}\cos(bT_s) + e^{-2aT_s}}{(z-1)z}. \quad (18)$$

On the other hand, (19) is the open-loop voltage transfer function $L_V(z)$, which has 5 poles and 3 zeros from the controller $C_V(z)$, the plant $G_V(z)$ and one sample delay. Its pole-zero map and its root locus evolution are illustrated in Fig. 9(a). Assuming that the two complex poles (in red, labelled as p_0 and p_0^* in Fig. 9(a)) are cancelled by the zeros of

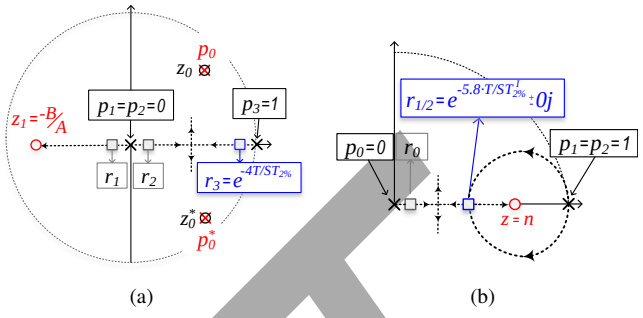


Fig. 9. $L_V(z)$ (a) and $L_I(z)$ (b) pole-zero maps and root locus in z domain of the voltage and current loops, respectively. The dominant (slowest) poles responsible for the closed-loop dynamics are r_3 (a) and $r_{1/2}$ (b).

the controller z_0 and z_0^*, the system is reduced to a third order one, with its three poles placed at $p_1 = p_2 = 0$ and $p_3 = 1$. Therefore, one of the three trajectories is defined from $p_1 = 0$ to $z_1 = -B/A$, while the other two trajectories advance to the two asymptotes at $\pm\pi/2$. Envisaged specifications are to fix the closed-loop response without any overshoot and with an adjustable settling time at 2 per cent $ST_{2\%}$. Therefore, the controller gain K_V must be calculated to place the closed-loop poles to the positions r_1, r_2 and r_3. Pole r_3 will be the slowest and therefore the dominant one, responsible for imposing the desired dynamics of $ST_{2\%}$. From a mathematical point of view, such conditions can be expressed as follows:

$$(z-r_1)(z-r_2)(z-r_3) = \\ = z^3 - z^2(r_1+r_2+r_3) + z(r_1r_2+r_1r_3+r_2r_3) - (r_1r_2r_3), \quad (20)$$

where $r_3 = e^{-4T_s/ST_{2\%}}$.

The characteristic equation with the closed-loop poles, assuming unitary feedback and perfect complex poles-zeros cancellation, is:

$$1 + L_V(z) = 1 + K_V\frac{(1/N)(Az+B)}{(z-1)(z)(z)} = 0, \quad (21)$$

and, rearranging (21), a third order polynomial is obtained:

$$z^3 - z^2 + K_V(1/N)(Az+B) = 0. \quad (22)$$

Imposing (22) to be equal to (20), the following set of equations is obtained:

$$-(r_1 + r_2 + e^{-4T_s/ST_{2\%}}) = -1, \quad (23)$$

$$r_1r_2 + r_1e^{-4T_s/ST_{2\%}} + r_2e^{-4T_s/ST_{2\%}} = K_VA/N, \quad (24)$$

$$-r_1r_2e^{-4T_s/ST_{2\%}} = K_VB/N. \quad (25)$$

From this equation system, the voltage controller gain is finally obtained:

$$K_V = N\frac{e^{-2(4T_s/ST_{2\%})} - e^{-3(4T_s/ST_{2\%})}}{Ae^{-4T_s/ST_{2\%}} + B}. \quad (26)$$

$$L_V(z) = C_V(z)\frac{1}{z}G_V(z) = K_V\frac{z^2 - 2ze^{-aT_s}\cos(bT_s) + e^{-2aT_s}}{(z-1)(z)}\frac{1}{z}\frac{(1/N)(Az+B)}{z^2 - 2ze^{-aT_s}\cos(bT_s) + e^{-2aT_s}}. \quad (19)$$

E. Current Controller design in z domain

The open-loop current transfer function $L_I(z)$ including the controller $C_I(z)$ and plant $G_I(z)$ transfer functions along with one sample delay is:

$$L_I(z) = C_I(z)\frac{1}{z}\frac{T_s}{L(z-1)}. \quad (27)$$

The targeted specifications for the current closed-loop response are to guarantee both the regulation capability and an adjustable settling time at two percent $ST^I_{2\%}$. Such specifications can be met with a first order controller with an integrator:

$$C_I(z) = K_I\frac{z-n}{(z-1)}, \quad (28)$$

Fig. 9(b) depicts the pole-zero map and root locus for $L_I(z)$. The dominant closed-loop poles of such root locus will lie anywhere within the trajectories beginning at poles $p1$ and $p2$. Among the infinite options available, the conservative one with a 0 % overshoot, i.e. $\zeta = 1$ and $\omega_n = 5.8/ST^I_{2\%}$, is chosen. Hence, the closed-loop poles $r_{1/2}$ will lie in the real axis ($r_1 = r_2 = e^{-5.8T_s/ST^I_{2\%}} \pm 0j$, Fig. 9(b)). Considering all the previous, the closed-loop poles can be mathematically expressed as:

$$(z-r_0)(z-r_1)^2 = \\ = z^3 - z^2(r_0+2r_1) + z(2r_0r_1 + {r_1}^2) - r_0{r_1}^2. \quad (29)$$

The characteristic equation with the closed-loop poles assuming unitary feedback is:

$$1 + L_I(z) = 1 + K_I\frac{z-n}{z-1}\frac{1}{z}\frac{T_s}{L(z-1)} = 0, \quad (30)$$

and, rearranging (30), a third order polynomial is obtained:

$$z^3 - 2z^2 + z(1 + \frac{K_IT_s}{L}) - \frac{K_IT_sn}{L} = 0. \quad (31)$$

Forcing the same coefficients for (29) and (31) brings the following set of equations:

$$-(r_0 + 2e^{-5.8T_s/ST^I_{2\%}}) = -2, \quad (32)$$

$$2r_0e^{-5.8T_s/ST^I_{2\%}} + e^{-2(5.8T_s/ST^I_{2\%})} = 1 + \frac{K_IT_s}{L}, \quad (33)$$

$$-r_0e^{-2(5.8T_s/ST^I_{2\%})} = -\frac{K_IT_sn}{L}. \quad (34)$$

From (32), r_0 is initially calculated. From (33), the current controller gain K_I is found, while n is obtained from (34). Finally, the unitary gain pre-filter of (35) is included to cancel any transient distortion created by the n zero.

$$PF_I(z) = \frac{1-n}{1-r_0}\frac{z-r_0}{z-n}. \quad (35)$$

Given the initial relative degree of the $PF_I(z)$ equal to 1, the closed-loop pole r_0 is also cancelled.

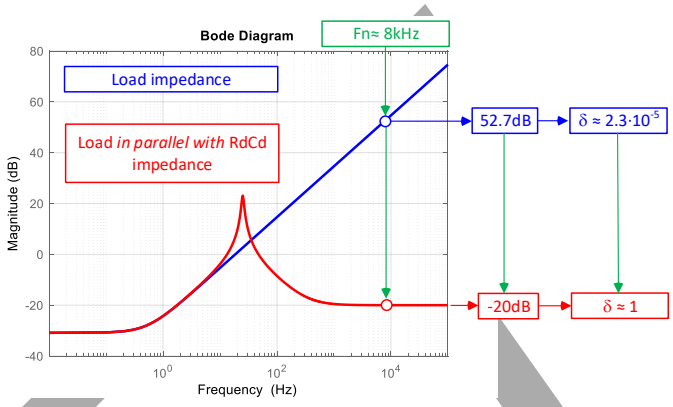


Fig. 10. Modulus impedances, with and without Z_d, considering table I values.

F. Tuning of the damping net

From the equivalent circuit of Fig. 5 and considering just the first cell, the transfer function of (36) is obtained.

$$\frac{v_{out}(s)}{v_1(s)} = \frac{1}{L_1C_1s^2 + (L_1/Z_{eq})s + 1}, \quad (36)$$

from where the characteristic pulsation $\omega_n = 1/\sqrt{L_1C_1}$ and the damping factor $\delta = 1/(2Z_{eq})\sqrt{L_1/C_1}$ are deduced.

The equivalent impedance Z_{eq} connected in parallel with C_1 is the load impedance (Z_{load}= Z_{mag} for the final application, see (1) and Fig. 2), which has a high pass filter characteristic with a rather low cut off frequency. For example, if the inductance (L_{load}) and resistance (R_{load}) values of the load used to carry out the high current experimental tests of section III-C are considered (table I), the modulus of Z_{eq} at ω_n is equal to 52.7 dB (Fig. 10). With such an extremely high value, δ is as low as $2.3.10^{-4}$. This will produce an unacceptable resonance and transient response. Actually, the PWM frequency could be eventually amplified by the resonance.

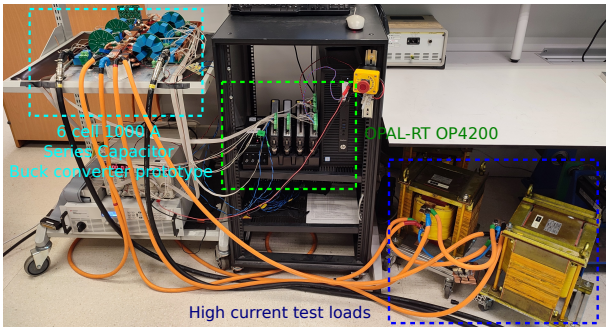
A damping net Z_d composed by R_d and C_d is connected in series with Z_{load} to obtain a proper damping factor. Hence, the total impedance tends to R_d at high frequencies, as it can be deduced from (37) and is illustrated in Fig. 10.

$$\frac{Z_{load}Z_d}{Z_{load}+Z_d} = \frac{R_{load}(R_dC_ds+1)(L_{load}/R_{load}s+1)}{L_{load}C_ds^2 + (R_{load}C_d + R_dC_d)s + 1}. \quad (37)$$

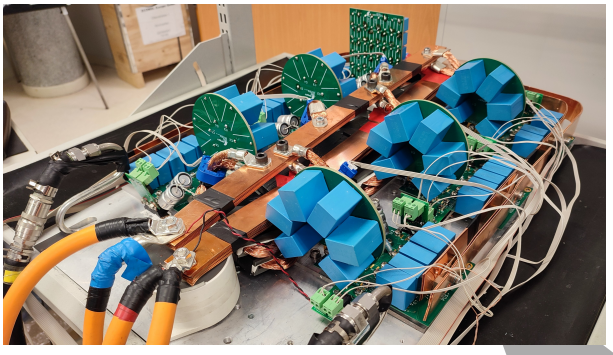
The damping resistor R_d, whose value is very low, is the Equivalent Series Resistance (ESR) of the capacitor C_d. Thus, in practice, no additional resistor has been incorporated in the damping impedances of the power supply prototype.

G. Interleaved PWM

Finally and once the duty cycles of all cells are determined, interleaved PWM firing pulses are generated. Within each cell, the PWM pulse applied to transistor M_2 is delayed 50 % of the modulation period T_s with respect to the one applied to



(a) Overview of the experimental platform.



(b) Detail of the six cell Series Capacitor Buck converter prototype.

Fig. 11. Test platform of the six cell 1000 A power supply Buck stage prototype.

M_1. Additionally, the interleaving delay between cell 1 and a given cell j is calculated as:

$$t_{d,j} = \frac{(j-1)}{2N} T_s, \; j = \{2, 3 \cdots N\}. \tag{38}$$

III. Experimental results

A. Experimental platform and prototype description

Fig. 11(a) shows the experimental platform implemented to validate the 1000 A Buck stage power supply prototype and the proposed control algorithm, whose most relevant parameters are shown in table I.

The converter prototype (Fig. 11(b)) has been built by using 6 Series Capacitor Buck cells, each cell incorporating two IXTN660N04T4 MOSFETs (V_{DS} = 40 V, $R_{DS,on}$ = 0.85 mΩ) and two DSS2x121-0045B diodes (a miniblock module per semiconductor device). For the final iteration of the prototype, diodes will be substituted by synchronous MOSFETs, and paralleled SMD devices will be used, which will considerably reduce power losses.

Considering the high current ratings of the application, the design of the series capacitor (C_{sc}) becomes extremely important. Such element has been manufactured by using 6 paralleled B32524Q1686K000 68 μF film capacitors in a daisy connection to reduce the parasitic inductance and distribute the currents evenly. All the series capacitors have been mounted vertically saving a significant amount of horizontal space. In this version of the prototype, a single can-type Kemet C4DEIPQ6100A8TK MKP capacitor of 100 μF has been placed at the output side of the converter to constitute C_{out}.

TABLE I
Most relevant parameters of the multiphase Series Capacitor Buck power supply, controller and test loads.

Power system parameters			
Number of cells (N)	6	Switching freq. (f_{sw})	50 kHz
Controller freq. (f_c)	50 kHz	Battery volt. (V_{bat})	24 V
DC-link cap. (C_{dc})	100 μF	Series cap. (C_{sc})	400 μF
Output cap. (C_{out})	100 μF	Cell induc. (L_a, L_b)	4 μH
Damping caps. (C_d)	4.7 mH	Damping res. (R_d)	0.1 Ω
Low current test parameters			
Load induct. (L_{load})	8.6 mH	Volt. $ST_{2\%}$ (1)	1000 ms
Load res. (R_{load})	28.6 mΩ	Cur. $ST^I_{2\%}$ (1)	5 ms
High current test parameters			
Load induct. (L_{load})	50 μH	Volt. $ST_{2\%}$ (2)	200 ms
Load res. (R_{load})	1 mΩ	Cur. $ST^I_{2\%}$ (2)	5 ms

(1) K_V = 0.0065 for $ST_{2\%}$ = 1000 ms and N = 3.
(2) K_V = 0.0056 for $ST_{2\%}$ = 200 ms and N = 6.
(1, 2) K_I = 0.0044, n = 0.9887, r_0 = 0.0459 for $ST^I_{2\%}$ = 5 ms.

The two inductors L_a and L_b of each cell have been built by using two E64/10/50 3C95 cores connected in series and with a single turn. The air gap has been adjusted to achieve an inductance of 4 μH. A Hall effect LEM HO-250S current sensor has been placed at the output side of each cell to provide the required feedback for current balancing.

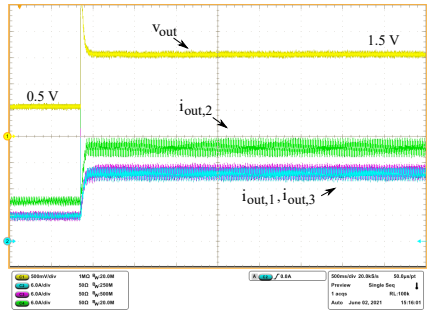
The six cells have been mounted over a liquid cooled cold plate with a size of 60 cm × 40 cm, with a coolant flow rate of 2.5 l/min. All inductors and connections have been manufactured by hand, which produces considerable inductance and resistance differences between paths. This way, current unbalances have been maximized to test the controller in a worst case scenario. An optimized interconnection layout will be manufactured for the final prototype.

An OPAL-RT OP4200 rapid control prototyping (RCP) platform incorporating a XilinX Zynq 7030 (Kintex 7 FPGA and dual core ARM9TM processor at 1 GHz) has been used to implement the proposed controller. The following IO boards have been used: a 16 channel OP4240-1 analog input cassette (16 bit ADCs, 2.5 μs maximum conversion speed) and a 32 channel OP4260-1 digital output cassette. The controller has been implemented in the FPGA with Matlab/Simulink by using the XilinX System Generator (XSG) and Real Time XSG toolboxes, following a model based design approach. The state logic and user interface communications have been implemented in a single core of the ARM9TM processor.

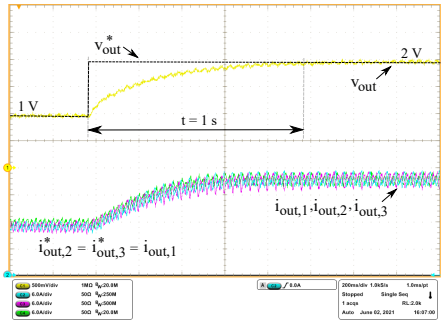
B. Low current test results

Initially, an inductor load of 8.6 mH and 28.6 mΩ has been placed at the output side of the power converter to carry out low current tests with three cells.

Fig. 12(a) shows the performance of the power supply when it is operated in open-loop and a voltage step from 0.5 V to 1.5 V is commanded. Under open-loop operation and due to impedance differences, currents circulating through the multiphase Series Capacitor cells are highly unbalanced, producing thermal unbalances that could jeopardize system reliability. In contrast, Fig. 12(b) shows the performance of the system when the proposed control algorithm is applied. The voltage and current regulators have been adjusted considering that the voltage regulation dynamic must be much slower than



(a) Operation in open-loop.



(b) Transient response obtained when using the proposed controller (step-up).

Fig. 12. Experimental results obtained for the Series Capacitor Buck with three cells in parallel: transient operation in open- and closed-loop.

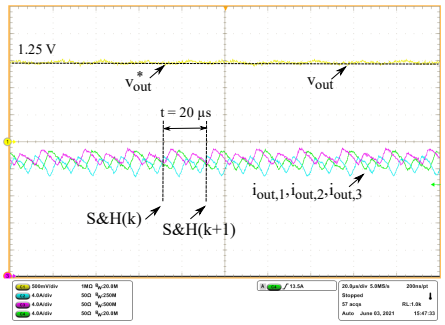


Fig. 13. Detail of current balancing for three Series Capacitor cells.

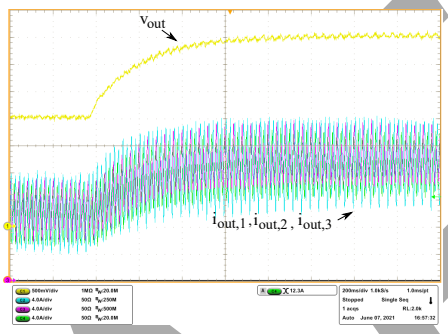
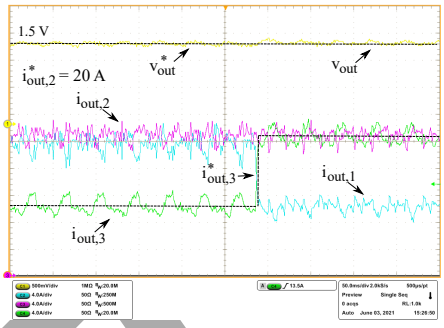
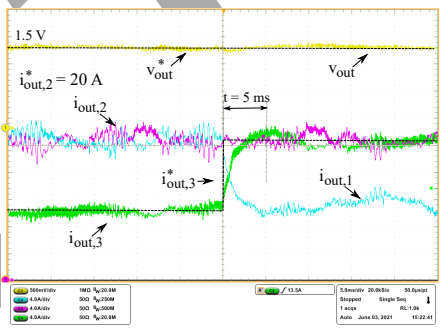


Fig. 14. Power converter response obtained in closed-loop and during a step-up when the converter does not incorporate damping resistors and capacitors.



(a) Current step on cell number 3.



(b) Current step on cell number 3 (detail).

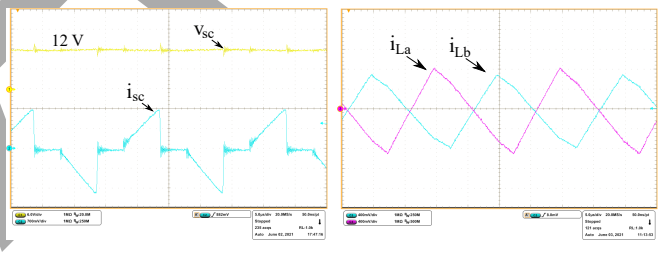
Fig. 15. Experimental results obtained for the IT magnet power supply prototype: independent cell output current control.

the ones for the current, i.e., $ST_{2\%}$ = 1 s, $ST^{I}_{2\%}$ = 5 ms and $\zeta = 1$. As demonstrated by the experiments, v_{out} tracks the voltage reference with the desired settling time and without any overshoot. Note that the current regulators' set-points have been set to $i^*_{out,j} = i_{out,1}$ and, consequently, the steady state per-cell currents increase from approximately 10 A to 20 A per cell when the output voltage step from 1 V to 2 V is applied. Hence, as desired, output cell currents have been kept balanced during both transient and steady-state operation (Fig. 12(b)). An analogous performance is achieved when applying a step down voltage reference, which confirms the correct performance of the proposed control approach.

Fig. 13 shows in detail how the current balance between cells is produced. As the discrete controller is executed with a sampling period of 20 μs, currents of the three cells are perfectly balanced at each sample & hold instant (S&H(k), Fig. 13). However, this difference is not relevant when the system operates at rated current (166 A per cell), as it is lower than 1 % of the rated current.

In order to illustrate the convenience of installing damping resistors (R_d) and damping capacitors (C_d) in the converter, such elements have been disassembled from the prototype and similar operation conditions of Fig. 12(b) have been carried out. As figure 14 illustrates, the performance of the system is worsened, as cell current ripple significantly increases.

In order to further validate the proposal, a different closed-loop test has been carried out, where the controller provides independent current set points to cells 2 and 3. In this test



(a) Voltage of the Series Capacitor with its charging and discharging current (AC component of i_{sc}).

(b) AC components of currents i_{La} and i_{Lb}.

Fig. 16. Experimental results obtained for the IT magnet power supply prototype: detailed single Series Capacitor cell operation under closed-loop control.

$i^*_{out,2}$ = 20 A, while a step has been commanded in $i^*_{out,3}$. Fig. 15 shows how $i_{out,2}$ and $i_{out,3}$ currents track their corresponding references, while the remaining current ($i_{out,1}$) circulates through cell one (which is voltage regulated). When a current reference step $i^*_{out,3}$ is commanded in cell number 3, $i_{out,3}$ follows the reference with the imposed dynamics. The independent control of each current is fully corroborated, and the fully decoupled performance of the output voltage and each module current is also clearly proven, since whenever one of the variables changes, all the others remain unaltered.

Fig. 16 exemplifies the performance of a single Series Capacitor cell during closed-loop operation of the power supply.

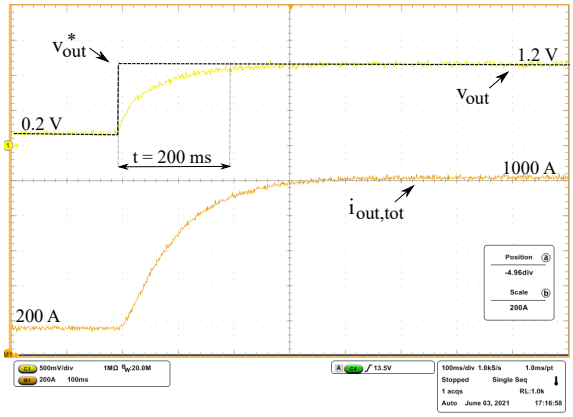


Fig. 17. High current test results at rated current (1000 A) for $ST_{2\%}$ = 200 ms and ζ = 1.

Fig. 16(a) shows how the voltage of the Series Capacitor remains $v_{sc} = v_{dc}/2$, while it is continuously charged and discharged (AC component of i_{sc}, Fig. 16(a)). Fig. 16(b) shows, in detail, the interleaved currents circulating through both inductors of a Series Capacitor single cell, showing the correctness of the modulation approach.

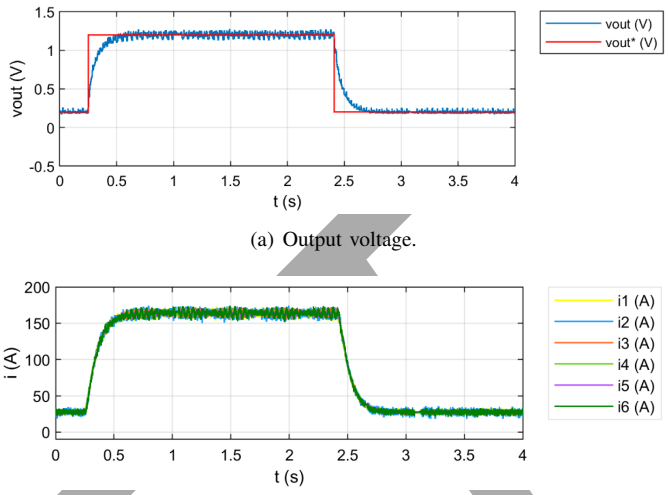
C. High current test results

Finally, the load has been substituted by an inductor of 50 μH and 1 mΩ and the performance of the six cell prototype has been tested in Buck mode at rated current. Fig. 17 shows the system performance when a voltage step from 0.2 V to 1.2 V is commanded. In this particular test, the controller has been set to $ST_{2\%}$ = 200 ms, $ST^I_{2\%}$ = 5 ms and $\zeta = 1$. The voltage step is performed with the desired dynamics and a total output current of 1000 A is obtained. Analogous results are obtained for step-down operation.

Fig. 18 shows the per cell currents and output voltage traces measured with the OPAL-RT OP4200 controller. As demonstrated in Fig. 18(b), six cell currents are balanced during the experiments at rated current, even during transients. In contrast, currents become unbalanced under open-loop operation due to impedance mismatches, which become relevant at high output current values (Fig. 19). Thus, all these high current operation results demonstrate the validity of the proposal.

IV. Conclusions

In this work, the utilization of multiphase DC/DC Series Capacitor Buck converters to supply the IT magnets of the future HL-LHC has been proposed. In this configuration, a highly coupled MIMO system is obtained. However, as it has been mathematically demonstrated, it is possible to find a transformation matrix to obtain the eigenvalues of such a complex system. This way, the system can be decoupled and controlled using SISO control tools. A novel control approach that takes advantage of such decoupling and independently regulates the power supply's output voltage and Series Capacitor cells' output currents has been proposed and



(a) Output voltage.

(b) Six cell currents.

Fig. 18. High current experimental test results registered by the controller in closed-loop ($ST_{2\%}$ = 200 ms and ζ = 1) for step-up and step-down operation.

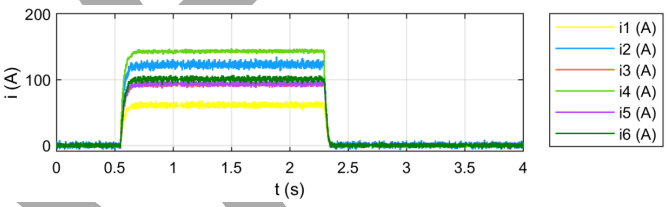


Fig. 19. High current experimental test results in open-loop registered by the controller.

experimentally validated. It is important to remark that the proposed control approach is not only valid for the multiphase Series Capacitor Buck configuration, as it could be applied to other multiphase DC/DC conversion topologies such as the ones incorporating conventional Buck converters. The proposal has been validated in a 1000 A unit incorporating 6 Series Capacitor Buck cells. As future work, the proposal will be extended for two-quadrant operation (control and hardware), high precision digitizers and PWM modules will be incorporated, and the solution will be evaluated in a full-scale platform with multiple units feeding the IT magnets.

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