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A Novel Detection and Localization Approach of Open-Circuit Switch Fault for the Grid-Connected Modular Multilevel Converter

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***Abstract*—The open-circuit fault detection and localization (FDL) technique can improve the reliability of the modular multilevel converter (MMC). However, the conventional software-based FDL methods usually have a heavy computation burden or a limited localization speed. This paper proposes a simplified and fast software-based FDL approach for the grid-connected MMC. Firstly, the errors between the measured state variables (the output current and the circulating current) and their estimated values are calculated. By comparing these errors with their threshold values, the switch fault can not only be detected, but also be localized to the specific arm. Then, the capacitor voltages in this faulty arm are collected, and the submodule (SM) with the highest capacitor voltage is selected. To confirm the switch fault in this SM, a modified *Pauta* criterion is presented to check the abnormal voltage data. As a result, the computation burden of the proposed software-based FDL approach is significantly reduced, and the faulty SM can be localized in a short period. Simulation and experimental results verify that the proposed approach can effectively detect and localize different open-circuit faults, and it is immune to the step of power references.**

***Index Terms*—modular multilevel converter, fault detection, fault localization, open-circuit fault, switch fault.**

I. Introduction

In the past decade, the modular multilevel converter (MMC) has emerged as one of the most promising topologies in the medium and high voltage applications [1], such as high-voltage dc (HVdc) systems, battery energy storage systems (BESSs), power electronic transformers (PET), motor drives, synchronic static compensators (STATCOMs), and so on [2]-[5]. The MMC has the advantages of modularity, scalability, low switching frequency, and good harmonic performance due to a large number of submodules (SMs) [6]. However, the existence of these SMs also increases the possibility of switch fault. It is estimated that over 38% of the faults in power conversion are attributed to semiconductor faults [7], [8]. Therefore, the fault detection and localization (FDL) technique has developed as an effective way to improve the reliability of power converters, especially for the MMC with a large number of power switches.

In general, there are two kinds of switch faults, the open-circuit fault and the short-circuit fault. The short-circuit fault is usually destructive and causes a high overcurrent within a short period. In practical engineering, the gate driver is usually integrated with short-circuit fault detection and protection circuits. Once detected with short-circuit fault, it will shut down the switching signals and bypass this SM immediately. On the contrary, the open-circuit fault is not very destructive and may even maintain undetected for some periods. The open-circuit fault is usually caused by unavailable drive signals, internal rupture of the wire connections, bond wire lift-off, and so on [9]. The SM with an open-circuit fault shows abnormal behavior only under certain switching statuses. If not detected in time, the open-circuit fault might cause secondary damage to the device and even lead to system failure. Therefore, it is necessary to detect and localize the open-circuit fault. The FDL methods can be categorized into hardware-based methods and software-based methods.

For the hardware-based method, a voltage and time criterion is used in [10] to process the error voltage signals from the fast A/D converter and FPGA. This method can diagnose the faulty arm, but it cannot localize the faulty SM. An improved FDL method is presented with additional SM output voltage measurement circuits and FPGA [11]. However, the extra cost and the design difficulty of the hardware circuits in each SM increase by a large extent. To simplify the hardware circuit, an FDL method based on arm inductor voltage is proposed in [12], where an additional rectifier bridge and FPGA are required. An FDL method by arm output voltage is proposed in [13], where the high-voltage hall-effect voltage sensors are necessary. Similarly, a fault localization method based on the arm output voltages is presented in [14], which can be applied to localize multiple SM faults in the same arm. However, in practical industrial applications, the arm voltage rating of the MMC can be very high, and the high-voltage hall-effect voltage sensor is quite expensive. Some other hardware-based methods are realized by changing the position of SM voltage sensors from the capacitor terminals to the SM output terminals [15], [16]. In [15], the measured SM output voltage and the arm currents are used to localize the faulty SM. In [16], the SM output voltage sensors and the capacitor voltage observer are combined to

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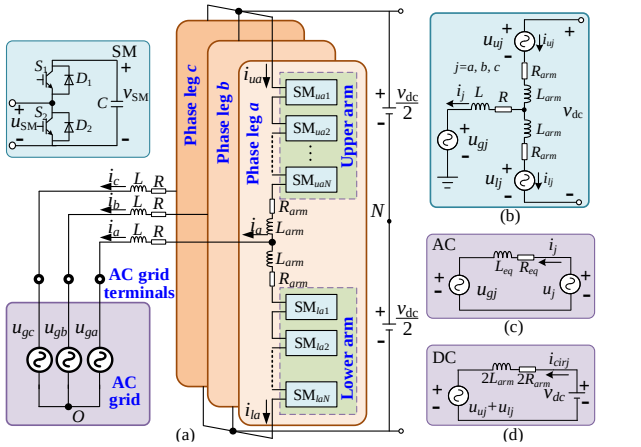

Fig. 1. Topology and equivalent circuit of the MMC. (a) Topology, (b) equivalent circuit, (c) ac control path, and (d) dc control path.

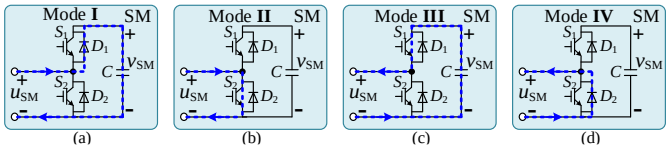

Fig. 2. SM Current path under normal operation conditions, (a) operation mode **I**, (b) operation mode **II**, (c) operation mode **III**, and (d) Operation mode **IV**.

realize the fast localization of the faulty SM. Overall, the hardware-based methods can provide faster detection of SM faults. However, they require a higher cost for additional power components or a reposition of the voltage sensor in each SM.

For the software-based method, a sliding-mode-observer-based FDL method is analyzed in [17]. Based on the observed and the measured values of the circulating current, the faulty phase can be detected if the error exceeds a certain threshold value. In [18], an observer-based injection item is introduced to estimate the system uncertainty and disturbance, which can improve the robustness and the accuracy of the sliding mode observer. A state observer is applied in [19], and a Kalman filter is applied in [20] to observe the circulating current. Similarly, the observed circulating current is compared with the measured value, and the error is used to identify the occurrence of SM fault. Then, the faulty SM can be localized by comparing the measured SM capacitor voltages with their reference values. In [21], a virtual capacitance estimation-based method is presented to detect and localize the faulty SM. In [22], the MMC predictive model is applied to detect the fault signal by predicting the circulating current. In [23], a capacitor voltage similarity-based method is proposed to localize the faulty SM. It calculates the correlation coefficients for every two SMs within the faulty arm and brings a heavy computation burden. In [24], a fault localization method is proposed, especially for the lower switch open-circuit fault. By analyzing the capacitor voltage increment in each switching period, the faulty SM can be localized. However, there is no fault detection operation, and more SMs need to be checked for fault localization.

In this paper, a simplified and fast software-based FDL approach of open-circuit switch fault is proposed for the grid-connected MMC. Compared with the conventional software-based FDL methods, the main contributions are as follows.

1) Two state variables (the output current and circulating current) are used to detect the open-circuit fault, so that reliable fault detection and faulty arm localization can be achieved simultaneously in the grid-connected MMC.

2) The measured state variables are compared with their estimated values instead of their references. Therefore, the fault detection is immune to the step of power references.

3) By faulty arm localization and modified *Pauta* criterion, the computation burden can be greatly reduced, and the faulty SM can be localized within a short period.

The rest of this paper is organized as follows. Section II introduces the operation principle and control model of the MMC. Section III analyzes the MMC behaviors under open-circuit fault. The proposed FDL approach is presented in Section IV. The parameter selection principle of the proposed FDL approach is analyzed in Section V. Simulation and experimental results are given in Section VI and Section VII, respectively, which verify the effectiveness of the proposed approach. The main conclusion is summarized in Section VIII.

II. Operation Principle and Control Model of the MMC

The basic operation principle and control model of the MMC are introduced in this section.

A. Operation Principle of the MMC

The circuit configuration of a three-phase MMC is shown in Fig. 1. The ac terminals of the MMC are connected to the ac grid through filter inductors (inductance L and equivalent resistance R), and the dc terminals of the MMC are connected to the dc source. In each phase, there are an upper arm and a lower arm. Each arm includes N half-bridge (HB) SMs. The HB SM contains a dc capacitor (C), two complementary switches, and two diodes (i.e., S_1, S_2, D_1, and D_2). The upper arm and the lower arm are connected through arm inductors (inductance L_{arm} and equivalent resistance R_{arm}), and the middle point is connected to the ac output terminal.

Normally, the output signal of each SM is controlled by its switching function S_{xjm}, which is defined as

$$S_{xjm}=\begin{cases}1, & S_1=1 \text{ and } S_2=0\\ 0, & S_1=0 \text{ and } S_2=1\end{cases} \tag{1}$$

where x indicates the arm position (x = u, l); j indicates the phase order (j = a, b, c); m indicates the SM number in each arm (m = 1, 2, …, N).

Supposing the SM capacitor voltage is v_{SM}, the SM output voltage can be expressed as

$$u_{SM}=S_{xjm}\cdot v_{SM} \tag{2}$$

During normal operation, there are four operation modes in each SM. The current paths of the four operation modes are shown in Fig. 2, and the detailed operation statuses are listed in Table I. For mode **I**, the arm current is positive (i_{xj}>0), the switching function is 1 (S_{xjm}=1), and this SM is inserted. In this mode, the capacitor is charged, and the output voltage is v_{SM}. For mode **II**, the arm current is positive (i_{xj}>0), the switching function is 0 (S_{xjm}=0), and this SM is bypassed. In this mode, the capacitor is bypassed, and the output voltage is 0. For mode **III**, the arm current is negative (i_{xj}<0), the switching function is 1 (S_{xjm}=1), and the SM is inserted. In this mode, the capacitor is discharged, and the output voltage is v_{SM}. For mode **IV**, the arm current is negative (i_{xj}<0), the switching function is 0 (S_{xjm}=0), and the SM is bypassed. In this mode, the capacitor is bypassed, and the output voltage is 0.

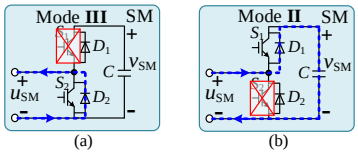

Fig. 3. Abnormal behaviors of the faulty SM under two types of open-circuit faults. (a) S_1 fault, and (b) S_2 fault.

TABLE I OPERATION MODES OF SMS

Mode	State	Capacitor status	Output voltage
I: $i_{xj} > 0$ && $S_{xjm} = 1$	Inserted	Charged	v_{SM}
II: $i_{xj} > 0$ && $S_{xjm} = 0$	Bypassed	Bypassed	0
III: $i_{xj} < 0$ && $S_{xjm} = 1$	Inserted	Discharged	v_{SM}
IV: $i_{xj} < 0$ && $S_{xjm} = 0$	Bypassed	Bypassed	0

TABLE II BEHAVIORS OF THE FAULTY SM UNDER DIFFERENT OPEN-CIRCUIT FAULTS

Fault types	Mode	State	Capacitor status	Output voltage
S_1 fault	**I**	Inserted	Charged	v_{SM}
	II	Bypassed	Bypassed	0
	III	Bypassed	Bypassed	0
	IV	Bypassed	Bypassed	0
S_2 fault	**I**	Inserted	Charged	v_{SM}
	II	Inserted	Charged	v_{SM}
	III	Inserted	Discharged	v_{SM}
	IV	Bypassed	Bypassed	0

B. Mathematical model and control equations

The MMC single-phase equivalent circuit is shown in Fig.1 (b), which can be further divided into two control paths, the ac control path in Fig. 1 (c) and the dc control path in Fig. 1 (d). Applying KVL to the equivalent control paths individually, the following equations can be derived

$$\begin{cases} R_{eq} i_j + L_{eq}(di_j/dt) = u_j - u_{gj} \\ 2R_{arm} i_{cirj} + 2L_{arm}(di_{cirj}/dt) = v_{dc} - 2u_{comj} \end{cases} \tag{3}$$

where i_j is the output current; u_j is the equivalent output voltage; u_{gj} is the grid voltage; v_{dc} is the dc-link voltage; i_{cirj} is the circulating current; L_{eq} and R_{eq} are the equivalent inductance and resistance in the ac path; i_j, u_j, i_{cirj}, and u_{comj} are defined as

$$i_j = i_{uj} - i_{lj}, \quad u_j = \frac{u_{lj} - u_{uj}}{2}, \quad i_{cirj} = \frac{i_{uj} + i_{lj}}{2}, \quad u_{comj} = \frac{u_{lj} + u_{uj}}{2} \tag{4}$$

where i_{uj} and i_{lj} are the arm currents in the upper and lower arms, respectively; u_{uj} and u_{lj} are the arm output voltages in the upper and lower arms, respectively. L_{eq} and R_{eq} can be defined as

$$L_{eq} = L + (L_{arm}/2), \quad R_{eq} = R + (R_{arm}/2) \tag{5}$$

The arm output voltage references can be expressed as

$$\begin{cases} u_{uj}^* = (v_{dc}/2) - u_j^* + u_{cirj}^* \\ u_{lj}^* = (v_{dc}/2) + u_j^* + u_{cirj}^* \end{cases} \tag{6}$$

where u_{uj}^* and u_{lj}^* are arm output voltage references; u_j^* is the ac output voltage references of the MMC; u_{cirj}^* is the voltage references for the circulating current control.

The conventional MMC linear control method in [25] is adopted to calculate the references u_j^* and u_{cirj}^*, which will not be further discussed in this paper.

III. MMC BEHAVIORS UNDER OPEN-CIRCUIT FAULT

In this section, the MMC output behaviors under different open-circuit faults are analyzed.

A. Behaviors of the Faulty SM

When an open-circuit fault occurs, the output voltage and current path of the faulty SM will be influenced under specific switching status. As shown in Fig. 3, there are two types of open-circuit faults, S_1 fault and S_2 fault. The abnormal SM behaviors under two types of faults are listed in table II. For S_1 fault, the current path is blocked under operation mode **III** (i_{xj}<0, S_{xjm}=1), and the current will go through the lower diode D_2. Consequently, the capacitor in this SM will be bypassed, and the output voltage will be 0 instead of v_{SM}. Under this condition, the capacitor is bypassed instead of being discharged. As a result, the capacitor voltage of the faulty SM tends to increase. For S_2 fault, the current path is blocked under operation mode **II** (i_{xj}>0, S_{xjm}=0), and the current will go through the upper diode D_1. Consequently, the capacitor in this SM will be charged, and the output voltage will be v_{SM} instead of 0. Under this condition, the capacitor is charged instead of being bypassed. As a result, the capacitor voltage of the faulty SM also tends to increase.

In conclusion, **under both types of open-circuit faults, the capacitor voltage of the faulty SM tends to increase**, which might lead to output distortions and malfunction of the MMC. However, the abnormal SM behaviors under different types of faults appear in different switching statuses. In addition, the SM output voltage under S_1 fault tends to decrease while the SM output voltage under S_2 fault tends to increase. The above differences can be used as the criterion to distinguish different open-circuit faults.

B. Output Characteristics of the Faulty Phase

According to the above discussion, when the open-circuit fault occurs, the output voltage of the faulty SM is different from the normal operation condition. Therefore, the measured values of output current and circulating current differ from their estimated values. This phenomenon can be used to detect the open-circuit fault and localize the faulty arm.

Based on the fault types in Table II and the positions of the faulty SM (fault in the upper or the lower arm), the fault conditions can be classified into four categories, the fault code of which is defined as 1 to 4. By substituting (4) into (3), the MMC control model can be derived, and the characteristics of the four fault codes can be analyzed.

$$\begin{cases} R_{eq} i_j + L_{eq}(di_j/dt) = (u_{lj} - u_{uj})/2 - u_{gj} \\ 2R_{arm} i_{cirj} + 2L_{arm}(di_{cirj}/dt) = v_{dc} - (u_{lj} + u_{uj}) \end{cases} \tag{7}$$

The output characteristics of the faulty phase are listed in Table III, and they are further explained as follows.

Fault code 1: For the first fault condition, S_1 fault occurs in the upper arm. According to the behavior descriptions in Table II, the faulty SM generates a lower output voltage under certain switching status. Hence, the output voltage of the upper arm u_{uj} will be lower than the reference value. Based on the control equation in (7), when u_{uj} decreases, the output current i_j and the circulating current i_{cirj} increase at the same time. Therefore, the measured output current and circulating current will be higher than their estimated values.

Fault code 2: For the second fault condition, S_2 fault occurs in the upper arm. According to the behavior descriptions in Table II, the faulty SM generates a higher output voltage under certain switching status. Hence, the output voltage of the upper

TABLE III FAULT CODE DEFINITION

Fault code	Faulty arm	Faulty switch	Arm voltage	Output current	Circulating current
1	Upper arm	S_1 fault	Lower	Higher	Higher
2	Upper arm	S_2 fault	Higher	Lower	Lower
3	Lower arm	S_1 fault	Lower	Lower	Higher
4	Lower arm	S_2 fault	Higher	Higher	Lower

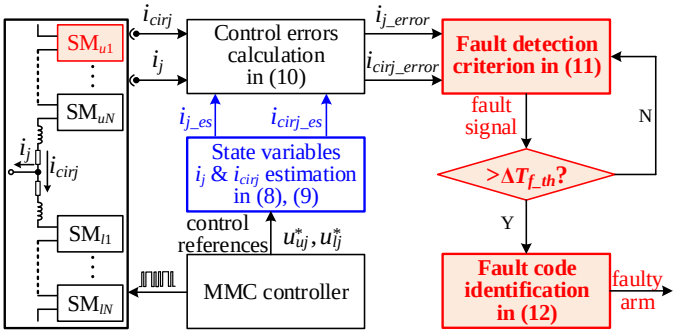

Fig. 4. Basic principle of the fault detection algorithm.

arm u_{uj} will be higher than the reference value. Based on the control equation in (7), when u_{uj} increases, both the output current i_j and the circulating current i_{cirj} decrease. Therefore, the measured output current and circulating current will be lower than the estimated value.

Fault code 3: For the third fault condition, S_1 fault occurs in the lower arm. According to the behavior descriptions in Table II, the faulty SM generates a lower output voltage under certain switching status. Hence, the output voltage of the lower arm u_{lj} will be lower than the reference value. Based on the control equation in (7), if u_{lj} decreases, the output current i_j decreases, and the circulating current i_{cirj} increases. Therefore, the measured output current will be lower than the estimated value, while the measured circulating current will be higher than the estimated value.

Fault code 4: For the fourth fault condition, S_2 fault occurs in the lower arm. According to the behavior descriptions in Table II, the faulty SM generates a higher output voltage under certain switching status. Hence, the output voltage of the lower arm u_{lj} will be higher than the reference value. Based on the control equation in (7), when u_{lj} increases, the output current i_j increases, and the circulating current i_{cirj} decreases. Therefore, the measured output current will be higher than the estimated value, while the measured circulating current will be lower than the estimated value.

IV. PROPOSED FDL APPROACH

The proposed FDL approach includes two steps. The first step realizes the fault detection and faulty arm localization, and the second step realizes the faulty SM localization.

A. Fault Detection Approach

According to the analysis in Section III, the fault detection method can be designed accordingly, as shown in Fig. 4. It is noted that the MMC controller includes two parts, the output current control and the arm energy and circulating current control. Namely, the output current control is used to control the active and reactive current of the converter. The arm energy and circulating current control is used to balance the internal capacitor voltages and suppress the harmonics of the circulating currents. More details can be found in [25].

For the proposed fault detection approach, firstly, the output current and circulating current are estimated based on the MMC control model.

Supposing the arm output voltage references calculated by the MMC controller are u^*_{uj} and u^*_{lj}, the estimated output current at the current time instant $i_{j\_es}(k)$ can be calculated based on the discrete model in (8).

$$\begin{cases} i_{j\_es}(k) = A[u^*_{lj}(k-1) - u^*_{uj}(k-1) - 2u_{gj}(k-1)] + Bi_j(k-1) \\ A = T_s/(2L+L_{arm}),\ B = 1-[(R_{arm}+2R_{ac})T_s/(2L+L_{arm})] \end{cases} \tag{8}$$

where T_s is the sampling period; k indicates the current time instant; k−1 indicates the last time instant; $i_j(k-1)$ and $u_{gj}(k-1)$ are the measured output current and the measured ac grid voltage at k−1 time instant, respectively.

The estimated circulating current at k time instant i_{cirj_es} can be expressed as

$$\begin{cases} i_{cirj\_es}(k) = C[v_{dc} - (u^*_{uj}(k-1) + u^*_{lj}(k-1))] + Di_{cirj}(k-1) \\ C = T_s/2L_{arm},\ \ D = 1-(R_{arm}T_s/L_{arm}) \end{cases} \tag{9}$$

where $i_{cirj}(k)$ is the measured circulating current.

The measured output current and the measured circulating current at the current time instant are $i_j(k)$ and $i_{cirj}(k)$. The errors between the measured values and the estimated values can be defined as

$$\begin{cases} i_{j\_error}(k) = i_j(k) - i_{j\_es}(k) \\ i_{cirj\_error}(k) = i_{cirj}(k) - i_{cirj\_es}(k) \end{cases} \tag{10}$$

where $i_{j\_error}(k)$ and $i_{cirj\_error}(k)$ are the output current error and the circulating current error at k time instant.

To detect the open-circuit fault, these errors are compared to their threshold values. If both errors and their threshold values meet the constraint in (11), the fault signal is triggered. If the fault signal lasts longer than the predefined time threshold ΔT_{f_th}, the open-circuit fault is confirmed in this phase.

$$\begin{aligned} &faultsignal = \\ &(|i_{j\_error}(k)| > \Delta I_{j\_th}) \,\&\, (|i_{cirj\_error}(k)| > \Delta I_{cirj\_th}) \end{aligned} \tag{11}$$

where ΔI_{j_th} is the threshold value of the output current error; ΔI_{cirj_th} is the threshold value of the circulating current error.

After detection of the open-circuit fault, the faulty arm can be localized, and the fault code can be identified

$$\text{fault code} = \begin{cases} 1; & i_{j\_error}(k) > 0, i_{cirj\_error}(k) > 0 \\ 2; & i_{j\_error}(k) < 0, i_{cirj\_error}(k) < 0 \\ 3; & i_{j\_error}(k) < 0, i_{cirj\_error}(k) > 0 \\ 4; & i_{j\_error}(k) > 0, i_{cirj\_error}(k) < 0 \end{cases} \tag{12}$$

As shown in (12), the fault code can be decided based on the fault criterion in Table III. If both errors are positive, the measured output current and circulating current are higher than their estimated values. Therefore, S_1 fault occurs in the upper arm, and the fault code is 1. If both errors are negative, the measured output current and circulating current are lower than their estimated values. Therefore, S_2 fault occurs in the upper arm, and the fault code is 2. If the output current error is negative and the circulating current error is positive, the measured output current is lower than the estimated value, and the measured circulating current is higher than the estimated value. Therefore, S_1 fault occurs in the lower arm, and the fault code is 3. If the output current error is positive and the circulating

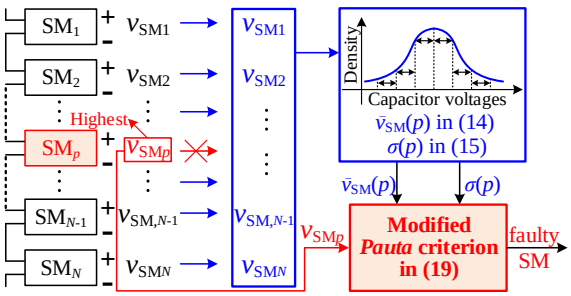

Fig. 5. Basic principle of the faulty SM localization algorithm.

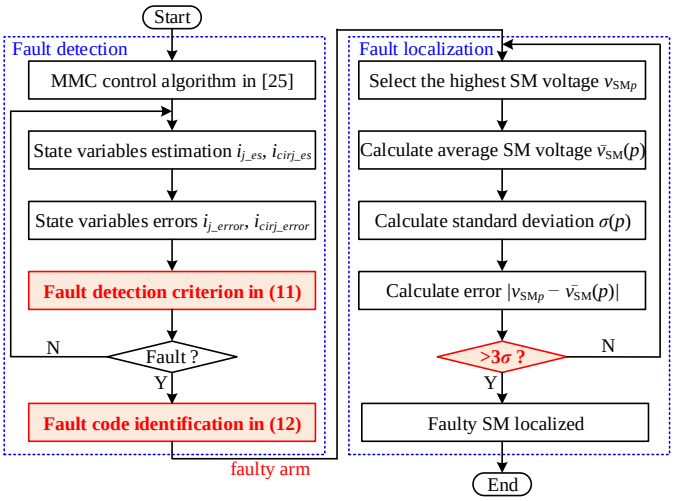

Fig. 6. Overall flow chart of the proposed FDL approach.

current error is negative, the measured output current is higher than the estimated value, and the measured circulating current is lower than the estimated value. Therefore, S_2 fault occurs in the lower arm, and the fault code is 4. Based on the above steps, the open-circuit fault can be detected, and the faulty arm can be localized with a specific fault code.

In addition, it is noted that the capacitor voltage in the faulty SM will increase, and the arm output voltage of the faulty arm could also be influenced under the switching status **I**. However, the influence is very limited due to the following reasons: (1) Before the faulty SM is localized, the capacitor voltage increment is limited. (2) Under switching status **I**, the capacitor voltage of the faulty SM is higher, and the faulty SM tends to be bypassed due to the capacitor voltage balancing algorithm. Therefore, the increased capacitor voltage has a very limited influence on the arm output voltage error.

B. Faulty SM Localization Approach

The faulty SM needs to be localized when the open-circuit fault is detected and the faulty arm is localized. To lower the computation burden of conventional fault localization methods, this paper proposes a simplified and fast localization approach.

For the MMC, the capacitor voltages are usually balanced by modulation reference adjustments. Therefore, a small deviation should exist (usually brought by the sensor measurement error or system control delay). Since the sensor measurement error conforms to the Gaussian (normal) distribution [26], the capacitor voltages in the MMC are also supposed to conform to the Gaussian distribution. The above hypothesis has been validated in [27], which means the *Pauta* criterion can be applied to detect the abnormal capacitor voltage data. The principle of the *Pauta* criterion is as follows:

Suppose $\boldsymbol{Y}$ is the set of all collected values

$$\boldsymbol{Y} = \{y_1, y_2, \ldots y_m\} \tag{13}$$

μ and σ represent the mean value and standard deviation of $\boldsymbol{Y}$, respectively, which can be expressed as

$$\mu = \sum_{i=1,}^{m} y_i \Big/ m \tag{14}$$

$$\sigma = \sqrt{\sum_{i=1,}^{m} (y_i - \mu)^2 \Big/ (m-1)} \tag{15}$$

The *Pauta* creation is the probability that the values are distributed in (μ-σ, μ+σ), (μ-2σ, μ+2σ), and (μ-3σ, μ+3σ) are 0.6826, 0.9544, and 0.9974, respectively. It can be seen that the probability of exceeding the range (μ-3σ, μ+3σ) is only about 0.27%. Therefore, it is considered that the values of $\boldsymbol{Y}$ are almost all concentrated in the interval (μ-3σ, μ+3σ).

Normally, the *Pauta* criterion is used in the statistics field to select abnormal data in Gaussian distribution. It indicates that if the error between a specific data and the average value is higher than 3σ (σ is the standard deviation), this data is supposed to be the abnormal data. However, considering the amount of capacitor voltage data is not always large in the MMC, this criterion is modified to reduce the influence of the abnormal value on the standard deviation.

As described above in Section III, if the open-circuit fault occurs, the capacitor voltage of the faulty SM always tends to increase. With this conclusion, if the closed-loop controller in MMC is working normally, the capacitor voltage of the faulty SM should be the highest within several operation periods. However, the SM with the highest capacitor voltages has to be checked if it is the faulty SM. This is because the highest capacitor voltage can also be created by the low speed and wide tolerance band of the individual capacitor voltage balancing controller. Based on this, the principle of the faulty SM localization process is shown in Fig. 5. Firstly, the SM with the highest capacitor voltage is selected as

$$v_{\mathrm{SM}p} = \max\{v_{\mathrm{SM1}}, v_{\mathrm{SM2}}, \ldots, v_{\mathrm{SM}N}\} \tag{16}$$

Then, the average capacitor voltage of the remaining SMs can be calculated as

$$\bar{v}_{\mathrm{SM}}(p) = \sum_{i=1, i\neq p}^{N} v_{\mathrm{SM}i} \Big/ (N-1) \tag{17}$$

Next, the standard deviation of the capacitor voltages in the remaining SMs can be expressed as

$$\sigma(p) = \sqrt{\sum_{i=1, i\neq p}^{N} (v_{\mathrm{SM}i} - \bar{v}_{\mathrm{SM}}(p))^2 \Big/ (N-2)} \tag{18}$$

Finally, the capacitor voltage divergence of the selected SM is confirmed. If the capacitor voltage meets the following constraint, this SM is confirmed as the faulty SM.

$$\left| v_{\mathrm{SM}p} - \bar{v}_{\mathrm{SM}}(p) \right| > 3\sigma(p) \tag{19}$$

The faulty SM can thus be localized.

C. Flowchart of the Proposed FDL Approach

The flow chart of the proposed approach is shown in Fig. 6. First, the state variables are estimated based on the MMC model and control references from the MMC controller. Based on the errors between the measured and estimated values of the state variables, the faulty arm can be localized in (11). Then, the SM with the highest capacitor voltage is selected in this faulty

TABLE IV COMPARISON OF DIFFERENT FDL METHODS

Items	Hardware-based methods						Software-based methods							
	[11]	[12]	[13]	[14]	[15]	[16]	[17]	[18]	[19]	[20]	[21]	[23]	[24]	Proposed
Detection	No	Yes	Yes	Yes	No	No	Yes	Yes	Yes	Yes	Yes	Yes	No	**Yes**
Localization	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	**Yes**
Detection time (about)	------	25 μs	------	200 μs	------	------	------	20 ms	10 ms	10 ms	20 ms	1.5 ms	------	**10ms**
Localization time (within about)	5 μs	85 ms	5 ms	200 μs	3.5 ms	300 μs	100 ms	50 ms	150 ms	1.2 s	20 ms	10.5 ms	150 ms	**10 ms**
Verified in grid-connected MMC	MMC dc/dc	Voltage source inverter			Yes	Yes	Voltage source inverter				Yes	Voltage source inverter		**Yes**
Additional cost	High	Low	Medium		Sensor reposition		No							**No**
Computation burden	No	Low	Medium				Low	High	Low		High	High	Medium	**Low**

TABLE V COMPUTATION BURDEN

Operations	Add	Multiply	Assign	Absolute	Compare
Runtime cycles	1	1	1	2	1

TABLE VI COMPUTATION BURDEN OF THE FDL METHODS IN ONE PHASE

FDL approach	Computation burden (runtime cycles)	Complexity
[18]	$2N(4N+7)$	$O(N^2)$
[19](slow localization)	$2N+38$	$O(N)$
[20](slow localization)	$6N+11$	$O(N)$
[21] Method 1	$(2F_0^2+8F_0)N+2F_0+1$	$O(F_0^2N)$
[21] Method 2	$12N+2$	$O(N)$
[23]	$(9F_0-4)N(N-1)/2+33$	$O(F_0N^2)$
[24](S_2 fault only)	$2(F_0N+4N+1)$	$O(F_0N)$
Proposed	$\mathbf{5N+24}$	$\boldsymbol{O(N)}$

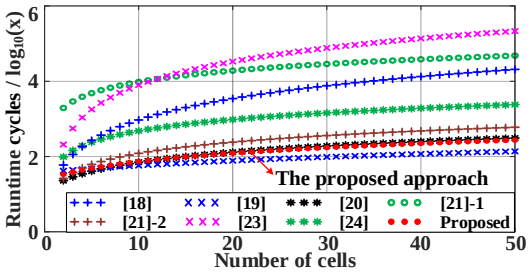

Fig.7. Computation burden of different FDL approaches.

arm. With these capacitor voltage data, the standard deviation of the remaining SMs can be calculated in (18). Finally, the error between the selected SM and the standard deviation can be calculated, and the switch fault can be confirmed by the modified *Pauta* criterion in (19).

It is noted the proposed FDL approach is designed especially for the single SM fault condition. The similar idea can also be applied to multiple SM fault conditions with some extra modifications. This will not be discussed in this paper.

D. Comparison with Existing FDL Methods

The proposed FDL approach is compared with the existing FDL methods, and the results are listed in Table IV. Generally, the hardware-based methods have a faster detection and localization speed. But they need more complicated hardware circuits and higher system costs, or require sensor repositions [15], [16]. Some of them still require some extra computation [13]-[16]. For the software-based methods, the detection speeds are more or less the same. However, the proposed approach has a much faster localization speed due to the modified *Puata* criterion. Most of these FDL methods are verified in MMC voltage source applications. The FDL method in [21] discusses its application for closed-loop control in the grid-connected MMC. However, the virtual SM capacitance estimation method is more complicated. In comparison, the proposed approach is designed especially for the grid-connected MMC application. It is noted that the main differences between the voltage source application and the grid-connected application are as follows:

1) The control targets and equations are different. For the voltage source application, the MMC is usually connected to the ac loads, and the control target is the output voltage and the circulating current. For the grid-connected application, the MMC is usually connected to the ac grid, and the control target is the output current and the circulating current.

2) The output current can be predicted in the grid-connected application. However, it cannot be predicted in the voltage source application due to the unpredicted ac loads.

The runtime cycles of the basic operations are listed in Table V [28], and the computation burden comparison of the software-based approaches is shown in Table VI. It is noted F_0 is defined as the sampling cycles in each fundamental period.

$$F_0 = f_s / f_g \tag{20}$$

where f_g is the grid frequency, f_s is the sampling frequency.

Supposing the sampling frequency is f_s=1 kHz, then F_0 is equal to 20, and the computation burden of the software-based approaches can be shown in Fig. 7. It is clear that the proposed approach has a relatively low computation burden compared with other FDL approaches. It can also be seen that the method in [19] has the least computation burden. However, it requires a higher time for faulty SM localization, as shown in Table IV.

V. DISCUSSION

In this section, the design principles of the threshold values are discussed for the proposed FDL approach. For the proposed FDL approach, the fault detection is realized by judging the errors between the estimated and measured values of the circulating current and output current. When the errors exceed the threshold values for a certain time period, the SM fault is ascertained. Therefore, it is necessary to carefully select and design the error and time threshold values.

A. Selection of the Threshold Values for ΔI_{j_th}

As described in the above section, the fault detection algorithm is established based on the measured and estimated values. Hence, the detection results are influenced by the sensor errors and the parameter accuracy of the predictive model. However, the sensor errors have a great influence on the control

accuracy but a very limited influence on the detection algorithm. Therefore, firstly, the threshold values are discussed based on the errors of the predictive model parameters.

As discussed in equation (8), the estimated value of the output current is mainly influenced by the parameter errors of the filter inductor and the arm inductor. Based on the simulation and experimental parameters, $(R_{arm}+2R)T_s/(2L+L_{arm})$ is much smaller than 1, and the coefficient $B\approx1$. As a result, the estimated value of the output current can be simplified as

$$i_{j\_es}(k)=\frac{T_s[u_{lj}^*(k-1)-u_{uj}^*(k-1)-2u_{gj}(k-1)]}{(2L+L_{arm})}+i_j(k-1) \quad (21)$$

It can be seen that the error of the estimated output current is mainly influenced by the filter and arm inductors. Usually, the uncertainties of the circuit parameters (especially the inductors) are within about 5% [29]. Define the estimated output current increment as

$$i_{j\_inc\_es}(k)=i_{j\_es}(k)-i_j(k-1) \quad (22)$$

Supposing the maximum parameter uncertainties are 5% or −5%, the estimated output current increment error will be about 1/0.95=1.0526 or 1/1.05=0.9524 times the actual value, and the percentages of the increment error are about 5.26% and 4.76%, respectively. The estimated output current can be expressed as

$$i_{j\_es}(k)=i_{j\_inc\_es}(k)+i_j(k-1) \quad (23)$$

During the steady-state operation condition, the error of the estimated output current will be lower than 5.26% and 4.76%. To avoid the disturbance of the parameter uncertainties, the threshold value should be selected to be higher than the error. Therefore, the first limitation should be that

$$\Delta I_{j\_th}>5.26\%I_{rated} \quad (24)$$

where I_{rated} is the rated amplitude of the output current.

In addition, the output current error is severely influenced by the abnormal output arm voltages, which is caused by the unexpected behavior of the faulty SM. The detailed analysis is as follows:

When the faulty SM appears, the influence of the abnormal SM output voltage on the output current can be derived based on (21)

$$\Delta I_{j\_error}=\frac{\lambda T_s v_{\mathrm{SM}}}{(2L+L_{arm})} \quad (25)$$

where λ is the duty cycle of the faulty SM. The second limitation of the threshold value can thus be expressed as

$$\Delta I_{j\_th}>\Delta I_{j\_error}=\frac{\lambda T_s v_{\mathrm{SM}}}{(2L+L_{arm})} \quad (26)$$

The threshold value of the output current error can thus be ascertained.

B. Selection of the Threshold Values for ΔI_{cirj_th}

As discussed in subsection *A*, the estimated value of the circulating current is mainly influenced by the parameter error of the arm inductor. Based on the simulation and experimental parameters, $R_{arm}T_s/L_{arm}$ is much smaller than 1, and the coefficient $D\approx1$. Therefore, the estimated value of the circulating current can be simplified as

$$i_{cirj\_es}(k)=\frac{T_s[v_{dc}-(u_{uj}^*(k-1)+u_{lj}^*(k-1))]}{2L_{arm}}+i_{cirj}(k-1) \quad (27)$$

Similarly, the error of estimated circulating current is influenced by the arm inductors, and the uncertainties of the circuit parameters are supposed to be within about 5% [29]. During the steady-state operation condition, the error of the estimated circulating current will be lower than 5.26% and 4.76%. To avoid the disturbance of the parameter uncertainties, the threshold value should be selected to be higher than the error. Therefore, the first limitation should be that

$$\Delta I_{cirj\_th}>5.26\%I_{cir\_rated} \quad (28)$$

where I_{cir_rated} is the rated amplitude of the circulating current.

In addition, the circulating current error is severely influenced by the abnormal arm output voltages, which is caused by the unexpected behavior of the faulty SM. The detailed analysis is as follows:

When the faulty SM appears, the influence of the abnormal SM output voltage on the circulating current is derived according to (27)

$$\Delta I_{cirj\_error}=\frac{\lambda T_s v_{\mathrm{SM}}}{2L_{arm}} \quad (29)$$

The second limitation of the threshold value can be expressed as

$$\Delta I_{cirj\_th}>\Delta I_{cirj\_error}=\frac{\lambda T_s v_{\mathrm{SM}}}{2L_{arm}} \quad (30)$$

The threshold value of the circulating current error can thus be ascertained.

C. Selection of the Threshold Values for ΔT_{f_th}

The threshold value for ΔT_{f_th} is also important for the proposed fault detection algorithm, which will help to eliminate the influence of system disturbance and increase the reliability of the fault detection results.

Firstly, as analyzed above, the abnormal output voltage of the faulty SM only appear in one certain switching status (switching status **III** under S_1 fault and switching status **II** under S_2 fault), which means the abnormal output voltage only appears in the following conditions: $i_{xj}<0$ under S_1 fault, and $i_{xj}>0$ under S_2 fault. If the output current of the MMC is sinusoidal, the time ratios under $i_{xj}<0$ and $i_{xj}>0$ will account for 50%. It further indicates that the fault code criterion in (12) is active only in half of the fundamental period. Therefore, the first limitation for the threshold value ΔT_{f_th} will be

$$\Delta T_{f\_th}<0.5T_g \quad (31)$$

where T_g is the fundamental period.

In addition, the system disturbance (sensor disturbance, etc.) usually appears in each sampling period. To avoid the influence

TABLE VII SYSTEM PARAMETERS

Items		Symbols	Simulation	Experiment
Rated dc voltage		v_{dc}	10 kV	120 V
Grid line-to-line voltage		U_{gl}	5.5 kV	62 V
Arm inductor	Inductance	L_{arm}	3 mH	5 mH
	Resistance	R_{arm}	0.0942 Ω	0.3 Ω
ac inductor	Inductance	L	2 mH	2.5 mH
	Resistance	R	0.0628 Ω	0.15 Ω
Carrier frequency		$f_{carrier}$	2 kHz	5 kHz
SM number per arm		N	10	4
SM capacitance		C	3 mF	3.84 mF
ΔI_{j_th}		ΔI_{j_th}	30 A	0.3 A
ΔI_{cirj_th}		ΔI_{cirj_th}	40 A	0.25 A
ΔT_{f_th}		ΔT_{f_th}	1 ms	1 ms

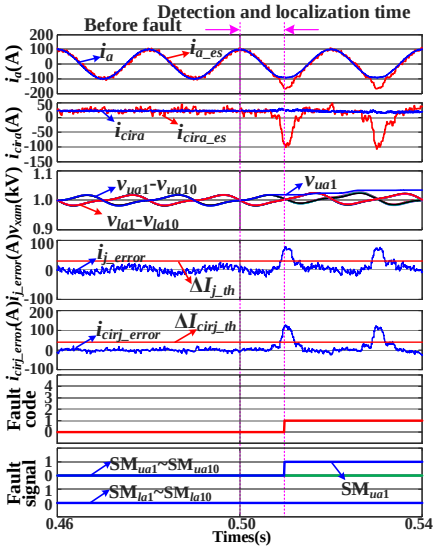

Fig. 8. Simulation results under S_1 fault in SM_{ua1}.

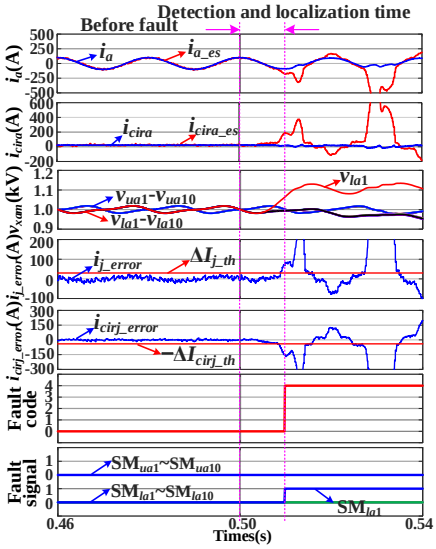

Fig. 9. Simulation results under S_2 fault in SM_{la1}.

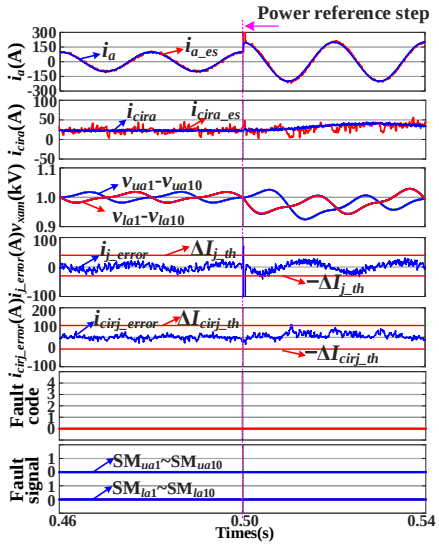

Fig. 10. Immunity test of power references step.

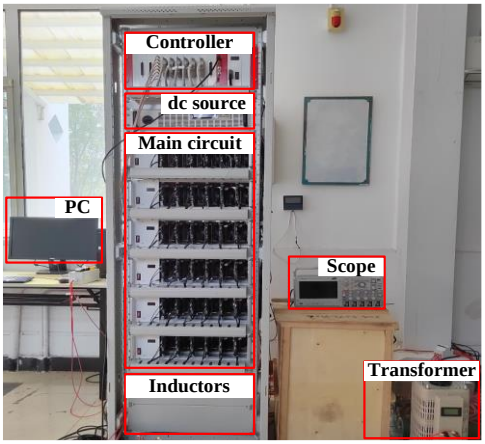

Fig. 11. Three-phase downscaled experimental setup of MMC.

of the system disturbance, the threshold value ΔT_{f_th} should be higher than the sampling period, which gives the second limitation

$$\Delta T_{f\_th} > T_s \tag{32}$$

Based on these two limitations, the time threshold of the fault signal can thus be selected.

VI. Simulation Results

To validate the performance of the proposed FDL approach, a simulation study is conducted in a three-phase grid-connected MMC. The simulation parameters are listed in Table VII, which are selected based on [25]. Due to the page limit, this section only provides the results under fault code 1, fault code 4, and the step of power references.

A. S_1 fault in the upper arm

The simulation results under S_1 fault in SM_1 in the upper arm in phase *a* are shown in Fig. 8. When the open-circuit fault occurs, the measured output current and circulating current are both higher than the estimated value for the first several periods. As a result, the fault code is identified as 1 after about 10 ms. In addition, the capacitor voltage of the faulty SM increases, and the faulty SM is localized as SM_1 in the upper arm. The results verify the effectiveness of the proposed FDL approach.

B. S_2 fault in the lower arm

Fig. 9 shows the simulation results under S_2 fault in SM_1 in the lower arm in phase *a*. When the open-circuit fault occurs, the measured output current is higher than the estimated value, and the measured circulating current is lower than the estimated value for the first several periods. Therefore, the fault code is identified as 4 after about 10 ms. Meanwhile, the capacitor voltage of the faulty SM increases, and the faulty SM is localized as SM_1 in the lower arm. The results verify the effectiveness of the proposed FDL approach.

C. Immunity against the step of power references

To verify the immunity of the proposed approach against the step of power references, the simulation results are given in Fig. 10. As shown in Fig. 10, when the power step occurs, the estimated output current experiences some disturbance for the first few sampling periods, and the estimated circulating current almost remain normal. Therefore, there is no detected fault signal under this condition. The robustness of the proposed FDL approach can thus be validated.

VII. Experimental Results

A three-phase downscaled MMC prototype in Fig. 11 to verify the effectiveness of the proposed FDL approach. The circuit parameters are also listed in Table VII. The MMC prototype works in the inverter mode, where the dc terminals are connected to a dc voltage source. The ac output terminals are connected to the ac grid emulated by an isolated transformer. The proposed algorithm is implemented on the digital signal processing controller, and the control signals from the controller are sent to each SM by optical fibers.

A. S_1 fault in the upper arm

The experimental results under S_1 fault in SM_3 in the upper arm in phase *a* are shown in Fig. 12. The output current, circulating current, and their estimated values are shown in Fig. 12 (a). At the first several periods after the open-circuit fault, both the output current and the circulating current are higher than

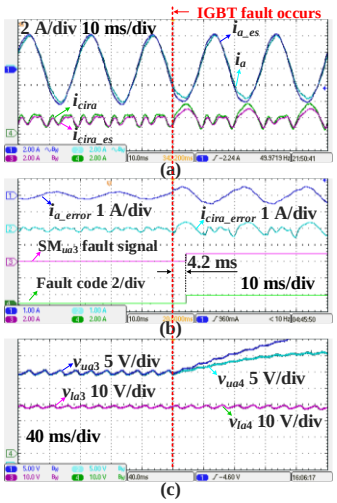

Fig. 12. Experimental results of the faulty phase under S_1 fault in SM_{ua3}. (a) Output current, circulating current, and their references, (b) output current error, circulating current error, fault signal, and fault code, and (c) capacitor voltages.

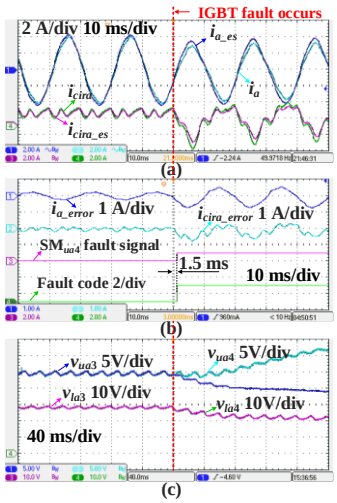

Fig. 13. Experimental results of the faulty phase under S_2 fault in SM_{ua4}. (a) Output current, circulating current, and their references, (b) output current error, circulating current error, fault signal, and fault code, and (c) capacitor voltages.

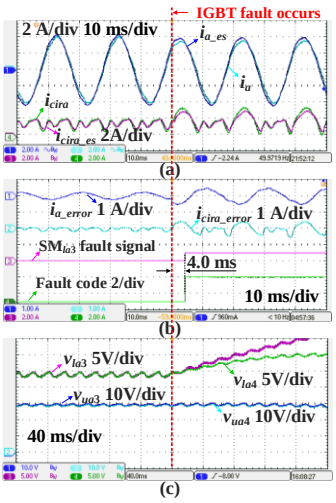

Fig. 14. Experimental results of the faulty phase under S_1 fault in SM_{la3}. (a) Output current, circulating current, and their references, (b) output current error, circulating current error, fault signal, and fault code, and (c) capacitor voltages.

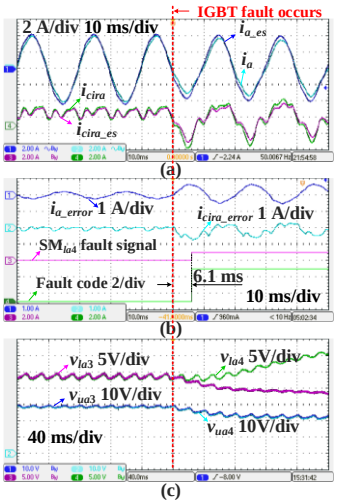

Fig. 15. Experimental results of the faulty phase under S_2 fault in SM_{la4}. (a) Output current, circulating current, and their references, (b) output current error, circulating current error, fault signal, and fault code, and (c) capacitor voltages.

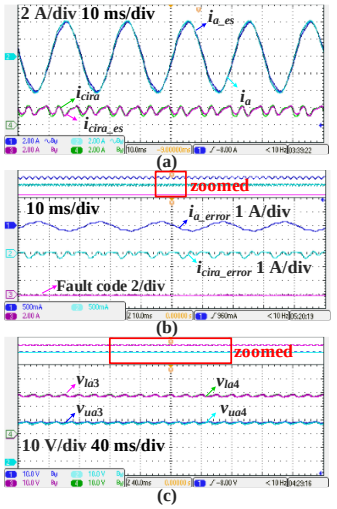

Fig. 16. Immunity test results of steady -state operation. (a) Output current, circulating current, and their reference values, (b) output current error, circulating current error, and fault code, and (c) capacitor voltages.

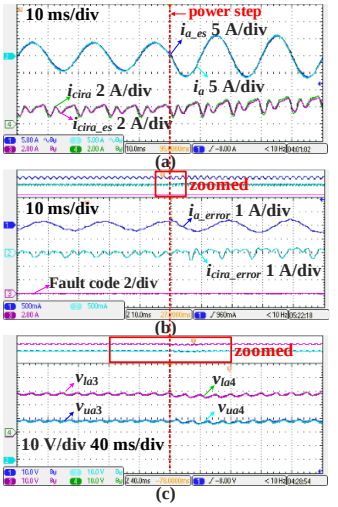

Fig. 17. Immunity test results of power step. (a) Output current, circulating current, and their reference values, (b) output current error, circulating current error, and fault code, and (c) capacitor voltages.

their estimated values. Based on (12), the fault code is identified as 1 at about 4.2 ms after the fault occurs, as shown in Fig. 12 (b). At the same time, the capacitor voltages are shown in Fig. 12 (c), where the capacitor voltage of the faulty SM tends to diverge, and the SM fault is localized immediately, as shown in Fig. 12 (b).

B. S_2 fault in the upper arm

The experimental results under S_2 fault in SM_{ua4} are shown in Fig. 13. The output current, circulating current, and their estimated values are shown in Fig. 13 (a). In the short period after the open-circuit fault, both the output current and circulating current are lower than their estimated values. Based on (12), the fault code is identified as 2 after about 1.5 ms, as shown in Fig. 13 (b). In addition, the capacitor voltages are shown in Fig. 13 (c), where the capacitor of the faulty SM tends to diverge, and the SM fault can be localized, as shown in Fig. 13 (b).

C. S_1 fault in the lower arm

The experimental results under S_1 fault in SM_{la3} are shown in Fig. 14. As shown in Fig. 14 (a), when the open-circuit fault occurs, the output current is lower, and the circulating current is higher than their estimated values. Based on (12), the fault code is identified as 3 after about 4.0 ms, as shown in Fig. 14 (b). At the same time, the capacitor voltages are shown in Fig. 14 (c), where the capacitor voltage of the faulty SM tends to diverge, and the SM fault is localized, as shown in Fig. 14 (b).

D. S_2 fault in the lower arm

The experimental results under S_2 fault in SM_{la4} are shown in Fig. 15. It can be seen in Fig. 15 (a), when the open-circuit fault occurs, the output current is higher, and the circulating current is lower than their estimated values. Based on (12), the fault code is identified as 4 after about 6.1 ms, as shown in Fig. 15 (b). At the same time, the capacitor voltages are shown in Fig. 15 (c), where the capacitor voltage of the faulty SM tends to diverge, and the SM fault is localized, as shown in Fig. 15 (b).

E. Immunity test of the proposed FDL approach

To verify the robustness of the proposed approach, the experimental results under steady-state and the power step operation conditions are shown in Fig. 16 and Fig. 17. As shown in Fig. 16 (a), the model-based estimated output current and circulating current can accurately track the realistic measured values under steady-state operations. As shown in Fig. 16 (b), no fault is detected during normal operations. In addition, the capacitor voltage waveforms are shown in Fig. 16 (c), where the average values stabilize at about 30 V. As shown in Fig. 17 (a), the model-based estimated output current and circulating current can accurately track the measured values during power

step operation. As shown in Fig. 17 (b), no fault is detected during the power step operation. In addition, the capacitor voltages are shown in Fig. 17 (c), where the average values are about 30 V. The above experimental results verify the immunity of the proposed approach under steady-state and power step operation conditions.

VIII. Conclusion

This paper has proposed a simplified and fast open-circuit FDL approach for the grid-connected MMC. This approach includes two steps. The first step realizes the fault detection and faulty arm localization, and the second step realizes the faulty SM localization. Based on the theoretical analysis and verification results, the following conclusion can be drawn.

1) By the faulty arm localization and voltage divergence confirmation of the SM with the highest capacitor voltage, the computation burden can be significantly reduced.

2) Under different open-circuit faults, the proposed approach can detect and localize the faulty SM within about 10 ms.

3) The proposed approach operates stably under steady-state operation conditions, and it is immune to disturbance from the step of power references.

Nevertheless, this paper only focuses on the single switch open-circuit fault conditions. The FDL approach for multiple switch faults will be discussed in future research work.

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