In Situ Diagnosis of Multichip IGBT Module Wire Bonding Faults Based on Collector Voltage Undershoot

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***Abstract*—Condition monitoring of IGBT modules is an effective way to improve the transient performance and reliability of modular multilevel converters (MMC). This paper proposes a novel bond wire failure monitoring method for the multichip IGBT modules in the MMC half-bridge submodule structure. The collector voltage undershoot $V_{CA(np)}$ of the complementary IGBT switch is measured during the turn-off switching transition of the controlled IGBT switch. $V_{CA(np)}$ is sensitive to the induced voltage over the stray inductance of the IGBT bond wires and provides high sensitivity as a health indicator. The non-intrusive measurement technique is demonstrated using a half-bridge circuit during the turn-off transition of the controlled IGBT, while its complementary switch (i.e., the device under test) is in the off state. Theoretical analysis and experimental results show that the parametric drift due to wire bonding failures can be effectively monitored with high specific relative sensitivity and granularity. To ensure its effectiveness in practical applications, the influence of load current, submodule capacitor voltage, and junction temperature is discussed. In addition, a readout circuit is designed featuring the integrated desaturation detection and voltage peak detection, which offers both the short-term overcurrent fault protection and long-term bond wire aging monitoring functions.**

***Index Terms*—condition monitoring (CM), bond wires diagnosis, insulated gate bipolar transistor (IGBT), modular multilevel converter (MMC), prognosis, reliability.**

NOMENCLATURE

$L_{CT/B}$	Stray inductance of the IGBT collector terminal
L_{EB}	Stray inductance of the IGBT emitter terminal
L_{eB}	Stray inductance of the IGBT-to-substrate bond wires from IGBT chip-top metallization
L_{DB}	Stray inductance of bond wires connecting the FWD chip-top and the IGBT chip-top.
L_{AEB}	Stray inductance of the IGBT auxiliary emitter bond wires
L_{GB}	Stray inductance of the IGBT gate bond wires
R_{GT}	Gate resistance of the top IGBT switch
R_{GB}	Gate resistance of the bottom IGBT switch
V_{GB}	Negative voltage of the bottom drive supply
R_F	The diode forward slope resistance
V_{F0}	Forward threshold voltage of the FWD
C_{oes}	Output capacitance of the IGBT device
v_{GET}	Gate-emitter terminal voltage of the top IGBT switch
i_T	Collector current of the top IGBT switch
I_L	Load inductor current
i_B	Collector current of the bottom IGBT switch
i_Q	Current flowing through the IGBT chip in the bottom IGBT switch
i_D	Current flowing through the FWD chip in the bottom IGBT switch
v_{CET}	Collector-emitter terminal voltage of the top IGBT
v_{CEB}	Collector-emitter terminal voltage of the bottom IGBT
v_{ce}	Collector-emitter voltage of the bottom IGBT chip
V_{th}	Gate threshold voltage
V_{GG+}	Positive voltage of the top drive supply
V_{GG-}	Negative voltage of the top drive supply
C_{GCB}	Miller capacitance of the bottom switch
C_{GEB}	Gate-emitter capacitance of the bottom switch
V_c	Capacitor voltage
T_j	Junction temperature of IGBT in the module

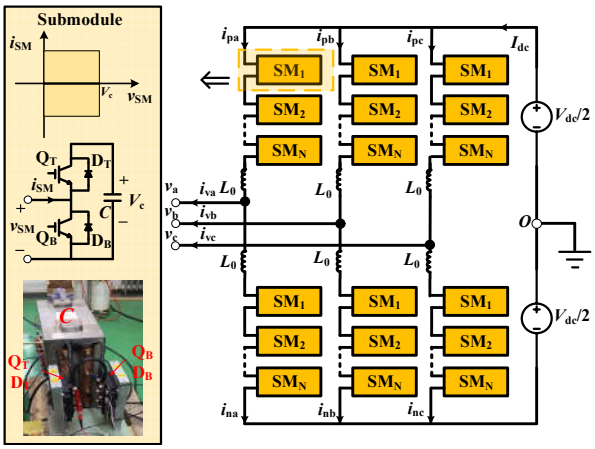


Fig.1 The circuit schematic of an MMC and an exemplar submodule (SM).

I. Introduction

Modular multilevel converter (MMC) has the advantages of strong expansion capability, low loss, and excellent harmonic performance, enabling its wide application in the flexible DC and AC transmission systems, railway traction systems, medium-voltage variable speed drives, power electronic transformers, and other fields [1-6]. The high-power MMC is composed of hundreds or thousands of submodules (SMs), and each SM includes IGBT modules, capacitors, control units, and the water-cooling device, as shown in Fig.1. The common SM structures include half-bridge structure, full-bridge structure, and clamp-double structure, among which the half-bridge SM is the most basic structure and has been the most popular SM adopted in the MMC [7],[8]. As the core component of the MMC, the failure of a single IGBT module may cause the SM to lose its function, and even cause the MMC to fail, ultimately causing additional power outages and economic losses. To overcome this challenge, implementing the condition monitoring techniques to the IGBT module is a vital and effective means to improve the performance and reliability of the MMC.

Bond wires fatigue is one of the main wear-out failure modes of IGBT modules [9-11]. For an individual IGBT chip inside the module packaging, several bond wires are connected to its emitter for electrical connection, whilst providing sufficient current carrying capability and redundancy in the power loop. Typically, the wire bonding fault can be divided into two scenarios: 1) Partial bond wires lift-off: fatigue or lift-off happening to partial bond wires of an IGBT chip, which manifests deteriorating electrical connectivity and increased loop inductance and resistance. However, the related IGBT chip still maintains its due function [12],[13] from the electrical perspective; 2) All bond wires lift-off: a chip open-emitter fault is caused by the loss of all the bond wires connected to the emitter metallization of an IGBT chip, which is treated as the virtual chip failure. This causes partial current capacity loss for a multichip IGBT (mIGBT) module, where the parallel configuration of multiple chips improves per-switch current capacity. Thus, the intended conduction function of multichip IGBT modules can still be sustained by the remaining intact chips. Without a doubt, the change-point detection for the loss of bond wire connection and chip connection are both of critical importance to the healthy operation and predictive maintenance in the MMC applications.

In recent years, numerous studies of the causal relationships between the health sensitive electrical parameters (HSEPs) and the device health status have been reported in the literature, which forms the backbone sensors to enable the in-situ condition monitoring of IGBT module bond wire failures and IGBT chip connection failures. Some typical research works, by no means exhaustive, are shown in TABLE I.

In terms of partial bond wire fracture monitoring, $V_{CE(on)}$ has been widely reported as an HSEP for IGBTs. The measurement takes place during the IGBT on-state, incurring lower switching noise interferences by the static nature of IGBT operation. However, its front-end readout circuit needs to be isolated from the high DC-bus voltage during the IGBT off-state, whilst ensuring millivolt-level resolution for the measurement of the saturation voltages of several volts [20-22]. Many efforts have also been made into the bond wire failure detection from the gate power loop. $V_{GE\_p(turn\text{-}on)}$ shows high sensitivity and a specific relative sensitivity (RS_p, defined for 50% loss of all bond wires from a single chip) of 8.2%. However, this method demands a fast frond-end measurement circuit to capture the dynamic gate voltage during the turn-on transitions, which is susceptible to noise interference, prone to false alarms, and costly. Other existing partial bond wire lift-off monitoring methods have low RS_p, which limits their field application especially when the operating point of the power converter is frequently changing. However, the partial bond wire lift-off monitoring can obtain earlier warning information for incipient virtual chip failures and catastrophic failures.

The entire chip connection loss, on the other hand, causes the emitter open-circuit fault, which changes the capacitance and impedance distribution within the mIGBT module. The failure is comparatively more significant, whilst the relative sensitivity of typical HSEPs to monitor a virtual chip loss failure can reach 30% and more [23]. The monitoring quantity is usually measured from the gate loop, and the monitoring device is easy to integrate into the drive unit without isolation of high voltage. For mIGBT modules, it is generally considered that 10% of chip failures are acceptable [13]. However, an IGBT chip connection failure has a great impact on the normal operation of the IGBT module, which is easy to cause the overall failure of the IGBT module.

In this article, a novel in-situ bond wire monitoring method is proposed based on collector voltage undershoot, $V_{CA(np)}$, during the turn-off switching transition of the complementary IGBT device in a typical hard-switching half-bridge configuration. This method is non-invasive and does not need to modify the existing drive and control methods. The experimental results show that the initial stage of bond wires fatigue can be effectively monitored. The method is proposed for the MMC half-bridge submodules and is also generally applicable to other power electronic converters containing half-bridge structures.

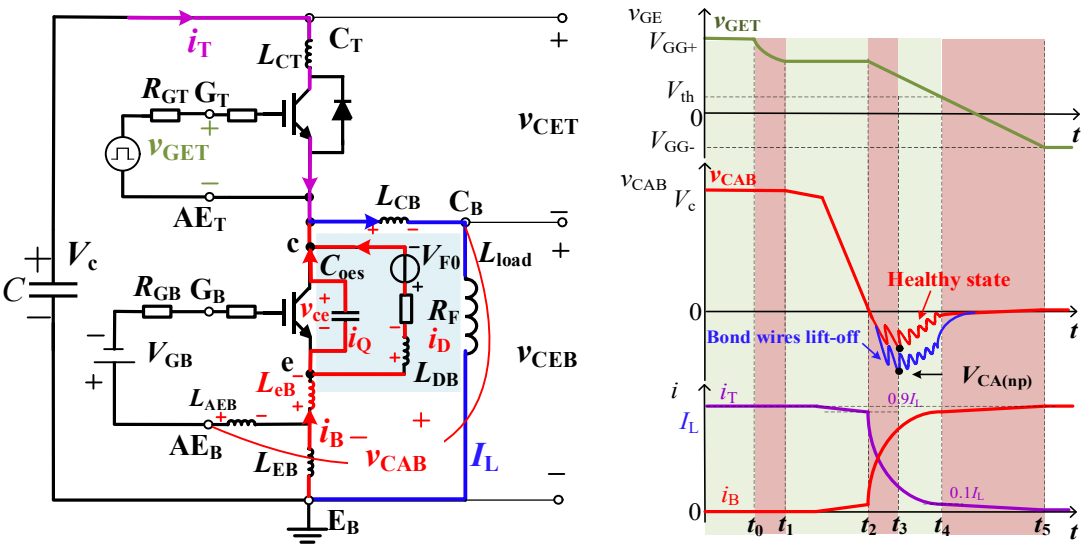
The rest of the article is organized as follows. In Section II, the internal structure and equivalent circuit of the IGBT module are given. Moreover, the collector voltage undershoot $V_{CA(np)}$ is

TABLE I

COMPARISON OF HSEPS FOR PARTIAL AND ALL BOND WIRES LIFT-OFF SCENARIOS

failure mode	health parameter	Number of parallel chips	Number of bond wires per chip	Number of bond wires lift-off	$RS_p = \frac{\lvert \text{failure value- healthy value} \rvert}{\lvert \text{healthy value} \rvert} \times 100\%$
Partial bond wires lift-off	$V_{CE(on)}$ [14]	1	6	3	7.0%
	$R_{CE(on)}$ [15]	2	4	2	3.5%
	I_{SC} [16]	2	8	4	2.2%
	$V_{GE\_p(turn\text{-}on)}$ [17]	3	6	3	8.2%
	$\Delta v_{CE(overshoot)}$ [18]	1	8	2	5.0%
	$V_{CA(np)}$ in this paper	3	13	6	20.2%
All bond wires lift-off	$I_{G(peak)}$ [19]	2	6	6(one chip)	36.0%
	t_{GC} [12]	2	8	8(one chip)	51.0%
	$V_{GE(pre\text{-}th)}$ [13]	16	8	16(two chips)	46.9%
	$V_{GE(t4)}$ [23]	3	6	6(one chip)	73.3%

Note: The RSp is specified when bond wire lift-off happens to half the number (medium value) of entire bond wires in a single chip scenario or an ultimate chip-connection loss happens to the first chip in an mIGBT module scenario, respectively.



(a) (b)

Fig.2 (a) The circuit diagram of the double pulse rig. (b) Waveforms of the v_{GET}, i_T, v_{CAB} during the Q_T turn-off process.

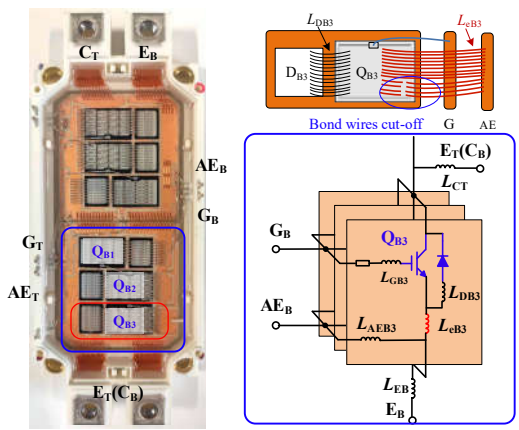


Fig.3 The internal structure of IGBT module and its equivalent circuit

analyzed in detail. In Section III, a commercial IGBT module is selected to carry out experiments with different load currents, capacitor voltages, and junction temperatures. The experimental results verify the effectiveness of the proposed method. A typical technical scheme for the integrated desaturation detection and bond wires lift-off monitoring has been discussed. In Section IV, the application of the method in the MMC submodules has been analyzed. Finally, Section V summarizes the conclusion obtained from theoretical analysis and experimental results.

II. MECHANISM OF THE MONITORING METHOD

A. Internal structure and connection of IGBT module

Figure 3 shows the internal structure, wire bonding sketch, and equivalent circuit of the bottom switch in a 600 A / 1700 V

IGBT module (FF600R17ME4) from Infineon. The module contains dual switches arranged in a half-bridge structure. Each switch is composed of three paralleled branches with each incorporating a single IGBT chip and a freewheeling diode (FWD) chip. The former subscript stands for the electrodes, gate (G), collector (C), or emitter (E), while the second subscript denotes a top (T) or bottom (B) switch.

Compared with FWDs, the IGBTs have a more complex structure, dominate the transient performance of the switching pair, and are prone to intensive electrothermal stresses during switching transients. For common resistive load and inductive load, the IGBTs are operating with a higher duty and thus longer on-time compared to the FWDs. Meanwhile, IGBTs have a higher on-state saturation voltage than the FWD forward voltage under the same load current. In addition, the emitter bond wires face comparatively more self-heating as they are used in the multiplexed nature, which is dictated to the interconnection shown in Fig.1. The IGBT-to-substrate bond wires are engaged with both IGBT and FWD current conduction, while the FWD-to-IGBT bond wires only accommodate FWD forward current. Overall, the increased self-heating losses arising from both IGBT and corresponding emitter bond wires are more critical and susceptible to the bond wire lift-off failures than the FWD anode bond wires. IGBT emitter bond wire plays a canary role in the power module under test and therefore is the focus of this paper.

A double pulse test (DPT) experimental circuit as shown in Fig.2(a) is established for this paper. The top IGBT (Q_T) is the control switch that alternates between its on-state and off-state following the pulse width modulation (PWM) signal provided by its gate driver through its gate resistor R_{GT}. The bottom IGBT (Q_B) is in the off-state by receiving a negative gate bias. Once its antiparallel diode D_B is forward biased by the load current given Q_T is in the off-state, D_B is modeled as a series network. Fig.2(b) illustrates voltage and current waveforms during the Q_T turn-off transition.

B. Collect Voltage Undershoot $V_{CA(np)}$

The voltage v_{CAB} appearing between the mid-terminal C_B and the auxiliary emitter AE_B of the bottom IGBT Q_B can be measured and leveraged as an HSEP. During the turn-off transition of Q_T, its gate voltage v_{GET} starts to decrease from t_0 until t_1. This is followed by the voltage commutation when v_{GET} is clamped to a constant the Miller voltage during the (t_1~t_2) interval. Meanwhile, the Q_T collector-emitter voltage v_{CET} increases gradually, with a simultaneous drop in v_{CAB} of Q_B. Since the diode D_B remains negative-biased and is in the blocking state, the Q_T collector current i_T remains unchanged (and equals the load current I_L) and the induced voltage on the stray inductance in the commutation loop is 0V. Therefore, v_{CAB} and v_{CET} satisfy the relationship:

$$\frac{\mathrm{d}v_{\mathrm{CAB}}}{\mathrm{d}t} = -\frac{\mathrm{d}v_{\mathrm{CET}}}{\mathrm{d}t} \tag{1}$$

Once the voltage commutation completes at t_2, v_{CEB} of Q_B drops to zero, and the diode D_B is at the transition into the conducting state. During the (t_2-t_3) interval, the load current I_L is commutating from Q_T to D_B when i_T and i_B satisfy the following relationship:

$$\frac{\mathrm{d}i_{\mathrm{B}}}{\mathrm{d}t} = -\frac{\mathrm{d}i_{\mathrm{T}}}{\mathrm{d}t} \tag{2}$$

The $\mathrm{d}i_T/\mathrm{d}t$ current slope produces an induced voltage across the parasitic inductance within the power loop, which is superimposed by the forward-recovery voltage of D_B. Therefore, a negative voltage peak $V_{CA(np)}$ appears. In addition, the Q_B output capacitance C_{oes} and the D_B stray inductance L_{DB} form the parallel resonant tank, leading to the oscillation of the voltage v_{ce} over time. The KVL equation of the loop shown in the blue box is:

$$R_{\mathrm{D}} i_{\mathrm{D}} + L_{\mathrm{DB}} \frac{\mathrm{d}i_D}{\mathrm{d}t} + V_{\mathrm{D}} + v_{\mathrm{ce}} = 0 \tag{3}$$

$$i_{\mathrm{D}} + i_{\mathrm{Q}} = i_{\mathrm{B}} \tag{4}$$

$$i_{\mathrm{Q}} = -C_{\mathrm{oes}} \frac{\mathrm{d}v_{\mathrm{ce}}}{\mathrm{d}t} \tag{5}$$

The t_2 is regarded as the zero time of the solution. At zero time, the capacitor voltage v_{ce} is zero. According to the switching rule:

$$\left.\frac{\mathrm{d}v_{\mathrm{ce}}}{\mathrm{d}t}\right|_{t=0} = 0 \tag{6}$$

Assuming that the edge rate of i_B is primarily constant during t_2-t_4, which is denoted as k, i_B can be approximated by i_B=kt. From (3)-(6), v_{ce} has arrived:

$$v_{\mathrm{ce}}(t) = v_{\mathrm{m}} e^{-\alpha t} \cos \omega t - R_{\mathrm{D}} k t - V_{\mathrm{D}} - L_{\mathrm{DB}} k + R_{\mathrm{D}}^2 C_{\mathrm{oes}} k \tag{7}$$

$$\alpha = \frac{R_{\mathrm{D}}}{2L_{\mathrm{DB}}} \tag{8}$$

$$\omega = \sqrt{\frac{1}{L_{\mathrm{DB}} C_{\mathrm{oes}}} - \left(\frac{R_{\mathrm{D}}}{2L_{\mathrm{DB}}}\right)^2} \tag{9}$$

$$v_{\mathrm{m}} = R_{\mathrm{D}} k t + L_{\mathrm{DB}} k - R_{\mathrm{D}}^2 C_{\mathrm{CE}} k + V_{\mathrm{D}} \tag{10}$$

The oscillation frequency, ω, of v_{ce} depends on the diode inductance L_{DB}. Given the diode bond wires normally are exposed to less intensive loading compared to the IGBT chip-top bond wires, the stray inductance L_{DB} is less susceptible to degradation-induced drifts compared to L_{eB} and can thus be assumed as a constant. It is noted that ω is dependent on C_{oes}, whose value remains unchanged when bond wire failures happen to a single IGBT chip, while ω increases with decreased C_{oes} given the entire chip loss occurs due to bond wire failures.

According to KVL, the terminal voltage v_{CAB} is

$$v_{\mathrm{CAB}}(t) = v_{\mathrm{ce}}(t) - L_{\mathrm{eB}} \frac{\mathrm{d}i_{\mathrm{B}}}{\mathrm{d}t} - L_{\mathrm{AEB}} \frac{\mathrm{d}i_{\mathrm{G}}}{\mathrm{d}t} - L_{\mathrm{CB}} \frac{\mathrm{d}I_{\mathrm{L}}}{\mathrm{d}t} \tag{11}$$

In (11), I_L is the load current, which is assumed to be a constant during the switching transitions and the induced voltage on L_{CB} can be ignored. i_G is the gate current, which is primarily generated by the displacement current through the Miller capacitance and is dependent on the voltage slew rate ($\mathrm{d}v_{CEB}/\mathrm{d}t$) across the off-state Q_B. Considering that $\mathrm{d}i_G/\mathrm{d}t$ is negligibly small and almost unchanged and irrespective of the

bond wire's health conditions, it can be regarded as a negligible factor for the failure indicator proposed. Hence to reveal the relationship between the bond wire failure and v_{CAB} more directly, the term of induced voltage over L_{AEB} can be ignored, and (11) is simplified to:

$$v_{CAB}(t) = v_{ce}(t) - L_{eB}\frac{di_B}{dt} \tag{12}$$

v_{CAB} is equivalent to the algebraic sum of the v_{ce} voltage and the kickback voltage induced by the emitter stray inductance, L_{eB}. of the attenuated oscillation superimposed on the induced voltage. It can be seen that the oscillation frequency and peak value are the key characteristics of v_{CAB}. However, before the bond wire failure of a single chip, the oscillation frequency remains unchanged, which cannot be used as an effective monitoring quantity for bond wire breakage.

For the oscillation peak value. When the change rate k of i_B reaches the maximum, the v_{ce} reaches the peak value, which is:

$$\begin{aligned} v_{ce(peak)} &= v_m e^{-\alpha t_{max}} \cos t_{max} - R_D k_{max} t_{max} - V_D \\ &\quad - L_{DB} k_{max} + R_D^2 C_{CE} k_{max} \end{aligned} \tag{13}$$

It is difficult to obtain an expression for the time t_{max} for the current rate of change to reach k_{max}, resulting in an inaccurate estimation of $v_{ce(peak)}$. Therefore, considering the maximum possible value of v_{ce}, that is, the first term including the cosine function is $-v_m$. At this time, $v_{ce(peak)}$ is:

$$v_{ce(peak)} \approx v_m - R_D k_{max} t_{max} - V_D - L_{DB} k_{max} + R_D^2 C_{CE} k_{max} \tag{14}$$

Taking (10) into (14), the simplified equation has arrived:

$$v_{ce(peak)} = -2L_{DB} k_{max} \tag{15}$$

At this time, the collector voltage v_{CAB} reaches negative peak amplitude (minimum), $V_{CA(np)}$. According to (12) and (15), $V_{CA(np)}$ is approximate:

$$V_{CA(np)} = -\left(2L_{DB} + L_{eB}\right) k_{max} \tag{16}$$

It can be seen that with either increasing L_{eB} as a result of bond wire lift-off or the increasing edge rate of the collector current, the fluctuating v_{CAB} changes accordingly, causing the negative peak $V_{CA(np)}$ to grow, while the oscillation frequency is maintained.

In the normal MMC operation, the edge rate of the collector current changes with the variation of operating points including the load current, submodule capacitor voltage, and junction temperature. To investigate the masking effect resulting from operating point changes when $V_{CA(np)}$ is leveraged as an HSEP, Section III will discuss this in detail.

C. Compared with other induced voltage methods

The methods reported in the existing literature that use the induced voltage changes of stray inductance to monitor the degree of bond wires fracture, the health parameters V_{hp} of which can usually be expressed as:

$$V_{hp} = V_{base} + \left(L_{DB} + L_{eB}\right)\frac{di}{dt} \tag{17}$$

The health parameters V_{hp} are composed of the base voltage and induced voltage of stray inductance. Among them, the induced voltage is the effective part to monitor the bond wires lift-off, and the base voltage V_{base} usually remains unchanged before and after the bond wires lift-off. However, in the existing literature, the base voltage V_{base} usually accounts for more than 50% of V_{hp}. For example, in [17], the base voltage V_{base} is the threshold voltage, and V_{bias} (5.8V) accounts for 54.2% of the V_{hp} peak value (10.7V). In [18], the base voltage V_{base} is the DC bus voltage, and V_{bias} (400V) accounts for 86.2% of the V_{hp} peak value (464V).

A higher bias voltage reduces the sensitivity of the monitoring method and increases the complexity of the monitoring system. In addition, the base voltage will usually be affected by factors other than bond wires lift-off, such as gate degradation will change the threshold voltage. The instability of the base voltage leads to a decrease in the specificity of the health parameters of bond wires lift-off and the possibility of false alarms. The method proposed in this paper directly reflects the induced voltage of the stray inductance of the bond wires, and the base voltage is approximately zero. $V_{CAB(n\text{-}pk)}$ has high relative sensitivity to bond wires lift-off monitoring and is not easily affected by other aging factors.

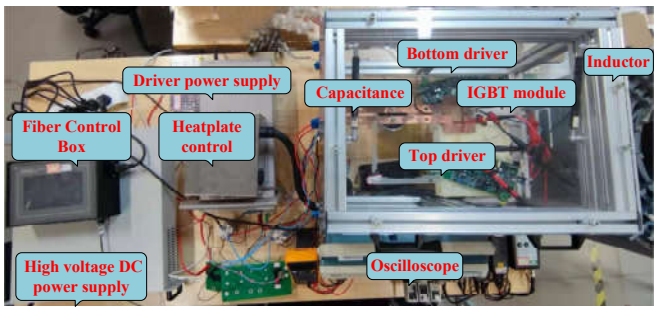


Fig.4 The experimental platform

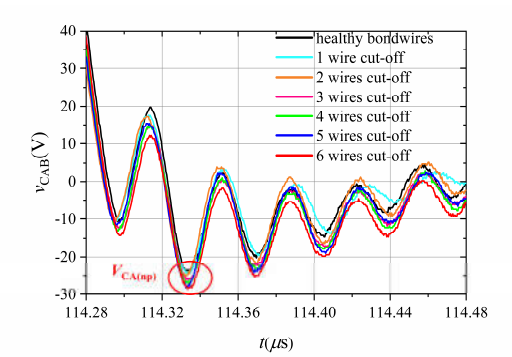
TABLE II
RELATED PARAMETERS OF EXPERIMENTAL PLATFORM

parameters	Value
C	1.2mF
L_{load}	0.3mH
R_{GT}	4.1Ω
R_{GB}	2.2Ω
V_{GB}	-10V/+15V

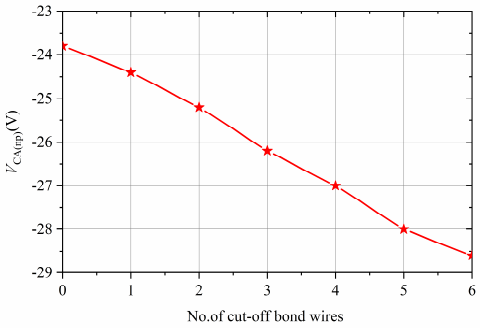
III. EXPERIMENTAL VALIDATION

The experimental platform has the same circuit connection as Fig.2(a), and its photo is shown in Fig. 4. The relevant parameters of the platform are concluded in TABLE II. The load inductance L_{load} is connected in parallel with the bottom IGBT Q_B. The top and bottom IGBT devices are controlled by separated driver boards, which are powered by an isolated power supply. The bond wire connection failure of an IGBT chip is emulated by cutting one wire off at a time. The experimental waveforms of the collector voltage v_{CAB} at 25℃ with different numbers of bond wire cut-off are compared in Fig. 5(a). The change of the undershoot peak value $V_{CA(np)}$ with

the number of bond wires cut-off is shown in Fig.5(b). The $V_{CAB\ (n\_pk)}$ of the healthy IGBT module is -23.8V. As the number of cut-off bond wires increases from one to six, $V_{CA(np)}$ gradually decreases from -24.4V to -28.6V. Compared with the healthy state, the relative sensitivity of $V_{CA(np)}$ after the bond wires cut off are 2.5%, 5.9%, 10.1%, 13.4%, 17.6%, and 20.2%.



(a)



(b)

Fig.5 (a) Parametric changes of the v_{CAB} fluctuations. (b) $V_{CA(np)}$ with the number of cut-off bond wires at 25℃.

The experimental results show that the collector voltage undershoot peak value $V_{CA(np)}$ of the IGBT module can effectively monitor the bond wires connection failure and has a high monitoring sensitivity. Note that the voltage drops on the resistance of a single bond wire (about 10mΩ), as well as the thermal drift of resistance, are negligibly small compared with the induced voltage across the parasitic inductance of bond wire. Therefore, the electrothermal coupling effect of bonding wire resistance is ignored, and only the effect of bonding wire inductance on $V_{CA(np)}$ is considered.

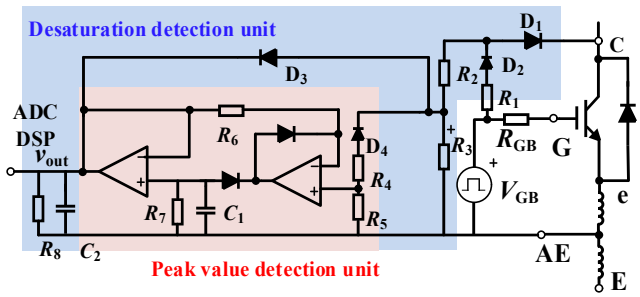


Fig.6 The readout circuit integrating the short-circuit protection and wire bonding health monitoring.

A. *In situ monitoring circuit discussion*

One benefit of the proposed monitoring method is its ease of implementation by taking the advantage of the commonly existing desaturation detection circuits available on the gate driver units of power modules for short-circuit detection [24],[25]. The proposed circuit monitoring the collector voltage's undershoot for the bond-wire faults can be added and mixed with the desaturation detection circuit without adding extra sensing points to the power stage, whilst benefiting simplicity and cost.

The proposed circuit schematic of the integrated short-circuit and bond-wire health detecting functions is shown in Fig.6, where the blue box is the desaturation detection unit, and the red box is the newly added peak voltage detection unit. The bandwidth of the monitoring signal is about 25MHz, and the operational amplifier bandwidth should be greater than 250MHz for better performance.

For the short-circuit detection, when the IGBT device is in conduction, the diodes D_1 and D_2 are turned on since the on-state voltage drop of the IGBT device is only a few volts and less than the driver supply voltage V_{GB} of 15V. Hence, the voltage across R_3 is a positive value (upper positive and lower negative), which equals the sum of the on-state voltage of the IGBT and the forward voltage of D_1 divided by the voltage divider of R_2 and R_3. So, the D_3 is turned on, while the diode D_4 is reverse biased. In this case, the output voltage v_{out} is approximate:

$$v_{out}=\frac{R_3}{R_2+R_3}\left(V_{CE(on)}-V_{D1}\right)-V_{D3} \tag{18}$$

If a short-circuit fault occurs and the collector overcurrent causes the IGBT device to desaturate, the collector voltage $V_{CE(on)}$ rises rapidly, and the measured v_{out} is compared with the threshold to determine whether an overcurrent has occurred.

For the bond-wires lift-off monitoring, the proposed method monitors when the IGBT device is in the negative voltage turn-off process. In the t_2-t_3 stages of the turn-off process, the collector voltage of the IGBT device decreases and turns into a negative voltage, and the diode D_1 is turned on. At this time, the voltage of the voltage divider R_3 is negative (upper negative and lower positive). The D_3 is turned off and the diodes D_4 is turned on. After the voltage of the resistor R_3 is further divided, the negative peak value is extracted by the peak detection and hold circuit. The output voltage v_{out} is:

$$v_{out}=\frac{R_3//\left(R_4+R_5\right)}{R_2+R_3//\left(R_4+R_5\right)}\cdot\frac{R_5}{R_4+R_5}V_{CA(np)} \tag{19}$$

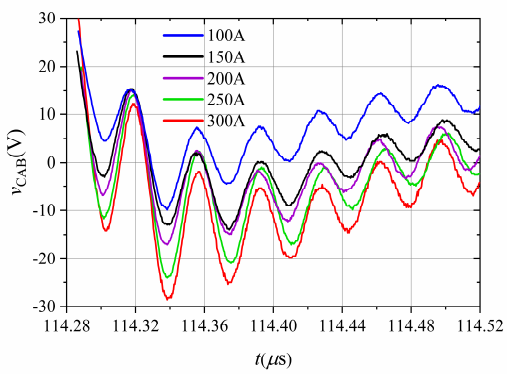
The measured negative peak of v_{out} gradually decreases with the increment in the number of disconnected bond wires during the long-term health diagnosis. By comparing with the reference peak value, the degree of bond-wire breakage can be judged. The operational reliability of the IGBT device is improved with a low extra cost. The signal processing of the control platform for the monitoring of bond wires faults is the same as that of the existing drive unit power supply detection

and overcurrent protection functions.

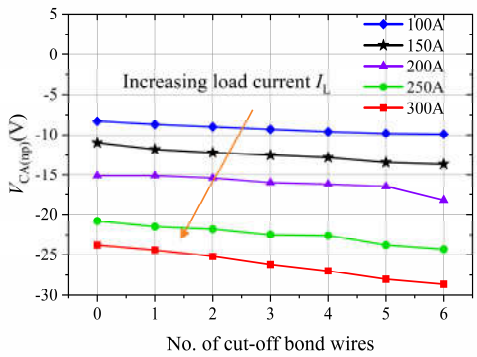
In terms of development trend, gate drivers will integrate richer functions, increase the complexity of device management, including performance improvement and active health management, and develop towards digitalization. In commercial MMCs, the specific gate drivers used inherently include custom-made collector voltage (V_{ce}) measurement circuits to realize the fault diagnosis and overcurrent protection of the IGBT module. The monitoring method proposed in this paper is realized by measuring the collector voltage at the pre-existed terminals available on module packaging and is even designed to be combined with the widely adopted short-circuit detection circuit on the gate driver. Also, even the existing ADC and data transmission fiber on an advanced digitalized gate driver can be shared and utilized to reduce the cost. With the proposed monitoring method, no new measurement port is added to the MMC, and the existing control mode is not changed. Only the signal post-processing part of the existing driver needs to be slightly modified.

B. Influence of the load current I_L

During the normal operation of the MMC, the load current I_L of the IGBT device will change according to an approximate sinusoidal law according to the modulation strategy. The change of I_L affects the collector current change rate $-\mathrm{d}i_T/\mathrm{d}t$ during the turn-off process, which in turn affects the undershoot peak value of the collector voltage. The change of I_L affects the rate of change of collector current $-\mathrm{d}i_B/\mathrm{d}t$ in turn-off process and then affects the undershoot peak of collector voltage $V_{CA(np)}$. The rate of change of i_T can be expressed as [26],[27]:



(a)



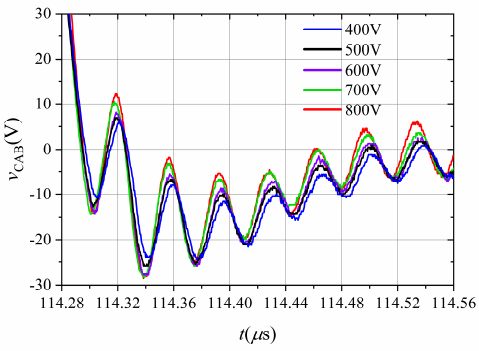
(b)

Fig.7 (a) v_{CAB} changes with load current I_L after six bond wires cut off. 25℃, 800V (b) Behaviors of $V_{CA(np)}$ with changes in I_L and the number of cut-off bond wires at 25℃.

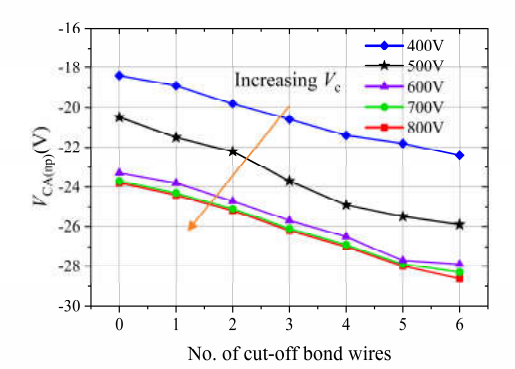
$$\frac{\mathrm{d}i_T}{\mathrm{d}t}=\frac{\mathrm{d}v_{GE}}{\mathrm{d}t}\cdot\left[\frac{1}{1-\alpha_{PNP}(T)}\right]\cdot\left[\mu_n(T)\cdot C_{ox}\cdot\frac{W}{L}\cdot\left(v_{GE}-v_{GE,th}(T)\right)\right] \tag{20}$$

α_{PNP} is the gain of the internal bipolar transistor, μ_n is the electron mobility, W/L is the ratio of the width to the length of the conduction channel. The load current I_L affects the BJT current gain α_{PNP} and the MOS channel width-to-length ratio W/L, which in turn affects the $\mathrm{d}i_T/\mathrm{d}t$. With the load current I_L increases, the maximum value of $-\mathrm{d}i_T/\mathrm{d}t$ decreases [17], and accordingly $V_{CA(np)}$ decreases.

When the load current I_L is set to 100A, 150A, 200A, 250A, and 300A, the experimental waveforms of v_{CAB} after six bond wires cut-off are shown in Fig.7(a). The capacitor voltage is 800V, and the junction temperature is 25°C. The variation of $V_{CA(np)}$ with load current I_L in the different number of bond wires cut off is shown in Fig.7(b). As the number of bond wires cut off increases, $V_{CA(np)}$ decreases. In the process of increasing the load current I_L from 100A to 300A, $V_{CA(np)}$ in the health state and after the bond wires cut-off are both decreased simultaneously. The change of load current interferes with the bond wire monitoring results. The amount of change between $V_{CA(np)\_6}$ (six bond wires cut-off) and $V_{CA(np)\_0}$ (healthy state)increases from 1.6 to 4.8V with the increase of load current.



(a)



(b)

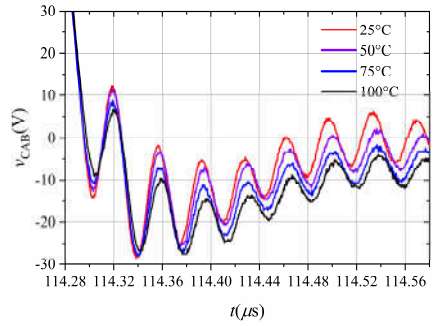
Fig.8 (a) v_{CAB} changes with capacitor voltage V_c after six bond wires cut off at 25℃, 300A. (b) Behaviors of $V_{CA(np)}$ with changes in V_c and the number of cut-off bond wires at 25℃.

C. Influence of the capacitor voltage V_c

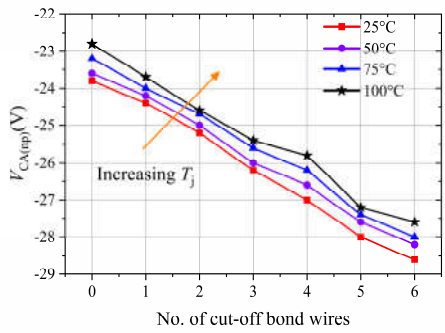
Since the submodule capacitor voltage frequently fluctuates in the real application, it is therefore of great importance to identify their influence. The maximum di_T/dt increases with the submodule capacitor voltage V_{dc} [17], and so does the magnitude of $V_{CA(np)}$. Given the load current I_L of 300A at the junction temperature of 25°C, the dynamic waveforms of v_{CAB} in response to the variations of the submodule capacitor voltages ranging from 400V to 800V are shown in Fig.8(a). The corresponding variations of $V_{CA(np)}$ for one to six lift-off bond wires with respect to changing V_{dc} are shown in Fig.8(b). Experimental results show that $V_{CA(np)}$ rises negatively with the increasing V_c. The amount of change between $V_{CA(np)\_6}$ (six bond wires cut-off) and $V_{CA(np)\_0}$ (healthy state)increases from 4.0V to 4.8V with the increase of capacitor voltage. The capacitor voltage has little effect on $V_{CA(np)}$ monitoring IGBT wire bonding faults.

D. Influence of the junction temperature T_j

The junction temperature T_j is an important factor that affects the current edge rate of the controlled IGBT during its turn-off transient, which can be attributed to the temperature dependence of the internal bipolar transistor gain α_{PNP}, electron mobility μ_n and threshold voltage $v_{GE,th}$. As the junction temperature rises, the collector current edge rate di_T/dt decreases [17], and $V_{CA(np)}$ increases accordingly. With the IGBT device junction temperature set to 25°C, 50°C, 75°C, and 100°C, the collector voltage v_{CAB} after six bond wires cut off is shown in Fig.9(a). The capacitor voltage V_c is 800V and the load current I_L is 300A. The variation of $V_{CA(np)}$ with junction temperature T_j in different numbers of bond wires cut off is shown in Fig.9(b). The experimental results show that in the same number of cut-off bond wires, the junction temperature T_j increases and $V_{CA(np)}$ increases. In the process of increasing the capacitor voltage, V_c from 25°C to 100°C, the change of junction temperature affects the identification of the number of bond wires cut-off. The amount of change between $V_{CA(np)\_6}$ (six bond wires cut-off) and $V_{CA(np)\_0}$ (healthy state)increases from 3.8V to 4.8V with the increase of junction temperature.



(a)



(b)

Fig.9 (a) v_{CAB} changes with junction temperature T_j after six bond wires cut off (b) Behaviors of $V_{CA(np)}$ with changes in T_J and the number of cut-off bond wires.

IV. MMC Submodules Application Analysis

When the monitoring method is applied to IGBT module bond wires fatigue of the MMC half-bridge submodules, the load current, capacitor voltage, and junction temperature affect the monitoring sensitivity change with the MMC operating conditions. A detailed analysis of the three aspects will be carried out.

Similar to any other multilevel converter topology, MMC has an active voltage balance strategy to balance and maintain SM capacitor voltage, the capacitor voltage fluctuates within 5% of the rated voltage [28],[29]. The relative variation of $V_{CA(np)}$ in the healthy state and after 6 bond wires cut off are both less than 1.1%. Therefore, when the monitoring method is applied to the MMC half-bridge submodules, the impact of capacitor voltage fluctuations can be ignored.

The load current I_L of the SM IGBT module contains the DC component, the fundamental frequency AC component, and the phase legs circulating current component [30],[31]. The load

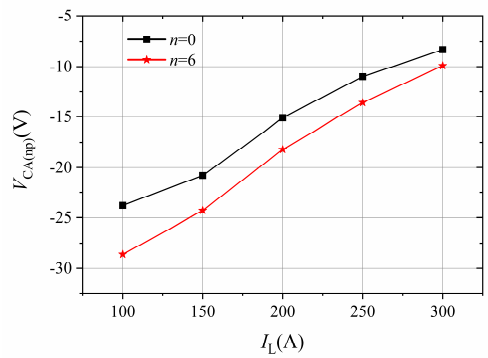


Fig.10 The experimental results of $V_{CA(np)}$ changes with load current I_L in the healthy state and after six bond wires cut off.

current I_L changes approximately sinusoidally with the current on the AC side of the MMC, and its influence on $V_{CA(np)}$ cannot be ignored. The experimental results of the undershoot $V_{CA(np)}$ of the collector voltage changes with load current I_L in the healthy state and after six bond wires cut off are shown in Fig.10. The relationship between $V_{CA(np)}$ and I_L can be approximated to a linear curve. Similarly, the relationship between $V_{CA(np)}$ and I_L can also be approximated as a linear curve.

In the healthy state, the experimental results of $V_{CA(np)\_0}$ with I_L and T_j can be fitted to the following expressions as a baseline value for verification:

$$V_{CA(np)\_0} = -0.0817 I_L + 0.0155 T_j + 0.1418 \quad (21)$$

After six bond wires cut off, the experimental results of $V_{CA(np)\_6}$ with I_L and T_j can be fitted to the following expressions as a failure threshold value:

$$V_{CA(np)\_6} = -0.0962 I_L + 0.0121 T_j + 0.0164 \quad (22)$$

Through the correction of the baseline value, the degree of IGBT wire bonding fault can be identified by comparing the actually measured $V_{CA(np)}$ with the baseline value and the failure threshold value. Considering the manufacturing spread in the parameters, pre-calibration for the IGBT modules from different batches can be executed before applying the proposed method in the field to ensure effective detection and accuracy. In practical application, the measurement circuit integrated in the gate driver is susceptible to electromagnetic interference from space, which could cause false alarms. It is necessary to analyze the electromagnetic field where the gate driver is located, and design professional electromagnetic shielding measures.

It is worth noting that although the method proposed in this paper is proposed for half-bridge MMC, it can be widely used in power electronic converters including basic half-bridge structures, such as full-bridge MMC, two-level converter, chain SVG, etc

V. Conclusion

A novel HSEP $V_{CA(np)}$, the collector voltage undershoot, for the wire bonding failure of a mIGBT module is established with high sensibility, easy access, and a simple readout circuit for the in-situ health monitoring. Some existing methods [13, 23] are only valid for the detection of more serious bond wire failures, once the entire loss of connection from one out of several parallel chips is resulted. In comparison, this method provides the chip-level bond wire failure detection with increased granularity and it allows the diagnosis of the wire bonding failure evolving in any parallel chip in an mIGBT module. The proposed method has been verified with effectiveness using theoretical analysis and experimental results. Its main conclusions appear as follows:

1) The proposed method can effectively monitor the degradation level when the bond wire fatigue takes place for a single chip in a mIGBT module, the relative sensitivity increases with the number of bond wires manifesting lift-off failures. For example, when the bond wire lift-off happens for 1 and 6 out of 13 bond wires, their relative sensitivity is about 2.5% and 19.7%, respectively.

2) As an HSEP, $V_{CA(np)}$ is less affected by the changing submodule capacitor voltage V_c in the MMC submodule application, whose impact can be ignored. However, $V_{CA(np)}$ is largely affected by other changing operating conditions. It decreases with the increasing load current I_L or with the decreasing junction temperature T_j. The linear relationship showing the dependence of $V_{CA(np)}$ on either I_L or T_j is given in both the healthy and the aging status with reference to the bond wire lift-off conditions.

3) The readout circuit for the in-situ monitoring and aging degree detection for bond wire failure of mIGBT modules are discussed. It also provides the integrated desaturation detection function for the overcurrent protection.

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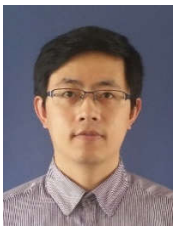

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