A 40-Pulse Autotransformer Rectifier Based on New Pulse Multiplication Circuit for Aviation Application

Abdollahi, Rohollah ; B. Gharehpetian, Gevork; Anvari-Moghaddam, Amjad; Blaabjerg, Frede

Published in:
I E E E Transactions on Industrial Electronics

DOI (link to publication from Publisher):
10.1109/TIE.2022.3227229

Publication date:
2023

Document Version
Accepted author manuscript, peer reviewed version

Citation for published version (APA):
Abdollahi, R., B. Gharehpetian, G., Anvari-Moghaddam, A., & Blaabjerg, F. (2023). A 40-Pulse Autotransformer Rectifier Based on New Pulse Multiplication Circuit for Aviation Application. *I E E E Transactions on Industrial Electronics*, *70*(11), 10822 - 10832. Article 9982680. https://doi.org/10.1109/TIE.2022.3227229

A 40-Pulse Autotransformer Rectifier Based on New Pulse Multiplication Circuit for Aviation Application

R. Abdollahi, and G. B. Gharehpetian, *Senior Member IEEE*, A. Anvari-Moghaddam, *Senior Member, IEEE, and* F. Blaabjerg, *Fellow, IEEE*

***Abstract*- In this paper, a new simple pulse multiplication circuit (SPMC) with low current stress is proposed, in order to upgrade a normal 20-pulse autotransformer rectifier (20PAR) to a 40PAR. The proposed SPMC comprises two tapped inter-phase reactors (TIPRs) and two additional diodes with lower conduction losses. The proposed SPMC does not require a zero-sequence blocking transformer (ZSBT) compared to conventional pulse multiplication circuits, which leads to simplicity in implementation. Simulation and experimental results show that the total harmonic distortion (THD) of the input current using 40PAR is less than 3%, which meets the DO-160G requirements for aviation applications.**

INDEX TERMS: 40-pulse autotransformer rectifier (40PAR), Pulse multiplication circuit, Tapped inter-phase reactor (TIPR), Harmonic suppression, Aviation application.

I. INTRODUCTION

The multi-pulse rectifiers have widely been used in aviation and shipboard power networks. In order to meet the related harmonic standards, many useful harmonic reduction methods have been presented. Also, various approaches have been offered to decrease the input current total harmonic distortion (THD) to meet the IEEE standard 519 which sets the goals for harmonic control in electric power systems [1]. Generally, they can be divided into three types. The first type uses passive and active power filters to suppress the input current harmonics produced by the rectifier. However, in several industrial applications, the capacity of the filter is large, which results in increased cost and volume [2-3]. In the second group, the pulse number is increased by increasing the number of output phases of the phase-shifting transformer. This method has been used to obtain 12 [4-5], 18 [6], 20 [7-8], 24 [9], 30 [10], 36 [11], and 44 [12] pulse rectifiers (PRs). However, by increasing the pulse number, the windings of the transformer and the components used in the rectifier will be increased, which results in a complicated structure and increased costs. The third type applies a pulse multiplication circuit (PMC) instead of a conventional inter-phase reactor (IPR) to multiply the pulse quantity of the rectifier [13-17]. The PMCs can be divided into three groups: active [13-14], hybrid [15], and passive [16-17] PMCs. While passive PMCs have simpler topologies, their performance is limited and inferior to that of active PMCs. However, active PMCs need control and drive circuits. In a hybrid PMC, the active part should eliminate high-order harmonics, and the passive part must increase the pulse number.

It should be noted that the active PMC has higher costs and it is less reliable because it requires control systems and accurate measurement of control variables. Therefore, passive PMCs have been considered by many researchers. To tackle the problem, the passive PMCs have been proposed for upgrading 12 pulse rectifiers (12PRs) in [18-23]. In [18-19], the pulses have been increased from 12 to 24, and in [20-23], the researchers have increased the number of pulses in the 12PR to 36 pulses. Furthermore, this method has also been used to upgrade a 20PR to 40 pulses [24-26], and also to upgrade a 36PR to 72 pulses [27-28].

To decrease the input current THD in aviation applications such as Airbus A380/A350 and Boeing 787, several multi-pulse autotransformer rectifiers (MPARs) have been presented [29]. The 18PRs are vastly employed as electric power conversion equipment for aviation power supply systems owing to their simple structure, low cost, and high reliability [30]. However, when the 18PRs are used alone, a series of $18n \pm 1$ order harmonics are injected into the utility interface, which will lower the power quality [31]. In [32], an 18PAR has been presented for input current harmonic reduction in aviation applications. The input current THD in this 18PAR is even more than 6% under full load, which certainly increases the input current THD in light load conditions. In addition, this 18PAR requires a filter to comply with the DO-160G standard [33]. To reduce the input current THD in industrial [34] and aviation [35] applications, several 20PARs have been presented.

TABLE I
CURRENT HARMONICS LIMITS BASED ON IEEE-519 AND DO-160 G

<table>
<tr><td colspan="12">IEEE-519</td></tr>
<tr><td>Harmonic order</td><td>I_{SC}/I_L</td><td>$3 \le h < 11$</td><td>$11 \le h < 17$</td><td>$17 \le h < 23$</td><td>$23 \le h < 35$</td><td>$35 \le h \le 50$</td><td colspan="5">THD</td></tr>
<tr><td>%</td><td><20</td><td>4.0</td><td>2.0</td><td>1.5</td><td>0.6</td><td>0.3</td><td colspan="5">5.0</td></tr>
<tr><td colspan="12">DO-160 G</td></tr>
<tr><td>Harmonic Order</td><td rowspan="2">Odd harmonics</td><td>3rd, 5th, 7th</td><td>Odd Triplen Harmonics (h = 9, 15, 21, ..., 39)</td><td>11th</td><td>13th</td><td>Odd Non Triplen Harmonics 17, 19</td><td>Odd Non Triplen Harmonics 23, 25</td><td>Odd Non Triplen Harmonics 29, 31, 35, 37</td><td rowspan="2">Even harmonics</td><td>Even Harmonics 2 and 4</td><td>Even Harmonics > 4 (h = 6, 8, 10, ..., 40)</td></tr>
<tr><td>Limits</td><td>$I_3 = I_5 = I_7 = 0.02 I1$</td><td>$I_h = 0.1 I_1/h$</td><td>$I_{11} = 0.1 I_1$</td><td>$I_{13} = 0.08 I_1$</td><td>$I_{17} = I_{19} = 0.04 I1$</td><td>$I_{23} = I_{25} = 0.03 I1$</td><td>$I_h = 0.3 I_1/h$</td><td>$I_h = 0.01 I_1/h$</td><td>$I_h = 0.0025 I_1$</td></tr>
</table>

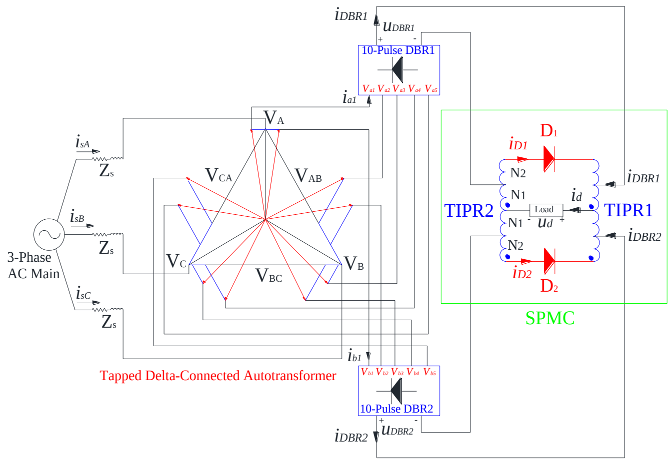


Fig.1. Proposed 40PAR based on a simple pulse multiplication circuit (SPMC)

Although the input current THD in 20PAR [35] is less than 5% and complies with the IEEE 519 standard, this 20PAR cannot be used in aviation applications without the use of input and output filters (i.e, it cannot meet the limitations of the 21st and 39th harmonics according to DO-160G (see Table I)).

To solve this problem, the use of a pulse multiplication circuit (PMC) is suggested as an economical and effective solution. In [36], a 20PAR with a pulse doubling circuit at the DC link has been presented which can meet the DO-160G requirements without using any input and output filter. However, to ensure the independent operation of two 10-pulse diode bridge rectifiers (DBRs), this structure requires a zero-sequence blocking transformer (ZSBT) circuit, which leads to an increase in the complexity of the 40PAR. Also, in [37], a 48PR using a 12PR with two harmonic reduction circuits in the dc-link has been presented to reduce the harmonic distortion of the input current in aviation applications. This 48PAR requires two 6-phase autotransformers, four 6-pulse DBRs, two ZSBTs, three tapped IPRs (TIPR), and 6 additional diodes, which leads to a complicated structure. It should be noted that the structure of this 48PR requires ZSBT with a rating of 7.57% of load power. Also, current stress and conduction losses of the additional diode are high in this pulse doubling circuit. In [38], the pulse multiplication circuit methods of parallel-connected 12PRs have accurately been classified. It should be noted that to use all of these pulse multiplication circuits in MPARs, they need a ZSBT, which leads to the higher complexity of the structure. In this paper, a new simple pulse multiplication circuit (SPMC) is proposed to lower the input current THD and output voltage ripple without increasing the complexity of 20PAR. It does not employ ZSBT and meets the DO-160G requirements. The advantages of the proposed 40PAR are as follows:

- In this 40PAR, an SPMC with low current stress and less diode conductivity losses is proposed to upgrade a typical 20PAR.
- The proposed SPMC does not require (ZSBT) compared to a conventional PMC, which leads to simplicity in implementation.
- The current passing through the additional diodes of the proposed SPMC is so low that compared to the load current, leads to a decrease in the conduction losses and the current stress of the proposed SPMC.
- Compared to the other 40PAR, the proposed 40PAR has a lower kVA rating.
- At 50Hz, the input current THD of the suggested 40PAR is 0.29% and 1.84%, at full and light load conditions, which is less than 3% and thereby within IEEE-519 requirements.
- At 400Hz-800Hz, input current harmonic components of the suggested 40PAR are less than the DO-160G standard limitations without using any input and output filters, which are suitable for aviation applications.
- The suggested 40PAR in comparison with other existing solutions, has higher efficiency, lower input current THD, less conduction losses, lower current stress, and also, less kVA, weight, and cost.

The rest of this paper is arranged as follows. In the second part, the structure of the proposed 40PAR is described. In the third part, in order to evaluate the performance of the proposed rectifier according to IEEE standard 519, the proposed rectifier is simulated and analyzed at grid frequency (50Hz). In the fourth part, to evaluate the feasibility of using the proposed 40PAR in aviation applications, the proposed rectifier is simulated and analyzed at 400Hz and 800Hz according to the DO-160G standard. In the fifth section, to confirm the simulation results, a laboratory prototype of the proposed 40PAR is made and tested. In the sixth section, for technical and economic evaluations, a comparison of the proposed 40PAR with the existing 40PAR is presented. In the last section, the conclusions are given.

II. PROPOSED 40PAR TOPOLOGY

A. Topology of proposed 40PAR

As shown in Fig. 1, the proposed 40PAR consists of two main sections:

- A typical 20PAR
- New SPMC

The 20PAR includes a tapped delta-connected 10-phase autotransformer with a low kVA rating to produce two sets of 5-phase voltages with a 18º phase shift. These two 5-phase voltage sets are passed through two 10-pulse DBRs to create a 20-pulse waveform. By connecting the proposed SPMC to the DC bus of these two 10-pulse DBRs, the 20-pulse waveform is increased to 40 pulses. The conventional 40PAR consists of two 10-pulse DBRs and a ZSBT and a PMC [24-26]. Autotransformer-based MPRs require a ZSBT to ensure the independent operation of DBRs: however, in the proposed 40PAR, an SPMC is used to upgrade the 20PAR to 40PAR, which eliminates the need of using a ZSBT. The SPMC consists of two tapped inter-phase reactors (TIPRs) and two addition diodes. Each of the TIPRs is installed in the positive and negative polarity of 10-pulse DBRs. Then, the two TIPRs are connected through two additional diodes. Finally, the two

TIPRs are connected to the load. As seen in Fig. 2, u_{T1} and u_{T2} are equal to the sum of the voltages of the windings N_1 and N_2 in TIPR1 and TIPR2, respectively. Also, u_d is the voltage across the load. In this paper, considering the turn ratio of windings N_1 and N_2, the turn ratio of the TIPR is selected to be $m=(N_1+N_2)/2N_1$.

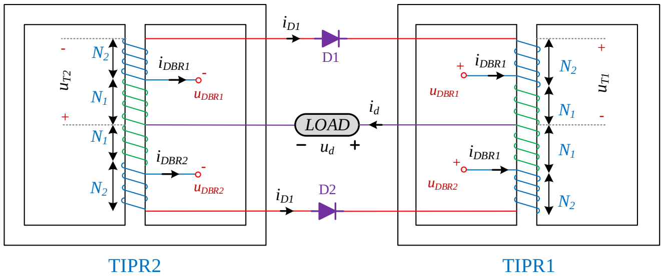


Fig. 2. Winding structure of two TIPRs in SPMC.

B. Working principle of the proposed SPMC

In Fig. 3, the structure of the proposed SPMC is given. In this figure, according to the relationship between load voltage u_d and voltage ($u_{T1}+u_{T2}$), the proposed SPMC has three working modes.

Working Mode 1 ($|u_{T1} + u_{T2}| < u_d$): As shown in Fig. 3(a), in this mode, two additional diodes D_1 and D_2 are reverse-biased and off, the currents $i_{D1} = i_{D2} = 0$, and the proposed 40PAR behaves as a conventional 20PAR. From Kirchhoff's Current Law (KCL) and Magnetic Motive Force (MMF) balance of the windings in the two TIPRs, the relationship among the output current i_{DBR1} of DBR1, the output current i_{DBR2} of DBR2 and load current i_d is given as follows:

$$i_{DBR1} = i_{DBR2} = \frac{1}{2} i_d \tag{1}$$

Working Mode 2($u_{T1} + u_{T2} > u_d$): As shown in Fig. 3(b), in this mode, only the additional diode D_2 turns on. The current $i_{D2} > 0$. The DBR1 is turned on: its output current is $i_{DBR1} > 0$. Meanwhile, the DBR2 is turned off, and its output current $i_{DBR2} = 0$. In terms of KCL and the MMF of two TIPRs, i_{DBR1} and i_{D2} are obtained as follows:

$$\begin{cases} i_{DBR1} = \frac{2m}{2m+1} i_d \\ i_{D2} = \frac{1}{2m+1} i_d \end{cases} \tag{2}$$

Working Mode 3($-(u_{T1} + u_{T2}) > u_d$): As shown in Fig. 3(c), in this mode, only the additional diode D_1 is turned on. The current $i_{D1} > 0$. The DBR2 is turned on; its output current is $i_{DBR2} > 0$. Meanwhile, the DBR1 is switched off, and its output current is $i_{DBR1} = 0$. In terms of KCL and the MMF of the two TIPRs, the currents i_{DBR2} and i_{D1} are given as follows:

$$\begin{cases} i_{DBR2} = \frac{2m}{2m+1} i_d \\ i_{D1} = \frac{1}{2m+1} i_d \end{cases} \tag{3}$$

Fig. 4 shows the simulation results on the relationship between u_d and ($u_{T1}+u_{T2}$). As seen in Fig. 4, considering the connection between $u_{T1}+u_{T2}$ and u_d, three working modes are defined for the SPMC circuit. In this figure, if $|u_{T1} + u_{T2}| < u_d$, i.e., blue and red waveforms are less than the black one, the period is named working mode 1. In working mode 2, where $u_{T1} + u_{T2} > u_d$, the blue waveform is higher than the black waveform. In the period called working mode 3, $-(u_{T1} + u_{T2}) > u_d$, i.e., the red waveform is higher than the black one.

In Fig. 4, the variations of the input current THD versus the TIPR turn ratio are shown. It can be seen that in the range of 10-20, the THD is less than 1%. Also, in the range of 5-50, the THD is less than 2%, which is suitable for the aircraft industry and also, and it shows low sensitivity to TIPR turn ratio variations. However, the proposed 40PAR has the lowest THD of 0.29% at m=14.17.

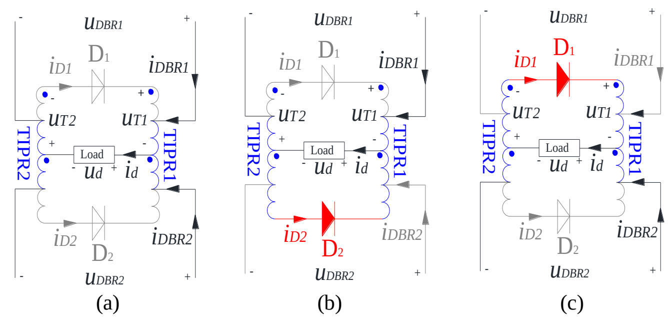


Fig. 3. Working modes of the proposed SPMC. (a) Mode 1, (b) Mode 2, and (c) Mode 3

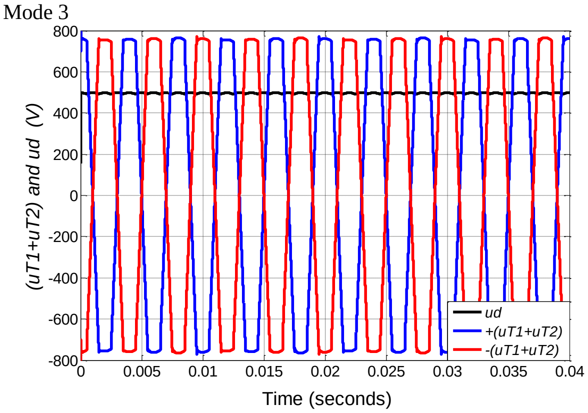


Fig. 4. Simulation results on the relationship between u_d and (u_{T1}+u_{T2})

The optimal turns ratio of the TIPR (i.e., m) is obtained based on the minimum %THD of the input current. To achieve this goal, many simulations with different m have been carried out and the input current THD of each case has been determined. The results are presented in Fig. 5. In this figure, TIPR turns ratio of 14.17 results in an input current THD of 0.29%. Therefore, designing the optimal TIPR turns ratio is the main purpose of the proposed SPMC, which plays an important role in reducing the %THD of the input current.

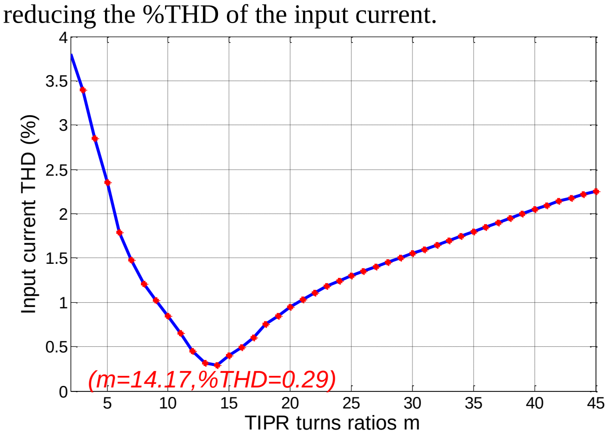
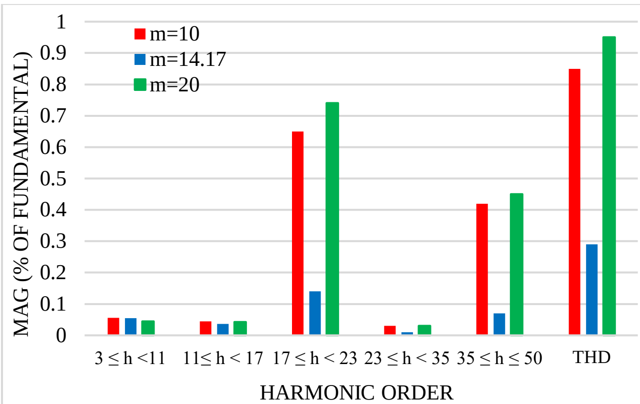
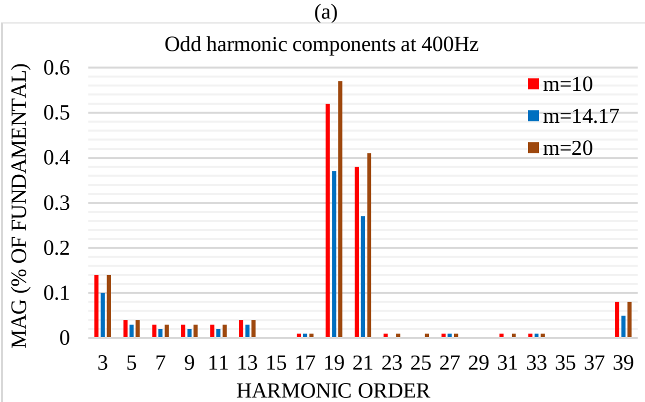


Fig. 5. Simulation results on variation in m with %THD of input current at 50 HZ

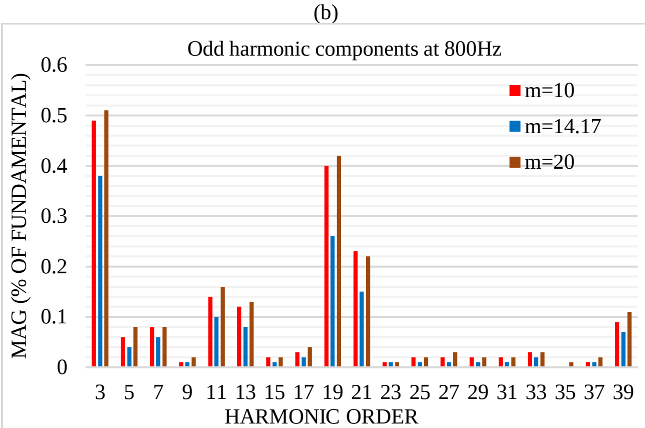
As a result, it improves the ability to reduce the input current THD in 20PAR suitably. To show the optimality of the value of the TIPR turn ratio, i.e., *m*=14.17, simulations with other TIPR turn ratios are carried out at 50Hz in accordance with IEEE-519 and at 400/800 Hz in accordance with DO-160G. The input current THD of the proposed rectifier with *m*= 10, 14.17, and 20, is shown in Fig. 6(a), 6(b), and 6(c) at 50Hz, at 400 Hz and at 800, respectively. As can be seen in these figures, the best performance can be achieved with *m*=14.7, and also with other turn ratios, the proposed rectifier cannot satisfy the requirements of IEEE-519 and Do-160G.



(a)



(b)

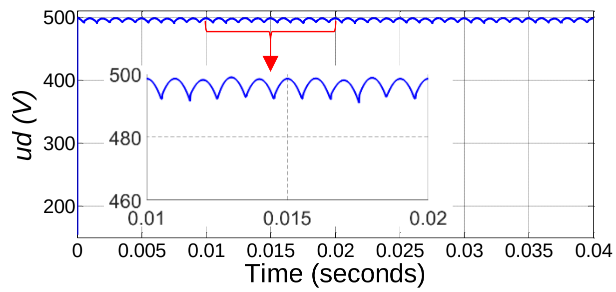


(c)

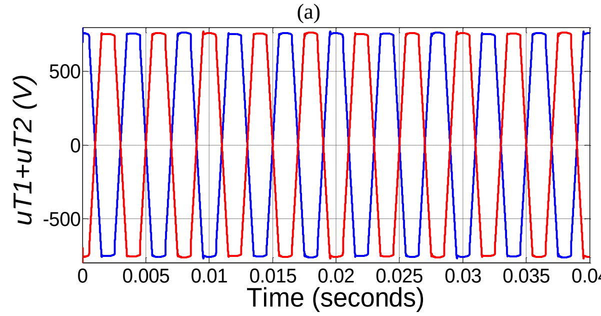
Fig. 6. Harmonic current limits of proposed 40PR with different turns ratios of the TIPR (*m*), (a) at 50Hz, (b) odd harmonic components at 400Hz, and (c) odd harmonic.

III. SIMULATION RESULTS AND ANALYSIS AT 50Hz

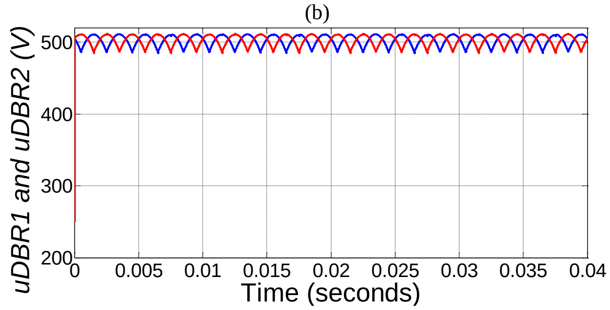
To evaluate the performance of the proposed rectifier following IEEE standard 519, the proposed 40PAR is simulated and analyzed at a typical grid frequency (50Hz). The load power is 10kW modeled as a resistor, which consumes about 20A. Figs. 7 and 8 show the main voltage and current of the proposed 40PAR with SPMC. The proposed rectifier output voltage waveform is shown in Fig. 7(a) and the TIPR1 and TIPR2 voltage waveforms are shown in Fig. 7(b). As mentioned before, the relationship between these voltages determines the operating modes of the SPMC. The output voltage of two 10-pulse DBRs is shown in Fig. 7(c). As can be seen in this figure, using the SPMC in the proposed 40PAR, the operational independence of these two DBRs is confirmed without the need for ZSBT.



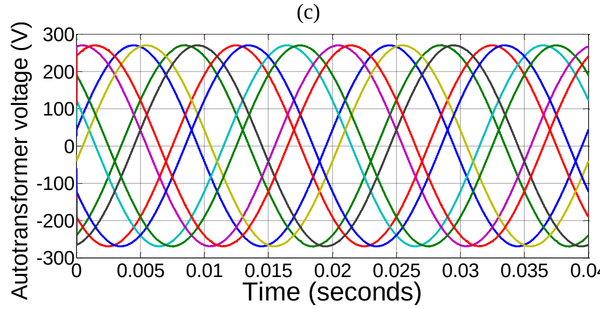
(a)



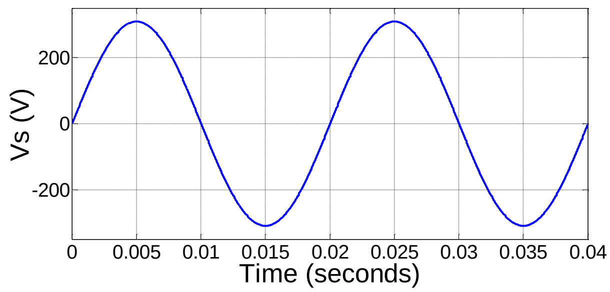
(b)



(c)



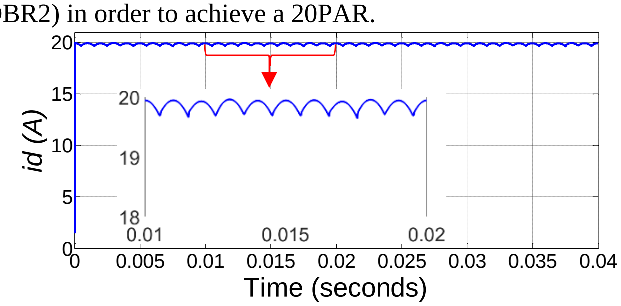
(d)



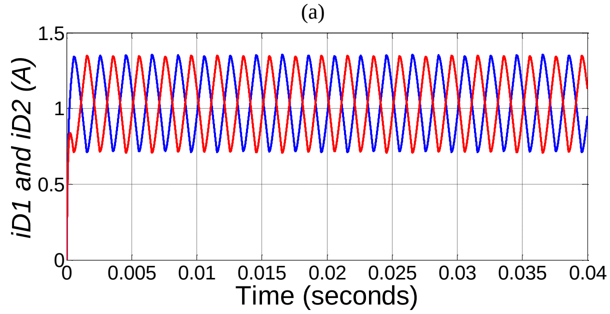
(e)

Fig. 7. Main voltage waveforms of the proposed 40PAR with SPMC. (a) u_d, (b) $u_{T1} + u_{T2}$, (c) autotransformer output voltage, (d) u_{DBR1} and u_{DBR2}, (e) V_S

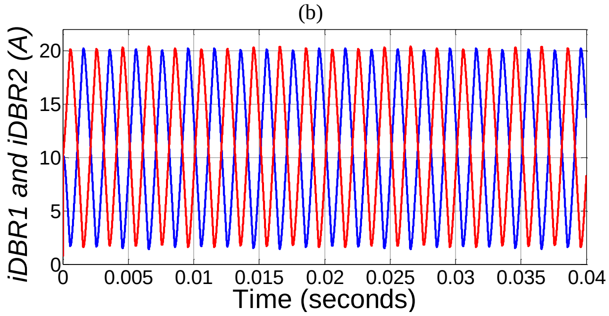
Fig. 7(d) shows the output waveform of a 10-phase autotransformer, which consists of two series of 5-phase voltages with 18-degree displacement. These two series of 5-phase voltages supply two 10-pulse diode bridges (DBR1 and DBR2) in order to achieve a 20PAR.



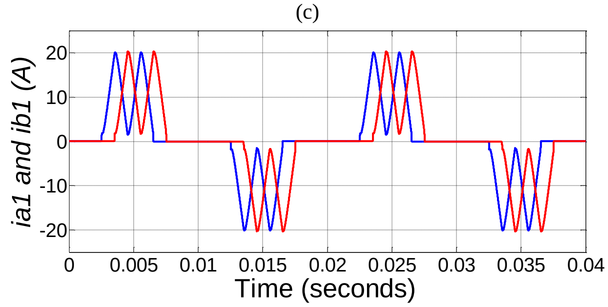
(a)



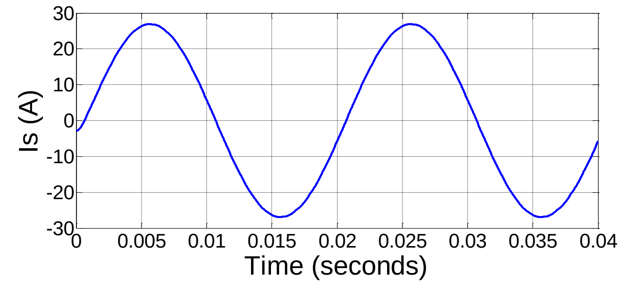
(b)



(c)



(d)



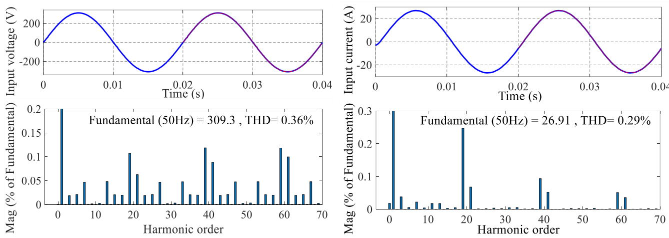
(e)

Fig. 8. Main current waveforms of the proposed 20PAR with proposed SPMC. (a) i_d, (b) i_{D1} and i_{D2}, (c) i_{DBR1} and i_{DBR2}, (d) i_{a1} and i_{b1}, (e) I_S

The input voltage waveform is also shown in Fig. 7(e). The proposed rectifier output current waveform is shown in Fig. 8(a). The currents flowing through the additional diodes (i_{D1} and i_{D2}) are shown in Fig. 8(b) and the current flowing through the TIPRs (i_{DBR1} and i_{DBR2}) is shown in Fig. 8(c). As it can be seen, a great part of the load current passes through the TIPRs and the current passing through the additional diodes is very small compared to the load current, which leads to a reduction in conduction losses and the current stress of the additional diodes. The input currents of these two diode bridges are shown in Fig. 8(d) and the input current of the proposed 40PAR is shown in Fig. 8(e). Fig. 8(e) confirms the high performance of the proposed 40PAR in reducing the harmonic distortions of the input current, and thus, providing a fully sinusoidal current.

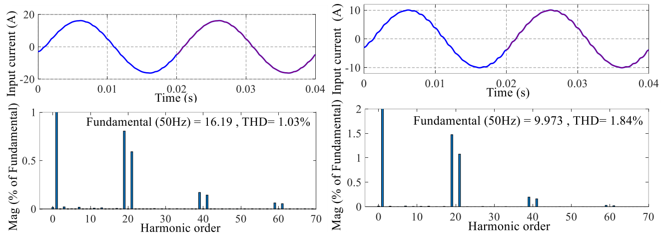
Fig. 9 shows the input voltage/current and their harmonic spectrums of the proposed 40PAR with SPMC (at full load). After using the SPMC in the proposed 40PAR, the simulated THD of the voltage and current are about 0.36% and 0.29%, respectively. Also, the source inductance has no effect on the optimal value of m. However, it should be mentioned that as discussed in [39], the source inductance is a very important parameter affecting the input current THD in different structures of multi-pulse rectifiers. Increasing the input current THD results in the input current THD [39]. In this study, this inductance is very low (0.03 mH), but the results are very good in comparison with the other 40 pulse rectifiers.

Also, for a more accurate evaluation, the input current THD of the proposed 40PAR under different loads is shown in Fig. 10. Under 50% of full load power, the input current THD is about 1.03%, and under 20% of the full load power, the input current THD is about 1.84%. Compared to full load power, the input current THD increases under light load but is still much lower than IEEE standard 519 standard requirements. Therefore, the harmonic reduction ability of the proposed SPMC is significant. The proposed solution is simulated under different loading conditions (20-100% of full load). The power factor and input current THD variations for the proposed 40PAR with SPMC are shown in Fig. 11(a) and Fig. 11(b), respectively. The results show that the input current of the proposed configuration has an almost unity power factor. Furthermore, in the worst case (light loads), the current THD is below 3%.



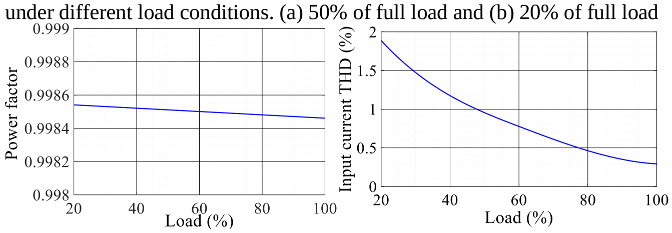
(a) (b)

Fig. 9. Input waveform and their harmonic spectrums of the proposed 40PAR with SPMC at full load. (a) voltage and (b) current



(a) (b)

Fig. 10. Input line current and harmonic spectrums of the proposed 40PAR under different load conditions. (a) 50% of full load and (b) 20% of full load

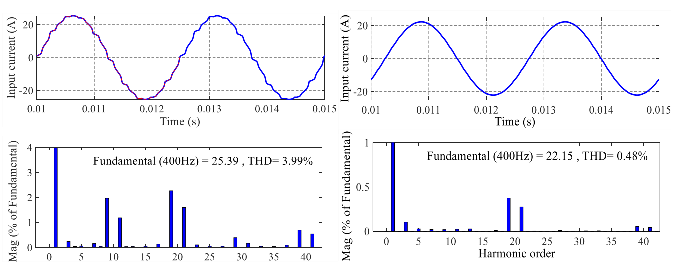


(a) (b)

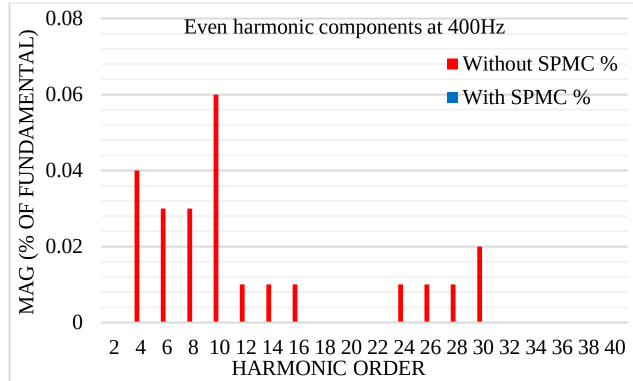
Fig. 11. Variation of (a) power factor and (b) %THD in proposed 40PAR with SPMC

IV. SIMULATION RESULTS AND ANALYSIS AT 400 Hz AND 800 Hz

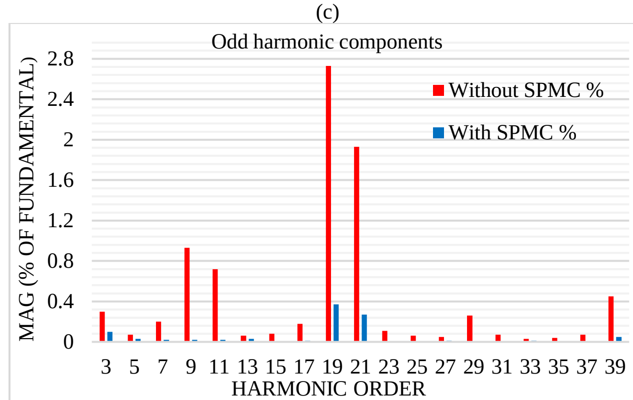
To evaluate the feasibility of using the proposed 40PAR in aviation applications, the proposed rectifier is next studied and analyzed at 400Hz and 800Hz for its ability to follow the DO-160G standard. Figs. 12 and 13 show the input current and their spectrums of rectifier with/without using SPMC at 400Hz and 800Hz, respectively. According to Figs. 12 and 13, it is clear that the input current THD at 400 Hz and 800 Hz are 0.48% and 0.51%, respectively. To more accurately evaluate the performance of the rectifier with/without using SPMC at 400Hz, the even and odd harmonic components compared to the DO-160G requirements are shown in Figs. 12(c) and 12(d), respectively. Similarly, at 800Hz the even and odd harmonic components compared to the DO-160G requirements are shown in Figs. 13(c) and 13(d), respectively.



(a) (b)



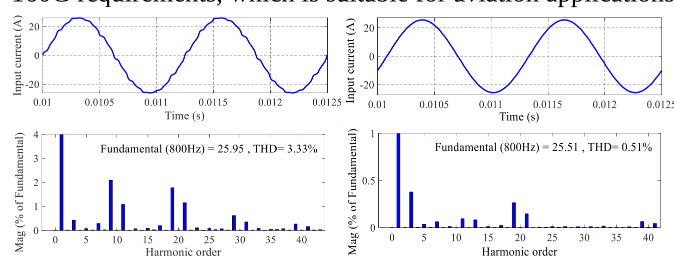
(c)



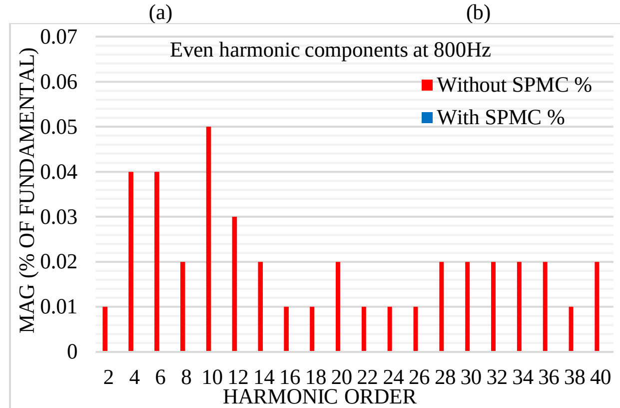
(d)

Fig. 12. Rectifier with/without using SPMC at 400Hz. (a) input current and their spectrums without SMPC, (b) input current and their spectrums with SMPC, (c) even harmonic components, and (d) odd harmonic components

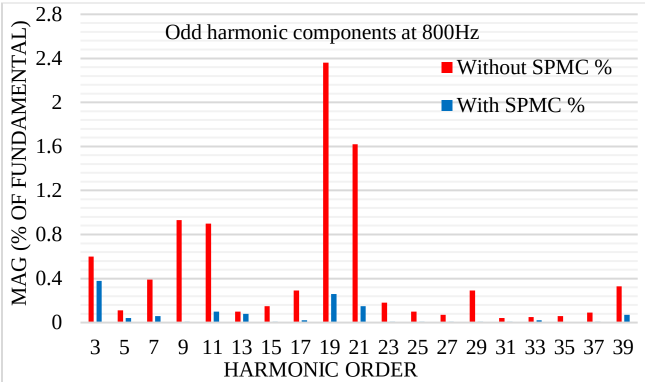
The results show that the amount of harmonic distortion of the 21st and 39th orders in the rectifier without using SPMC is more than the DO-160G limitations and a filter must be used to meet the DO-160G standard. But the proposed 40PAR with the SPMC does not need input and output filters and can meet DO-160G requirements, which is suitable for aviation applications.



(a) (b)



(c)



(d)

Fig. 13. Rectifier with/without using SPMC at 800Hz. (a) input current and their spectrums without SMPC, (b) input current and their spectrums with SMPC, (c) even harmonic components, and (d) odd harmonic components

Figs. 12(c) and 13(c) show the spectra of even harmonics at 400 Hz and 800 Hz, respectively. As can be seen in these figures, the magnitude of even harmonics of the 20PR without SPMC is low (less than 0.06%). Also, in the proposed 40PR, i.e., 20PR with SPMC, the even harmonics are very low (nearly zero) and neglectable.

V. EXPERIMENTAL VALIDATION

To verify the simulation results, a laboratory prototype of the proposed 40PAR with SMPC (as shown in Fig. 14) is made and tested under 380V/50Hz conditions. For light and full load tests, a variable resistive load is used. The line voltage is 380V, as a result, the dc link voltage is about 500V. Therefore, to model a 10 kVA load, the resistance of the load is adjusted to 25 and 50 ohms in full and light loads, respectively. For the proposed 40PAR, the experimental results of the input voltage/current and their spectrums under full load are shown in Fig. 15, and under light load (i.e., 50% the full load), the same results are presented in Fig. 16. As it can be seen, the input voltage and current THDs are about 0.53% and 0.98% under full load and about 0.42% and 2.76% under light load, respectively. It should be noted that as the load decreases, the voltage decreases but the current THD increases. However, the values of the voltage and current THD are always following the standard requirements.

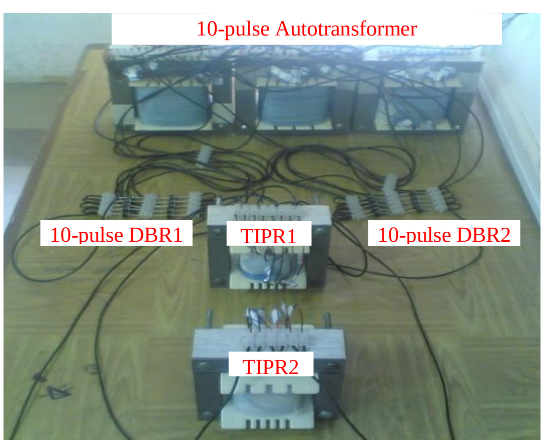
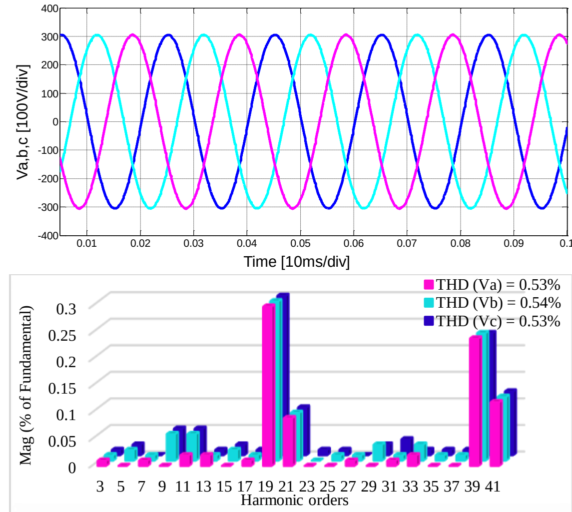
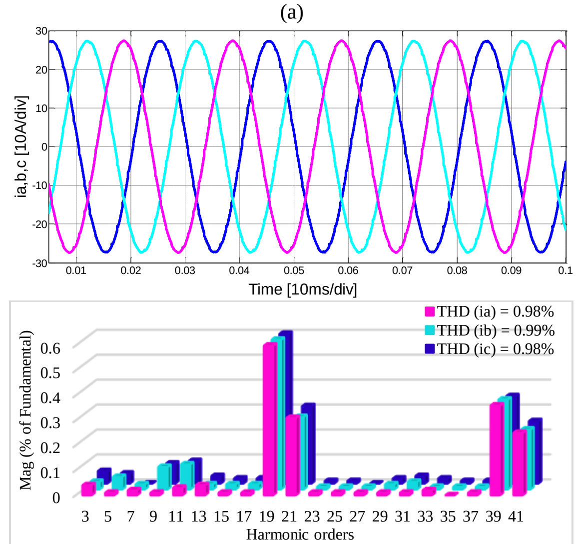


Fig. 14. A laboratory prototype of the proposed 40PAR with SMPC.

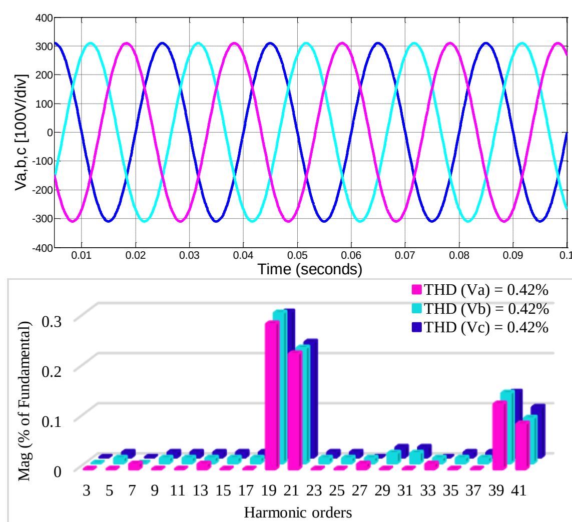


(a)

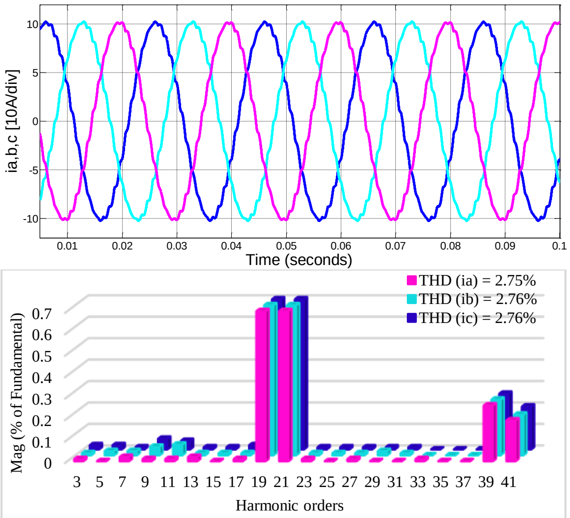


(b)

Fig. 15. Experimental results of input voltage/current and their harmonic spectrums of the proposed 40PAR under full load. (a) Voltage, and (b) Current



(a)



(b)

Fig. 16. Experimental results of input voltage/current and their harmonic spectrums of the proposed 40PAR under light load. (a) Voltage, and (b) Current

Also, the experimental results validate the simulation results and the high efficiency of the proposed 40PAR.

VI. Comparison of Proposed 40PAR with Existing 40PARs

To clarify the main characteristics of the proposed 40PAR, a technical and economic comparison is performed between the proposed 40PAR and the existing 40PARs in this section. Technical indexes are calculated in the previous sections and for economic evaluation, first, the kVA rating of the proposed 40PAR is calculated and then the cost is estimated according to the approach outlined in [39], where the cost of the transformer is estimated to be 4.5 times the kVA rating and a diode price is considered as 2.25$. The kVA rating of the components of the proposed 40PAR, including 10-phase autotransformers and two TIPRs, is calculated based on the following equation [31]:

$$S = 0.5 \sum V_{winding} I_{winding} \tag{4}$$

where $V_{winding}$ and $I_{winding}$ are the voltage and current rms of the windings of the 40PAR components obtained from simulations at under 10kW load. It can be seen that the kVA ratings of the 10-phase autotransformer and two TIPRs are 2.71 kVA, and 1.06 kVA, respectively. Therefore, the proposed 40PAR rating is 37.7% of the load power.

TABLE II
PARAMETERS USED IN THE CALCULATION OF LOSSES

Parameter	Symbol	Value
Material Coefficient	k_c	6.754×10^{-4}
Window Utilization Factor	K_u	0.4
AC/DC Resistance Factor	K_i	1.05
Maximum Flux Density	B_m	1.2 T
Current Density	J	2.3 A/mm^2
Electrical Resistivity of Cu	ρ_{cu}	2.3×10^{-8} Ωm
Exponent of Frequency	β	1.651
Exponent of Flux Density	α	1.559

The power losses of diodes are determined by considering the voltage drop of the diode (V_f = 0.7 V), the diode internal resistance (R_d = 1 mΩ), and the diode current (I_d =1.04 A), as follows:

$$P_{Diode} = \frac{1}{\pi}\int_0^{\pi}(V_f I_d + I_d^2 R_d)d\theta = V_f I_d + I_d^2 R_d \tag{5}$$

The iron and winding losses of the transformer are calculated as follows:

$$P_{core} = m_c k_c B_m^{\alpha} f_T^{\beta} \tag{6}$$

The copper losses can be determined by:

$$P_{copper} = \sum J \rho_{cu} (MLT_i) K_i N_i I_i \tag{7}$$

where, the mean length per turn *(MLT_i)*, the number of turns *(N_i)*, and the rms current of the i^{th} winding *(I_i)* have been given in [40]. The efficiency of the proposed 40PAR with the SMPC has been calculated based on simulations using equations (5)-(7) and the parameters listed in Table II. The total losses of the proposed 40PAR with the SMPC are 195.84 W and its efficiency will be 98.08%. As mentioned, the current passing through the additional diodes is 1.04 A, which is very low compared to the load current (20 A), which causes low diode conduction losses (1.45 W) and low current stress (5% of the load current) in the additional diodes of the proposed SMPC. Taking Equations (5)-(7) and Table II into consideration, power losses for the 20PAR, and proposed SMPC are 161.24 W, and 34.6 W, respectively. Therefore, the total losses of the 20PAR with the proposed SMPC can be calculated as 195.84 W and its efficiency is 98.08%. The total power losses of the 20PAR are 161.24 W, including, core losses of 30.92 W, copper losses of 46.85 W, and conduction losses of 83.47 W. The total power losses of the SMPC are 34.6 W, including core losses of 10.65 W, copper losses of 22.5 W, and conduction losses of 1.45 W.

TABLE III
COMPARISON OF PROPOSED 40PAR WITH EXISTING MPARS

	18-Pulse [6]	18-Pulse [32]	20-Pulse [7]	20-Pulse [8]	20-Pulse [35]	24-pulse [16]	36-pulse [11]	44-pulse [12]	48-pulse [37]	72-pulse [27]	40-pulse [24]	40-pulse [25]	40-pulse [26]	Proposed 40PAR with SMPC
THD %	4.36	6.74	3.70	3.04	3.71	3.9	2.82	1.55	3.13	1.68	2.55	2.65	2.22	0.29
Efficiency %	-	98.5	94.43	97.65	97.75	97.26	97.35	96.48	98.3	97.53	97.54	97.50	97.48	98.08
Total kVA rating of the autotransformer (% of load rating)	34.3	34	45.47	40.27	44.48	45.71	43.55	42	31.57	44.33	63.98	48.45	57.26	37.7
No. of Diodes	18	18	20	20	20	16	36	44	30	38	22	22	22	22
Approximate total cost ($)	194.85	193.5	249.6	226.2	245.2	241.69	276.9	288	210	285	382.4	312.5	352.2	219.15

To clarify the characteristics and strengths of the suggested 40PAR, Table III lists a comparison with other MPARs, and similar 40PARs presented in [24-26]. As shown in Table III, the efficiency of the proposed 40PAR is about 98% which is competitive with those of other MPARs. The kVA ratings and cost of the proposed 40PAR are lower than those of the 20PARs [7, 8, 35], 24PAR [16], 36PAR [11], 44PAR [12], and 72PAR [17]. Under the same input/output conditions, the proposed 40 PAR has a smaller volume and lighter weight than other MPARs. Although the kVA rating, and therefore, the cost of the proposed 40PAR is slightly higher than 18PARs [6] and [32] and the 48PAR [37], the input current THD in the proposed rectifier is much lower than these rectifiers. In addition, as mentioned before, 18PARs [6 and 32] are not able to meet the DO-160G requirements without using any input/output filters. Also, the 48PAR [37] has a very complex structure and the number of diodes is very high, which leads to increased conduction losses and diode current stress. In general, the input current THD of the proposed 40PAR is much lower than that of MPARs, which confirms the high ability of the proposed rectifier to meet the requirements of the IEEE standard 519 and DO-160G standards without using any input/output filters. For the aircraft industry, weight is a vital parameter. Using (8), the transformer weight can be estimated [40].

$$W_T = K_w A_P^{0.75} = K_w \left(\frac{S_T}{k_f k_u B_m J f_T}\right)^{0.75}. \quad (8)$$

where, K_w is core configuration constant and f_T represents frequency of operation. The value of K_w is 68.2, if the core type is laminated. Equation (8) calculates the weight of the proposed rectifier, employing the parameters listed in Table II.

As can be seen in Table IV, the power density of the 20PAR along with the proposed SMPC is 0.32 kg/kW, which is less than the other existing solutions. To clarify the characteristics and privileges of the suggested 40PAR, Table IV lists the comparison results with similar 40PARs presented in [24-26]. As listed in Table IV, the input current THD, efficiency, kVA rating, and cost of the suggested 40PAR are lower than those of similar 40PARs. Also, the current stress and conduction losses of the additional auxiliary diodes in the proposed SMPC are much less than those of similar MPCs.

TABLE IV
COMPARISON OF PROPOSED WITH SIMILAR 40PARS (10KW LOAD)

		Unit cost ($)	40PAR [24]	40PAR [25]	40PAR [26]	Proposed 40PAR
% of THD			2.55	2.65	2.22	0.29
% of Efficiency			97.54	97.50	97.48	98.08
Weight (g)			5438	4118	4867	3205
Additional auxiliary diodes	Conduction loss [W]		18.83	18.83	18.83	1.45
	Current stress [A]		20	20	20	1.04
Total kVA rating of the autotransformer (% of load rating)		4.5 times the kVA	63.98	48.45	57.26	37.7
Diode		2.25	22	22	22	22
Approximate total cost ($)			382.4	312.5	352.2	219.15

The suggested 40PAR is more suitable for high current and low voltage applications because of its lower current stress and conduction losses in comparison with that of the 40PARs [24-26]. For the reliability evaluation, the basic failure rate and components coefficients are determined by checking MIL-HDBK-217F similar to [39]. For 40PAR, the mean time between failure (MTBF) determined by part stress analysis and parts count methods is 175131h and 98058h, respectively. Considering that there are some errors in the data sources used in the parameter estimation of the component prediction model in the MIL-HDBK-217F, according to the engineering experience, we set the design margin of MTBF to 1.5 times the target, in order to ensure the accuracy of the reliability prediction. The MTBF of the 40PAR power supply is 98058 / 1.5 = 65372 h > 15000 h, which meets the requirement of an MTBF ≥ 15000 h for the 40PAR power supply system.

VII. CONCLUSION

A new SPMC based on two TIPRs and two additional diodes for upgrading a typical 20PAR to a 40PAR was presented in this paper. Considering low diode conduction losses (1.45 W) and low current stress (5% of the load current) for the additional diodes, the proposed SMPC had high reliability. Also, the proposed SPMC did not require a ZSBT compared to conventional PMCs, leading to simplicity in implementation. The sinusoidal input current was obtained at 50Hz with a THD below 2% under light load and below 1% under full load. The experimental results indicated that when the load changes, the proposed PAR has still good harmonic suppression capacity. The input current THD at 400Hz / 800Hz was less than 1% under full load. As presented in the simulation results, it can be seen that in light load conditions and 50Hz, the current THD has a slight increase but it is less than 2%, which is the privilege of the proposed rectifier. Also, in light load conditions, there is a small increase in losses and its efficiency is 96.5%. In addition, the proposed 40PAR could meet the DO-160G requirements without using any input and output filters. Therefore, this 40PAR can be considered for aviation applications, as a rectifier with sinusoidal input current and low conduction losses, and negligible current stress. The increase in the circuit frequency results in disorder in operation modes and a slight increase in the input current THD. This is the disadvantage of all the passive harmonic reduction circuits and the proposed SPMC as well. The solution to this problem can be considered a subject of future research. However, this increase in the case of the proposed solution is acceptable because it satisfies the requirements of DO-160G.

REFERENCES

[1] IEEE Standard 519-2014, *IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems*. New York, 2014.

[2] M. S. Hamad, M. I. Masoud, K. H. Ahmed and B. W. Williams, "A Shunt Active Power Filter for a Medium-Voltage 12-Pulse Current Source Converter Using Open Loop Control Compensation," *IEEE Trans. Ind. Electron*., vol. 61, no. 11, pp. 5840-5850, Nov. 2014.

[3] X. Li, W. Xu, and T. Ding, "Damped High Passive Filter—A New Filtering Scheme for Multipulse Rectifier Systems," *IEEE Trans. Power Del*., vol. 32, no. 1, pp. 117-124, Feb. 2017.

[4] A. de O. C. Neto, A. L. Soares, G. B. de Lima, D. B. Rodrigues, E. A. A. Coelho, and L. C. G. Freitas, “Optimized 12-Pulse Rectifier with Generalized Delta Connection Autotransformer And Isolated Sepic Converters For Sinusoidal Input Line Current Imposition, ” *IEEE Trans. Power Electron*., vol. 34, no. 4, pp. 3204-3213, April 2019.

[5] B. Singh, G. Bhuvaneswari, and V. Garg, “Harmonic Mitigation Using 12-Pulse AC–DC Converter in Vector-Controlled Induction Motor Drives”, *IEEE Trans. Power Electron*., vol. 21, no. 3, pp. 1483-1492, July 2006.

[6] B. Singh, V. Garg, and G. Bhuvaneswari, “A novel T-connected autotransformer-based 18-pulse AC–DC converter for harmonic mitigation in adjustable-speed induction-motor drives,” *IEEE Trans. Ind. Electron*., vol. 54, no. 5, pp. 2500–2511, Oct. 2007.

[7] R. Kalpana, G. Bhuvaneswari, B. Singh, S. Singh, and S. Gairola, “Autoconnected-transformer-based 20-pulse ac–dc converter for telecommunication power supply,” IEEE Trans. Ind. Electron., vol. 60, no. 10, pp. 4178-4190, Oct. 2013.

[8] S. P. P, R. Kalpana, B. Singh, and G. Bhuvaneswari, "A 20-Pulse Asymmetric Multi-Phase Staggering Autoconfigured Transformer for Power Quality Improvement, ” *IEEE Trans. Power Electron*., vol. 33, no. 2, pp. 917-925, Feb. 2018.

[9] B. Singh, G. Bhuvaneswari, and V. Garg, “T-connected autotransformer-based 24-pulse AC-DC converter for variable frequency induction motor drives,” *IEEE Trans. Energy Conver.*, vol. 21, no. 3, pp. 663-672 Sept. 2006.

[10] Rohollah Abdollahi, “Comparison of power quality indices and apparent power (kVA) ratings in different autotransformer-based 30-pulse AC–DC converters,” *Journal of Applied Research and Technology*, vol. 15, no. 3, pp. 223-232, 2017.

[11] R. Abdollahi, “Design and construction of a polygon-connected autotransformer-based 36-pulse AC-DC converter for power quality improvement in retrofit applications,” *Bulletin of the Polish Academy of Sciences: Technical Sciences*, vol. 63, no. 2, 2015.

[12] R. Abdollahi, “Multi-Phase Shifting Autotransformer Based Rectifier,” *IEEE Open Journal of the Industrial Electronics Society*, vol. 1, pp. 38-45, 2020. DOI: 10.1109/OJIES.2020.2984715, 2020.

[13] B. S. Lee, J. Hahn, P. N. Enjeti, and I. J. Pitel, “A robust three-phase active power-factor-correction and harmonic reduction scheme for high power,” *IEEE Trans. Ind. Electron*., vol. 46, no. 3, pp. 483-494, Jun 1999.

[14] F. Meng, W. Yang, Sh. Yang, and L. Gao, “Active harmonic reduction for 12-pulse diode bridge rectifier at dc side with two-stage auxiliary circuit,” *IEEE Trans. Ind. Inform*., vol. 11, no 1, pp. 64-73, Feb. 2015.

[15] R. Izadinia and H. R. Karshenas, “Current Shaping in a Hybrid 12-Pulse Rectifier Using a Vienna Rectifier,” *IEEE Trans. Power Electron*., vol. 33, no. 2, pp. 1135-1142, Feb. 2018.

[16] F. Meng, X. Xu, L. Gao, “A Simple Harmonic Reduction Method in Multi-Pulse Rectifier Using Passive Devices,” *IEEE Trans. Ind. Inform.*, vol. 13, no. 5, pp. 2680- 2692, Oct. 2017.

[17] S. Yang, J. Wang, and W. Yang, “A Novel 24-Pulse Diode Rectifier with an Auxiliary Single-Phase Full-Wave Rectifier at DC Side,” *IEEE Trans. Power Electron*., vol. 32, no. 3, pp. 1885-1893, March 2017.

[18] R Abdollahi, GB Gharehpetian, A Anvari-Moghaddam, and F Blaabjerg, “An improved 24-pulse rectifier for harmonic mitigation in more electric aircraft,” *IET Power Electron.*, vol. 14, no. 11, pp. 2007-2020, 2021.

[19] F. Meng, Q. Du, L. Wang, L. Gao, and Zh. Man, “A Series-Connected 24-Pulse Rectifier Using Passive Voltage Harmonic Injection Method at DC Link,” *IEEE Trans. Power Electron*., vol. 34, no. 9, pp. 8503-8512, Sept. 2019.

[20] L. Gao, X. Xu, Zh. Man, J. Lee, “A 36-Pulse Diode-Bridge Rectifier Using Dual Passive Harmonic Reduction Methods at DC Link”, *IEEE Trans. Power Electron*., vol. 34, no. 2, pp. 1216-1226, Feb. 2019.

[21] F. Meng, X. Xu, L. Gao, Z. Man, and X. Cai, "Dual Passive Harmonic Reduction at DC Link of the Double-Star Uncontrolled Rectifier,” *IEEE Trans. Ind. Electron*., vol. 66, no. 4, pp. 3303-3309, April 2019.

[22] R. Abdollahi, G. B Gharehpetian, A. Anvari-Moghaddam, and F. Blaabjerg, “Pulse Tripling Circuit and Twelve Pulse Rectifier Combination for Sinusoidal Input Current,” *IEEE Access*, vol. 9, pp. 103588-103599, 2021.

[23] J. Wang, X. Yao, X. Gao, and Sh. Yang, “Harmonic reduction for 12-pulse rectifier using two auxiliary single-phase full-wave rectifiers,” *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12617–12622, Dec. 2020.

[24] R. Abdollahi and G. B. Gharehpetian, “Inclusive Design and Implementation of Novel 40-Pulse AC-DC converter for retrofit application and harmonic mitigation,” *IEEE Trans. Ind. Electron*., vol. 63, no. 2, pp. 667-677, Feb. 2016.

[25] R. Abdollahi, “a Simple Harmonic Reduction Method in 20-Pulse AC-DC Converter,” *Journal of Circuits, Systems, and Computers*, vol. 28, no. 01, pp. 19500132018. DOI: 10.1142/S0218126619500130, 2019.

[26] B. Singh and S. Gairola, “A 40-pulse ac-dc converter fed vector-controlled induction motor drive,” *IEEE Trans. Energy Conver*., vol. 23, no. 2, pp. 403-411, June 2008.

[27] R. Abdollahi, G. B. Gharehpetian, and M. S. Mahdavi, “Cost-effective multi-pulse AC-DC converter with lower than 3% current THD,” *International Journal of Circuit Theory and Applications*, vol. 47, no. 7, pp. 1105-1120, 2019.

[28] R. Abdollahi, “Power quality enhancement of a T-connected autotransformer based on 72-pulse AC–DC converter with rated power reduction,” *Electr. Eng.*, vol. 102, no. 3, pp. 1253-1264, 2020.

[29] T. Clark, F. J. Chivite-Zabalza, A. J. Forsyth, M. Barnes, and D. R. Trainer, “Analysis and comparison of diode rectifier units suitable for aerospace applications,” *2008 4th IET Conference on Power Electronics, Machines and Drives*, 2008, pp. 602-606.

[30] J. Chen, Y. Shen, J. Chen, H. Bai, Ch. Gong, and F. Wang, “Evaluation on the autoconfigured multipulse AC/DC rectifiers and their application in more electric aircrafts,” *IEEE Trans. Transp. Electrif.*, vol. 6, no. 4, pp. 1721–1739, Dec. 2020.

[31] D. A. Paice, *Power Electronic Converter Harmonics: Multipulse Methods for Clean Power*. New York: IEEE Press, 1996.

[32] J. Chen, J. Shen, J. Chen, P. Shen, Q. Song, and Ch. Gong, “Investigation on the Selection and Design of Step-Up/Down 18-Pulse ATRUs for More Electric Aircrafts,” *IEEE Trans. Transp. Electrif.*, vol. 5, no. 3, pp. 795-811, 2019.

[33] RTCA Inc., “Environmental Conditions and Test Procedures for Airborne Equipment - RTCA DO-160”, RTCA Inc. Std. [Online]. Available: http://www.rtca.org.

[34] S. Prakash P, R. Kalpana, and B. Singh, “Inclusive Design and Development of Front-End Multi-Phase Rectifier with Reduced Magnetic Rating and Improved Efficiency,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no 3, pp. 2989-3000, Sep. 2020.

[35] R. Abdollahi and G. B. Gharehpetian, “A 20-pulse autotransformer rectifier unit for more electric aircrafts,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 3, pp. 2992–2999, Jun. 2021.

[36] R. Abdollahi, G. B. Gharehpetian, and M. Davari “A Novel More Electric Aircraft Power System Rectifier Based on a Low-Rating Autotransformer”, *IEEE Trans. Transp. Electrif.*, 2021(Early Access).

[37] J. Chen, H. Bai, J. Chen, and Ch.Gong, “A Novel Parallel Configured 48-Pulse Autotransformer Rectifier for Aviation Application,” *IEEE Trans. Transp. Electrif.*, vol. 37, no. 2, pp. 2125-2138, Feb. 2022.

[38] Q. Du, L. Gao, Q. Li, T. Li, and F. Meng, “Harmonic Reduction Methods at DC Side of Parallel-connected Multi-pulse Rectifiers: A Review,” *IEEE Trans. Power Electron*., vol. 36, no. 3, pp. 2768–2782, March 2021.

[39] R. Abdollahi, G. B. Gharehpetian, “"Suggestion of DC side passive harmonic reduction circuits for industrial applications based on a comparative study,” *IET Power Electron*., vol. 15, no. 6, pp. 531-547, 2022.

[40] Colonel Wm. T. McLyman, “Transformer and Inductor Design Handbook,” Taylor & Francis Group, LCC, 5-7, 2011.

[41] Reliability Prediction of Electronic Equipment, *Standard MIL-HDBK-217F*, Department of Defense USA, 1995.