IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS

Simple Explicit Solution of Finite Control Set Model Predictive Control for Cascaded H-Bridge Inverters

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Abstract—In multilevel converters, finite control set model predictive control (MPC) suffers from high computational costs. This article proposes a simple method to reduce the computational burden by solving the equivalent unconstrained continuous control problem, by constraining the solution, and thus by searching the nearest feasible voltage vector. The proposed technique requires a few simple computations that do not depend on the number of levels. An analysis of the computational complexity of the proposed technique is presented and comparisons with other methodologies are discussed. The proposed technique was implemented on a field programmable gate array (FPGA) and tested on a cascaded H-bridge multilevel static synchronous compensator, evaluating the execution time and verifying the validity of the approach.

Index Terms—Model predictive control (MPC), multilevel converter, static compensator.

I. INTRODUCTION

D URING the last decade, model predictive control (MPC) has become a popular control technique for power converters. The main idea of MPC is to formulate the control problem as an optimization problem and the control action is computed by minimizing the error between the reference and the predicted state variables for different future instants. A dynamical model of the system is employed to compute the predictions and the optimum problem can handle the physical constraints of the system. The continuous control set MPC (CCS-MPC) or modulated MPC (indirect MPC) computes a continuous voltage vector that

Digital Object Identifier 10.1109/TIE.2023.3321979

is modulated to synthesize the switching signals [1], [2]. The finite control set MPC (FCS-MPC or direct MPC), instead, is formulated as a discrete optimization problem by considering the discrete nature of the switches, which can only be turned ON and OFF. The consequence of directly controlling the switching state is a fast dynamic response, which makes a modulation algorithm unnecessary. The most straightforward way to implement the FCS-MPC is to compute predictions of the output variable for every possible switching pattern and compute the related cost to find the best control action. The main disadvantage of this strategy is its large number of computations, which grows exponentially when the converter number of levels increases. Many works can be found in the literature to reduce the computational burden of the FCS-MPC algorithm for cascaded H-bridge (CHB) inverters. A simple approach consists of searching for the optimum input in a subset of all the possible combinations, as in [3], [4], [5], and [6]. For example, the manuscript [3] limits the search set to the vectors that are nearest to the last applied vector, reducing the number of calculations to only seven predictions. It leads to a suboptimal solution, which is effective in the steady state but negatively affects the transient performance.

Other approaches explicitly use the dynamical model of the converter without solving an optimization problem [7], [8].

By contrast, model-free predictive control avoids using a nominal model [9]. It uses past data samples to make predictions of future states, creating a data-driven controller that improves the robustness to parametric variations. However, the optimization problem is addressed by limiting the search space, leading to a suboptimal result.

The sphere decoding algorithm was successfully investigated by the authors in [10], [11], and [12], reducing the number of computations when using multiple prediction horizons, and it is referred to as multistep or long-horizon FCS-MPC. One of the major problems of this algorithm is the choice of the initial radius, which strongly affects the computational load during fast transients. Moreover, the computational improvement relies on the fact that the search space is limited to the vectors adjacent to the previous control input, implying a suboptimal solution.

Despite the improvements when using multiple prediction horizons in motor drives [13], [14], many applications employ the FCS-MPC formulation with one prediction horizon. In grid-tied inverters, for instance, the iterative predictions of the output variable would rely on the prediction of the grid voltage,

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Manuscript received 27 April 2023; revised 24 August 2023 and 25 September 2023; accepted 28 September 2023. This work was supported in part by NEST, - PNRR MUR – M4C2 - I 1.3 under grant D93C22000900001, in part by the DigiPower Ltd., L'Aquila, Italy, under Grant "HORIZON 2020," and in part by the PON I&C2014-2020, under Grant F/050220/X32 CUP B18I15000100008. (Corresponding author: Francesco Simonetti.)

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TIE.2023.3321979.



Fig. 1. CHB inverter.

which is generally not feasible and leads to inaccuracy. The authors in [15], [16], and [17] applied FCS-MPC to a CHB static synchronous compensator (CHB-STATCOM), dividing the overall optimization problem into subproblems, strongly reducing the total computational burden. Zhang et al. [15] individually compute the currents and voltages optimization subproblems, reducing the computational burden from exponential to polynomial level. Zhang et al. [18] further improved the current optimization, proposing an algorithm with linear complexity. The authors in [19], [20], [21], and [22] proposed machine learning techniques to speed up the online implementation of the control. However, the obtained control low is a suboptimal solution.

In this work, an algorithm for finding the global optimal solution of the current control problem of FCS-MPC is presented. The main contribution of this approach is that it allows computing the optimal switching vector with a few simple mathematical operations regardless of the number of levels, thus overcoming the existing methodologies.

II. CHB INVERTER MODEL

Fig. 1 shows the schematic diagram of the considered CHB inverter connected to a general RL load and a three-phase voltage source. Depending on the application, this schematic can represent a grid-tied inverter connected to the grid through a filter inductor with its internal resistance, such as an inverter connected to a motor, where the voltage sources represent the electromotive forces [23].

The discretized dynamic equations of the currents, in $\alpha\beta$ coordinates, are as follows:

$$\mathbf{i}_{\alpha,\beta} \left(k+1\right) = \begin{bmatrix} 1 - \frac{T_s}{L}R & 0\\ 0 & 1 - \frac{T_s}{L}R \end{bmatrix} \mathbf{i}_{\alpha,\beta}(k) + \begin{bmatrix} \frac{T_s}{L} & 0\\ 0 & \frac{T_s}{L} \end{bmatrix} \left(\mathbf{v}_{s(\alpha,\beta)}(k) - \mathbf{v}_{\alpha,\beta}(k)\right) \quad (1)$$

where $\mathbf{i}_{\alpha,\beta}$ is the current vector, $\mathbf{v}_{s(\alpha,\beta)}$ is the voltage source vector, $\mathbf{v}_{\alpha,\beta}$ is the voltage vector at the inverter terminals, Rand L are resistance and inductance of the load, considered balanced, and T_s is the sampling period. The inverter voltage can be expressed as $\mathbf{v}_{\alpha,\beta}(k) = \mathbf{S}_{\alpha,\beta}(k)V_{dc}$, where V_{dc} is the nominal dc-link voltage of each H-bridge and $\mathbf{S}_{\alpha,\beta}(k)$ is the switching vector at the time k, which is a discrete variable corresponding to the control input applied to the inverter. Equation (1) can be formulated as follows:

$$\mathbf{i}_{\alpha,\beta}(k+1) = \mathbf{A} \, \mathbf{i}_{\alpha,\beta}(k) + \mathbf{B} \, \mathbf{S}_{\alpha,\beta}(k) + \mathbf{F} \, \mathbf{v}_{s(\alpha,\beta)}(k) \quad (2)$$

where

$$\begin{split} \mathbf{A} &= \begin{bmatrix} 1 - \frac{T_s}{L}R & 0\\ 0 & 1 - \frac{T_s}{L}R \end{bmatrix} \\ \mathbf{B} &= \begin{bmatrix} -\frac{T_s}{L} & 0\\ 0 & -\frac{T_s}{L} \end{bmatrix} V_{\mathrm{dc}} \qquad \mathbf{F} = \begin{bmatrix} \frac{T_s}{L} & 0\\ 0 & \frac{T_s}{L} \end{bmatrix}. \end{split}$$

III. PROPOSED METHOD

The MPC problem is expressed as follows:

$$\min_{\mathbf{S}_{\alpha,\beta}(k+1)} \left\| \mathbf{i}_{\alpha,\beta}^{ref}(k+2) - \mathbf{i}_{\alpha,\beta}(k+2) \right\|_{\mathbf{Q}} + \\
+ \left\| \mathbf{S}_{\alpha,\beta}(k+1) - \mathbf{S}_{\alpha,\beta}(k) \right\|_{\mathbf{P}}$$
s.t. equations(2)

$$\mathbf{S}_{\alpha,\beta}(k+1) \in \mathbf{V}_{\alpha,\beta} \tag{3}$$

where **Q** and **P** are two weighting matrices and $\mathbf{i}_{\alpha,\beta}^{\text{ref}}(k+2)$ is the predicted reference value. The optimal switching vector must belong to $\mathbf{V}_{\alpha,\beta}$, the set of all the vectors that the inverter can physically generate. In order to compute the control at time k + 1, the currents at time k + 2 must be computed. Iterating (2), the following formulation is obtained:

$$\mathbf{i}_{\alpha,\beta} \left(k+2 \right) = \mathbf{A} \, \mathbf{i}_{\alpha,\beta} \left(\mathbf{k}+1 \right) + \mathbf{B} \, \mathbf{S}_{\alpha,\beta} \left(\mathbf{k}+1 \right)$$
$$+ \mathbf{F} \, \mathbf{v}_{s(\alpha,\beta)} \left(k+1 \right)$$
$$= \mathbf{A}^2 \, \mathbf{i}_{\alpha,\beta}(k) + \mathbf{A} \mathbf{B} \, \mathbf{S}_{\alpha,\beta}(k) + \mathbf{A} \mathbf{F} \, \mathbf{v}_{s(\alpha,\beta)}(k)$$
$$+ \mathbf{B} \, \mathbf{S}_{\alpha,\beta} \left(k+1 \right) + \mathbf{F} \, \mathbf{v}_{s(\alpha,\beta)} \left(k+1 \right)$$
(4)

with two unknowns: the control input at next time $S_{\alpha,\beta}(k+1)$, which is the variable to be computed, and the grid voltage at next time $\mathbf{v}_{s(\alpha,\beta)}(k+1)$, which must be predicted. It is reasonable to approximate the grid voltage at time k+1 as the voltage at time k rotated by one step at line frequency ω , i.e.,

$$\mathbf{r}_{s(\alpha,\beta)} (k+1) = \mathbf{T} \mathbf{v}_{s(\alpha,\beta)}(k),$$
$$\mathbf{T} = \begin{bmatrix} \cos(\omega T_s) & -\sin(\omega T_s) \\ \sin(\omega T_s) & \cos(\omega T_s) \end{bmatrix}.$$

v

With this assumption, the currents at time k + 2 are given as follows:

$$\mathbf{i}_{\alpha,\beta} (k+2) = \mathbf{A}^2 \mathbf{i}_{\alpha,\beta}(k) + \mathbf{AB} \mathbf{S}_{\alpha,\beta}(k) + (\mathbf{AF} + \mathbf{FT})$$

$$\times \mathbf{v}_{s(\alpha,\beta)}(k) + \mathbf{B} \, \mathbf{S}_{\alpha,\beta}(k+1)$$

= $\mathbf{A}^2 \, \mathbf{i}_{\alpha,\beta}(k) + \mathbf{E} \, \mathbf{S}_{\alpha,\beta}(k) + \mathbf{G} \, \mathbf{v}_{s(\alpha,\beta)}(k)$
+ $\mathbf{B} \, \mathbf{S}_{\alpha,\beta}(k+1)$. (5)

The current reference at time k + 2 can be predicted by $\mathbf{i}_{\alpha,\beta}^{\text{ref}}$ $(k+2) = \mathbf{T}^2 \mathbf{i}_{\alpha,\beta}^{\text{ref}}(k).$

The proposed method aims to solve the discrete optimization problem in (3) solving, at first, the equivalent continuous problem; then, the discrete solution is found based on the continuous solution. Assuming the variables to be continuous, the problem in (3) becomes a quadratic programming problem since there is a quadratic cost function and the optimization variables must belong to a hexagonal space vector, which is defined by linear inequalities. This problem can be solved using standard quadratic programming. However, since several iterations could be needed, a simple way to solve this quadratic and constrained problem is proposed.

The overall problem is divided into three distinct steps. First, the equivalent continuous unconstrained problem is solved. Then, the unconstrained solution is projected into the space vector to find the continuous constrained solution. Finally, the discrete optimum solution is found based on the continuous constrained solution.

A. Continuous Unconstrained Problem

Let us call $S_{\alpha,\beta}^{c}$ the continuous unconstrained optimum switching vector. The minimum problem of the MPC in (3) becomes as follows:

$$\mathbf{S}_{\alpha,\beta}^{c} = \min_{S_{\alpha,\beta}} \left(\mathbf{i}_{\alpha,\beta}^{\text{ref}} \left(k+2 \right) - \mathbf{i}_{\alpha,\beta} \left(k+2 \right) \right)^{T} \mathbf{Q}$$
$$\times \left(\mathbf{i}_{\alpha,\beta}^{\text{ref}} \left(k+2 \right) - \mathbf{i}_{\alpha,\beta} \left(k+2 \right) \right)$$
$$+ \left(\mathbf{S}_{\alpha,\beta} - \mathbf{S}_{\alpha,\beta} (k) \right)^{T} \mathbf{P} \left(\mathbf{S}_{\alpha,\beta} - \mathbf{S}_{\alpha,\beta} (k) \right)$$
(6)

where $\mathbf{S}_{\alpha,\beta}$ is the optimization variable and $\mathbf{i}_{\alpha,\beta}(k+2)$ is predicted by using (5). The solution of (6) is simply given by computing the derivative of the cost function with respect to $\mathbf{S}_{\alpha,\beta}$, and setting it to zero. In this discussion, the calculation of the derivative is omitted and just the result is given, that is as follows:

$$\mathbf{S}_{\alpha,\beta}^{c} = \left[\mathbf{B}^{T}\mathbf{Q} \mathbf{B} + \mathbf{P}\right]^{-1} \left[-\mathbf{B}^{T}\mathbf{Q} \mathbf{A}^{2} \mathbf{i}_{\alpha,\beta}(k) - \left(\mathbf{E}^{T}\mathbf{Q} \mathbf{B} + \mathbf{P}\right) \mathbf{S}_{\alpha,\beta}(k) - \mathbf{B}^{T}\mathbf{Q} \mathbf{G} \mathbf{v}_{s(\alpha,\beta)}(k) + \mathbf{B}^{T}\mathbf{Q}\mathbf{T}^{2} \mathbf{i}_{\alpha,\beta}^{ref}(k)\right].$$
(7)

B. Continuous Constrained Problem

Once the optimal continuous unconstrained solution is computed, it is needed to compute $\mathbf{S}_{\alpha,\beta}^{\text{proj}}$, i.e., the projection of $\mathbf{S}_{\alpha,\beta}^{c}$ into the hexagonal space of feasible solutions. The hexagonal space is a polytope described by six inequalities. Given *n* Hbridges per phase, the vertices of the polytope, by construction,



Fig. 2. Space vector with constraints for a n=10 CHB inverter.

are as follows:

$$\mathbf{V} = \left\{ \begin{pmatrix} \frac{4}{3} \\ 0 \end{pmatrix}, \begin{pmatrix} \frac{2}{3} \\ -\frac{2}{\sqrt{(3)}} \end{pmatrix}, \begin{pmatrix} -\frac{2}{3} \\ -\frac{2}{\sqrt{(3)}} \end{pmatrix}, \begin{pmatrix} -\frac{4}{3} \\ 0 \end{pmatrix}, \begin{pmatrix} -\frac{4}{3} \\ 0 \end{pmatrix}, \begin{pmatrix} -\frac{2}{3} \\ 0 \end{pmatrix}, \begin{pmatrix} \frac{2}{3} \\ \frac{2}{\sqrt{(3)}} \end{pmatrix}, \begin{pmatrix} \frac{2}{3} \\ \frac{2}{\sqrt{(3)}} \end{pmatrix} \right\} \cdot n.$$
(8)

By simply computing the equations of the lines passing through two consecutive vertices, it is possible to obtain the constraints of the hexagon, shown in Fig. 2. Given $\overline{m} = \sqrt{3}$ and $\overline{q} = 4n/\sqrt{3}$, the constraints are as follows:

$constraint 1: S_{\beta} \leq -\overline{m}S_{\alpha} + \overline{q}$	$constraint 2: S_{\beta} \ge \overline{m} S_{\alpha} - \overline{q}$
$constraint 3 \colon S_{\beta} \! \ge \! -\overline{m}S_{\alpha} \! - \! \overline{q}$	$constraint 4 \colon S_{\beta} \! \leq \! \overline{m}S_{\alpha} \! + \! \overline{q}$
$constraint 5: S_\beta \!\leq\! 2n/\sqrt{3}$	$constraint 6: S_{\beta} \ge -2n/\sqrt{3}$
	(9)

where S_{α} and S_{β} are continuous points on the α and β axes, respectively. If one of these inequalities is not satisfied for the computed solution $\mathbf{S}_{\alpha,\beta}^c$, it is necessary to identify in which region outside the hexagon the point lays. Once the region is determined, the constrained solution is computed by projecting the point on the violated constraint, i.e., computing the point on the violated constraint. Let us refer to the violated constraint as $S_{\beta} = mS_{\alpha} + q$, with m and q as in (9). This problem can be expressed as follows:

$$\mathbf{S}_{\alpha,\beta}^{\text{proj}} = \min_{\mathbf{S}_{\alpha,\beta}} \left(\mathbf{S}_{\alpha,\beta} - \mathbf{S}_{\alpha,\beta}^{c} \right)^{T} \left(\mathbf{B}^{T} \mathbf{Q} \mathbf{B} + \mathbf{P} \right) \left(\mathbf{S}_{\alpha,\beta} - \mathbf{S}_{\alpha,\beta}^{c} \right)$$

s.t. $S_{\beta} = mS_{\alpha} + q$
$$= \min_{S_{\alpha},S_{\beta}} \left(\begin{bmatrix} S_{\alpha} \\ S_{\beta} \end{bmatrix} - \begin{bmatrix} S_{\alpha}^{c} \\ S_{\beta}^{c} \end{bmatrix} \right)^{T} \begin{bmatrix} w_{11} & w_{12} \\ w_{21} & w_{22} \end{bmatrix} \left(\begin{bmatrix} S_{\alpha} \\ S_{\beta} \end{bmatrix} - \begin{bmatrix} S_{\alpha}^{c} \\ S_{\beta}^{c} \end{bmatrix} \right)$$

s.t. $S_{\beta} = mS_{\alpha} + q$ (10)

where the matrix $(\mathbf{B}^T \mathbf{Q} \mathbf{B} + \mathbf{P})$ is the quadratic term of the cost function. In general, it does not make sense to weigh the α coordinate differently from the β coordinate, and \mathbf{Q} and \mathbf{P} are diagonal matrices. Consequently, $w_{11} = w_{22}$ and $w_{12} = w_{21} = 0$, so the level curves of the cost function are circles and it is possible to find the projection by simply applying the point-to-line projection formula. Indeed, with these assumptions, (10) becomes

$$\mathbf{S}_{\alpha,\beta}^{\text{proj}} = \min_{S_{\alpha},S_{\beta}} \quad (S_{\alpha} - S_{\alpha}^{c})^{2} + (S_{\beta} - S_{\beta}^{c})^{2}$$

s.t. $S_{\beta} = mS_{\alpha} + q$ (11)

which leads to

$$S_{\alpha}^{\text{proj}} = \min_{S_{\alpha}} \quad (S_{\alpha} - S_{\alpha}^{c})^{2} + \left(mS_{\alpha} + q - S_{\beta}^{c}\right)^{2}.$$
(12)

The solution S_{α}^{proj} is simply computed by setting the derivative with respect to S_{α} to zero

$$S_{\alpha}^{\text{proj}} = \left(S_{\alpha}^{c} + m\left(S_{\beta}^{c} - q\right)\right) / \left(1 + m^{2}\right)$$
$$S_{\beta}^{\text{proj}} = mS_{\alpha} + q.$$
(13)

If the violated constraints are two, the projection is one of the vertices of the hexagon. The constraints that determine the regions are computed by substituting S^c_{α} and S^c_{β} with the vertices in (8) in the projection formulas in (13), in this way, the separation lines between the regions are found.

The constraints of the regions are the following, where $\hat{m} = -1/\overline{m}$ and $\hat{q} = \overline{q}/3$:

 $\begin{aligned} & constraint \ 7: \ S_{\beta} \ge -\hat{m}S_{\alpha} + \hat{q} \quad constraint \ 8: \ S_{\beta} \le -\hat{m}S_{\alpha} - \hat{q} \\ & constraint \ 9: \ S_{\beta} \ge \hat{m}S_{\alpha} + \hat{q} \quad constraint \ 10: \ S_{\beta} \le \hat{m}S_{\alpha} - \hat{q} \\ & constraint \ 11: \ S_{\alpha} \le -2n/\sqrt{3} \quad constraint \ 12: \ S_{\alpha} \ge 2n/\sqrt{3}. \end{aligned}$ (14)

Fig. 3 shows the different regions outside the hexagonal space vector and underlines the constraints of the regions. The set $\mathbf{V}_{\alpha,\beta}$ of feasible points is computed by transforming in the α, β frame all the a, b, c switching vectors that the inverter can output. The figure also shows an example of a generic unconstrained solution $\mathbf{S}_{\alpha,\beta}^c$ that lays outside the polytope. As evident, the level curves of the quadratic cost function are circles and the optimal constrained solution is the point related to the lower level curve, i.e., the projection $\mathbf{S}_{\alpha,\beta}^{\text{proj}}$ of the point into the hexagon. Table I summarizes the projection rule. In the first column, the regions are listed and in the second one, the constraints that define the regions are shown where not(*) means that the constraint is violated. The last column is related to the projection rule of the



Fig. 3. Space vector with level curves for a n=10 CHB-inverter.

TABLE I PROJECTION RULE

	Constraint evaluation	Projection rule
Region 1	not(1-7-8)	eq. (13): $m = \overline{m}, q = \overline{q}$
Region 2	8 - 9	$\mathbf{S}^{\mathrm{proj}}_{lpha,eta} = \mathbf{V}_1$
Region 3	not(2-9-10)	eq. (13): $m = \overline{m}, q = -\overline{q}$
Region 4	10 - 11	$\mathbf{S}^{ ext{proj}}_{lpha,eta} = \mathbf{V}_2$
Region 5	not(6 - 11 - 12)	$\mathbf{S}^{ ext{proj}}_{lpha,eta}~=\left(S^c_lpha;-rac{2}{\sqrt{(3)}}n ight)$
Region 6	8 - 11	$\mathbf{S}^{ ext{proj}}_{lpha,eta} = \mathbf{V}_3$
Region 7	not(3-7-8)	eq. (13): $m = -\overline{m}, q = \overline{q}$
Region 8	7 - 10	$\mathbf{S}^{\mathrm{proj}}_{lpha,eta} = \mathbf{V}_4$
Region 9	not(4-9-10)	eq. (13): $m = -\overline{m}, q = -\overline{q}$
Region 10	9 - 11	$\mathbf{S}^{ extsf{proj}}_{lpha,eta_{ extsf{b}}} = \mathbf{V}_{5}$
Region 11	not(5 - 11 - 12)	$\mathbf{S}^{ extsf{proj}}_{lpha,eta} \;= \left(S^c_lpha;rac{2}{\sqrt{(3)}}n ight)$
Region 12	7 - 12	$\mathbf{S}^{\mathrm{proj}}_{lpha,eta}=\mathbf{V}_{6}$

different regions: the solution can be a projection on an edge or a vertex of the hexagon.

C. Discrete Problem

Due to the quadratic cost function, the optimal point must be one of the feasible points close to the continuous constrained solution $\mathbf{S}_{\alpha,\beta}^{\text{proj}}$. Since the searched point lies on a plane, the candidate points are four. To simplify the computations, the possible points $\mathbf{S}_{\alpha,\beta}$ are scaled as follows:

$$\tilde{\mathbf{S}}_{\alpha,\beta} = \begin{bmatrix} 3 & 0\\ 0 & \sqrt{3} \end{bmatrix} \mathbf{S}_{\alpha,\beta} = \mathbf{H} \mathbf{S}_{\alpha\beta}.$$
 (15)

Thanks to this scaling, the feasible points are equidistant and have integer values. The quadratic part of the cost function, with the previous assumptions, is given as follows:

$$\mathbf{S}_{\alpha,\beta}^{T}\left(\!\mathbf{B}^{T}\mathbf{Q}\,\mathbf{B}\!+\!\mathbf{P}\!\right)\mathbf{S}_{\alpha,\beta}=\tilde{\mathbf{S}}_{\alpha,\beta}^{T}\mathbf{H}^{-1}\left(\mathbf{B}^{T}\mathbf{Q}\,\mathbf{B}\!+\!\mathbf{P}\right)\mathbf{H}^{-1}\tilde{\mathbf{S}}_{\alpha,\beta}$$



Fig. 4. Feasible points inside the space vector.

$$= \tilde{\mathbf{S}}_{\alpha,\beta}^{T} \begin{bmatrix} \frac{1}{3} & 0\\ 0 & \frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} w_{11} & 0\\ & \\ 0 & w_{11} \end{bmatrix} \begin{bmatrix} \frac{1}{3} & 0\\ 0 & \frac{1}{\sqrt{3}} \end{bmatrix} \tilde{\mathbf{S}}_{\alpha,\beta}$$
$$= \tilde{\mathbf{S}}_{\alpha,\beta}^{T} \begin{bmatrix} \frac{w_{11}}{9} & 0\\ 0 & \frac{w_{11}}{3} \end{bmatrix} \tilde{\mathbf{S}}_{\alpha,\beta} = \tilde{\mathbf{S}}_{\alpha,\beta}^{T} \tilde{\mathbf{W}} \tilde{\mathbf{S}}_{\alpha,\beta} \qquad (16)$$

where in these new variables, $\tilde{\mathbf{W}}$ weights differently in α and β directions and the relative level curves are ellipses. Since W is a diagonal matrix, the axis of the ellipses are aligned with α and β axes and, if all the integer values would be feasible points, it would be sufficient to round the continuous solution $\mathbf{S}_{\alpha,\beta}^c$ to obtain the optimal point. However, only two of the four points around $\tilde{\mathbf{S}}_{\alpha}^{c}$ are feasible by construction. Once the rounded point is computed, it is necessary to verify if it is a feasible point. If it is not, the two feasible points around the continuous solution are evaluated. The distances between them and the continuous solution, weighted by $\hat{\mathbf{W}}$, are computed and the closest one is the solution of the discrete optimization. Fig. 4 shows an example of a continuous solution with the four points around it. The rounded solution, in the example, is not a feasible point and, as underlined by the level curves, the optimum point is (-26;0). The flow chart in Fig. 5 summarizes the overall procedure.

IV. COMPUTATIONAL ANALYSIS OF THE PROPOSED ALGORITHM

The first part of the algorithm in Section III-A requires the computation of (7), which can be expressed as follows:

$$\mathbf{S}_{\alpha,\beta}^{c} = \mathbf{U}_{0} \, \mathbf{i}_{\alpha,\beta}^{ref}(k) + \mathbf{U}_{1} \, \mathbf{i}_{\alpha,\beta}(k) + \mathbf{U}_{2} \, \mathbf{S}(k) + \mathbf{U}_{3} \, \mathbf{v}_{s(\alpha,\beta)}(k)$$
(17)

where, unnumberd shown bottom of the next page. are 2×2 matrices computed offline. The online computations are the



Fig. 5. Optimization algorithm flow chart.

sum of four 2×2 matrices times 2×1 vectors. The total computations are 16 multiplications and 14 sums.

In order to compute the constrained solution in Section III-B, the constraints in (9) must be evaluated, which requires four multiplications, four sums, and six inequality operators. If one of them is violated, the projection must be computed and one if-than-else is needed. In order to identify the region outside the hexagon, the evaluation of constraints in (14) requires four multiplications, four sums, and six inequality operators. The projection rule in Table I requires 12 comparisons and the most involved projection rule is in (13), which requires six online multiplications, 14 sums, and 13 comparisons.

In the discretization of the continuous solution in Section III-C, the scaling operation in (15), and the subsequent inverse scaling to compute $\tilde{\mathbf{S}}_{\alpha,\beta}^{\text{proj}}$ and $\mathbf{S}_{\alpha,\beta}^{*}$ in the flow chart in Fig. 5 requires four multiplications. The odd/ $\overline{\text{even}}_{\alpha,\beta}$ in Fig. 5 is obtained by taking the first bit of \tilde{S}_{α}^{r} and \tilde{S}_{β}^{r} , which is the mod₂(*) operator. To compute the vector $\tilde{\mathbf{S}}_{\alpha,\beta}^{r}$, the round(*) operator is needed. The dir_{α,β} in Fig. 5 is the vector containing

6

IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS

 TABLE II

 COMPUTATIONAL ANALYSIS OF THE ALGORITHM.

III-A	III-B	III-C	Overall procedure
14	14	10	38
16	14	12	42
0	0	6	6
0	13	2	15
0	0	2	2
	III-A 14 16 0 0 0	III-A III-B 14 14 16 14 0 0 0 13 0 0	III-A III-B III-C 14 14 10 16 14 12 0 0 6 0 13 2 0 0 2

TABLE III COMPUTATIONAL BURDEN OF DIFFERENT APPROACHES

	Fast MPC [15]	B and B Approach [18]	Explicit Solution
Sums	$12n^2 + 50n + 16$	16n + 13	38
Multiplications	48n + 18	22n + 27	42
Comparisons	$12n^2 + 10n + 2$	10n + 2	15
Rounds	0	2n + 1	2
Divisions	0	1	0

the sign bits of the result of two subtractions. Computing the feasible solutions $\tilde{\mathbf{S}}_{\alpha,\beta}^{f1}$ and $\tilde{\mathbf{S}}_{\alpha,\beta}^{f2}$ requires two sums, whereas the two distance operators d(*) require four subtractions, eight multiplications, and two sums. The total operations are 12 multiplications, four sums, six subtractions (or six two's complement calculations and six sums), two rounding, and two comparisons.

Table II summarizes the basic operations needed by the overall procedure. In order to emphasize the computational advantages of the proposed technique, a comparison with two other methodologies is presented. Table III depicts the number of elementary operations for the proposed approach compared with "Fast MPC" in [15] and "B and B Approach" in [18]. The "Fast MPC" algorithm reduces the computational burden from exponential to quadratic level. The "B and B Approach" leads to an algorithm of linear complexity with respect to n, overcoming the previous one. Finally, the proposed approach consists of less computations for every n > 1 and the number of operations is constant irrespective of n, further overcoming the other methodologies.

V. EXPERIMENTAL RESULTS FOR A FIVE-LEVEL CHB-STATCOM

In order to evaluate the time spent by the overall control technique and to test the validity of the proposed strategy, an experimental validation was carried out using a five-level CHB STATCOM built by DigiPower Ltd [24]. Since the prediction of the grid voltage can cause inaccuracy and deterioration of the controller performance, the STATCOM MPC is commonly formulated with one prediction horizon. The control scheme comprises a reference generator for the reference direct current able to balance the overall capacitor voltage.

A. CHB-STATCOM Control Scheme

A PI regulator is employed to compute the reference direct current i_d^{ref} capable of stabilizing the average dc-link voltage \overline{v}_C to the nominal value $\overline{v}_C^{\text{ref}}$. The MPC scheme follows the well-known partially stratified approach where the currents controller (CC) is followed by the voltages balancing controller, as in [15], [18], and [25]. The reference currents are transformed into α and β frame, and the CC is computed as in Section III. The dc-link capacitor voltage dynamics is

$$v_{Cpi}(k+1) = v_{Cpi}(k) + \frac{T_s}{C} (s_{pi}(k) \cdot i_p(k))$$

$$i = 1, \dots, n, \quad p = \{a, b, c\}$$
(18)

where v_{Cpi} is the voltage on the *i*thcapacitor of phase p and $s_{pi} = \{-1, 0, 1\}$ is the related switching signal. The optimum vector $\mathbf{S}^*_{\alpha,\beta}$, computed by the CC, is transformed into $\mathbf{S}^*_{a,b,c}$ in a, b, c coordinates. Then, the voltage controller computes the switching signals in order to balance the dc-link capacitor voltages by solving the following optimization problem:

$$\min_{\mathbf{s}_{p}(k)} \left\| \overline{\mathbf{v}_{C}}^{\text{ref}} - \mathbf{v}_{Cp} \left(k+1 \right) \right\|_{\mathbf{Q}_{v}} + \\
+ \left\| \mathbf{s}_{p}(k) - \mathbf{s}_{p} \left(k-1 \right) \right\|_{\mathbf{P}_{v}} \\
\text{s.t.} \quad (18) \\
\sum_{i=1}^{n} s_{pi}(k) = S_{p}^{*}(k) \\
s_{pl} \times s_{pm} \ge 0 \quad \forall \ l, m = 1, \dots, n : l \neq m \quad (19)$$

where $\overline{\mathbf{v}_C}^{\text{ref}} = [\overline{v_C}^{\text{ref}}; \ldots; \overline{v_C}^{\text{ref}}]$ is the $n \times 1$ vector of the reference voltage, $\mathbf{v}_{Cp} = [v_{Cp1}; \ldots; v_{Cpn}]$ is the dc-link voltage vector, and $\mathbf{s}_p = [s_{p1}; \ldots; s_{pn}]$ is the vector of the individual switching signals of phase p. The voltages balancing problem can be solved by employing the algorithms in [15], [18], and [25]. Fig. 6 shows the diagram of the overall control scheme.

B. Experimental Setup

The experimental system in Fig. 7 is composed of two series-connected H-bridges per phase supplied by C = 0.9 mF dc-link capacitors. The three-phase system is connected to the grid through a 230/80 V isolation transformer and an L = 0.6 mH inductor. Table IV summarizes the main parameters of the hardware components and the controller. A master–slave converter architecture comprises a main control board with a 50 MHz Intel Cyclone V 5CEBA7F31C8 field programmable gate array (FPGA), one external I/O board capable of acquiring the grid voltage measurements, and six H-bridges with local signal conditioning circuits, used to sample the dc input voltages

$$\mathbf{U}_{0} = \begin{bmatrix} \mathbf{B}^{T} \mathbf{Q} \mathbf{B} + \mathbf{P} \end{bmatrix}^{-1} \mathbf{B}^{T} \mathbf{Q} \mathbf{T}^{2} \qquad \mathbf{U}_{1} = -\begin{bmatrix} \mathbf{B}^{T} \mathbf{Q} \mathbf{B} + \mathbf{P} \end{bmatrix}^{-1} \mathbf{B}^{T} \mathbf{Q} \mathbf{A}^{2}$$
$$\mathbf{U}_{2} = -\begin{bmatrix} \mathbf{B}^{T} \mathbf{Q} \mathbf{B} + \mathbf{P} \end{bmatrix}^{-1} (\mathbf{E}^{T} \mathbf{Q} \mathbf{B} + \mathbf{P}) \qquad \mathbf{U}_{3} = -\begin{bmatrix} \mathbf{B}^{T} \mathbf{Q} \mathbf{B} + \mathbf{P} \end{bmatrix}^{-1} \mathbf{B}^{T} \mathbf{Q} \mathbf{G}$$



Fig. 6. Control scheme of MPC for CHB-STATCOM.



Fig. 7. Five-level CHB STATCOM experimental setup.

TABLE IV
PARAMETERS OF THE FIVE-LEVEL CHB-STATCOM

	Value		Value
PCC voltage RMS	80 V	Capacitor C	0.9 mF
Grid frequency	50 Hz	Inductance L	6 mH
Rated power	$\pm 2 \text{ kVAR}$	Sampling time T_s	50 μ s
H-bridges per phase n	2	Inductor resistance R	$0.5 \ \Omega$
dc-link voltage	80 V	Peak current reference	6 A

and the output currents. Each H-bridge equips a Texas Instrument TMS320 F28377SPTPT digital signal processor (DSP) responsible for acquiring the measurements and sending them to the master FPGA. Fig. 8 shows the schematic diagram of the experimental system. At the beginning of each sampling interval, the FPGA applies the switching signals computed during the



Fig. 8. Block diagram of the experimental setup.

TABLE V TIME AND SPACE UTILIZATION FPGA IMPLEMENTATION

	SPI	PLL	PI i_d^{ref}	CC	VB
Time spent $[\mu s]$	7.74	1.64	0.52	0.94	0.58
ALMs needed	1178	5620	55.4	2860	2051
Combinational ALUTs	2139	6525	78	4202	3252
Dedicated Logic Registers	1918	918	269	3430	2088
DSP blocks	0	3	0	24	36

previous interval. Then, it starts an serial peripheral interface (SPI) communication process with the seven peripheral slaves to sample the three-phase grid voltage, the dc-link capacitors voltages, and the current flowing through the H-bridges, i.e., the three-phase current exchanged to the grid. Once the data are sampled, the FPGA starts the computation of the overall optimization algorithm and computes the optimal switching signals to be sent to the insulated-gate bipolar transistors (IGBTs) at the start of the next sampling interval. Table V summarizes the time and the resource utilization of the different parts of the implementation, i.e., SPI transmission, phase locked loop (PLL), PI of the reference direct current, CC, and voltages balance (VB).



Fig. 9. CHB-STATCOM inductive mode. (a) Steady-state v_{Ca1} , v_{Cb1} , v_{Cc1} , and $i_{a,b,c}$ inductive mode. (b) Steady-state v_{Ca1} , v_{Ca2} , v_{Cb1} , v_{Cc2} , and $i_{a,b,c}$ inductive mode. (c) Step response grid voltages and output currents inductive mode. (d) Steady-state grid voltages and output currents inductive mode.



Fig. 10. Steady-state output voltages and currents.

C. Control Performance

1) Inductive Mode CHB-STATCOM: Fig. 9(a) shows the steady-state currents for a 4A inductive current and the relative voltages on capacitors of different phases, i.e., v_{Ca1}, v_{Cb1} , and v_{Cc1} . Fig. 9(b) shows the steady-state currents and the dc-link voltages on the same phases, i.e., $v_{Ca1}, v_{Ca2}, v_{Cb1}$, and v_{Cb2} . The two figures demonstrate good current reference tracking performance and voltage balancing performance between capacitors on the same phase and between the dc-link of the different phases. Finally, Fig. 9(c) shows the step response for the 4 A inductive current reference, whereas Fig. 9(d) underlines the phase shift between grid voltage and currents in the steady-state inductive mode. Fig. 10 shows the

 TABLE VI

 HARMONIC COMPONENTS FOR 4 A RMS 50 Hz CURRENT

	dc	$50~\mathrm{Hz}$	100 Hz	150 Hz	200 Hz	$250~\mathrm{Hz}$
Inductive [A]	0.086	5.77	0.014	0.011	0.008	0.042
Capacitive [A]	0.108	5.88	0.010	0.017	0.013	0.006
						_
	300 Hz	350 Hz	400 Hz	$450~\mathrm{Hz}$	500 Hz	
Inductive [A]	0.014	0.021	0.022	0.009	0.006	_
Capacitive [A]	0.028	0.023	0.037	0.029	0.038	

five-level three-phase CHB-STATCOM output voltage and currents when injecting +2 kVAR into the grid.

2) Capacitive Mode CHB-STATCOM: Similarly, the system was tested for the rated current in capacitive mode. Fig. 11(a) shows the output current underlying the dc-link balancing between the three phases. Fig. 11(b) highlights the balancing of the different dc-link capacitors in the same phase. Fig. 11(c) and (d) shows the step response and steady-state performance of the system when absorbing 2 kVAR from the grid. Table VI summarizes the harmonic components of the output current for both inductive and capacitive modes when following a 4 A rms current reference.

D. Robustness

The robustness of the proposed controller was studied by applying parametric variations in the nominal model used to compute the predictions. Since the aim of this work is to present



Fig. 11. CHB-STATCOM capacitive mode. (a) Steady-state v_{Ca1} , v_{Cb1} , v_{Cc1} , and $i_{a,b,c}$ capacitive mode. (b) Steady-state v_{Ca1} , v_{Ca2} , v_{Cb1} , v_{Cb2} , and $i_{a,b,c}$ capacitive mode. (c) Step response grid voltages and output currents capacitive mode. (d) Steady-state grid voltages and output currents capacitive mode.



Fig. 12. Steady-state CHB-STATCOM parametric variations. (a) v_{Ca1} , v_{Cb1} , v_{Cc1} , and $i_{a,b,c}$ inductive mode -20% R and L. (b) v_{Ca1} , v_{Cb1} , v_{Cc1} , and $i_{a,b,c}$ capacitive mode -20% R and L. (c) v_{Ca1} , v_{Cb1} , v_{Cc1} , and $i_{a,b,c}$ inductive mode +20% R and L. (d) v_{Ca1} , v_{Cb1} , v_{Cc1} , and $i_{a,b,c}$ capacitive mode +20% R and L. (d) v_{Ca1} , v_{Cb1} , v_{Cc1} , and $i_{a,b,c}$ inductive mode +20% R and L.

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	Nominal model	(R,L) - 20%	(R,L)+20%
THD inductive mode	2.965%	3.146%	2.984%
THD capacitive mode	3.287%	3.252%	3.498%

TABLE VII

TOTAL HARMONIC DISTORTION PARAMETRIC VARIATIONS



Fig. 13. Time comparison with "B and B Approach" in [18]. (a) Execution times comparison for different levels. (b) Time reduction of the proposed approach for different levels.

a current control method, only the parameters of the current model were changed, i.e., R and L, while the individual dc-link voltage balance was kept unchanged. Fig. 12(a) and (b) shows the performance when the rated inductance L and resistance R in the mathematical model are 20% smaller than the actual values. Conversely, Fig. 12(c) and (d) presents the performance when the controller considers R and L as 20% larger than the actual values. Table VII summarizes the total harmonic distortion of the three-phase output current for both cases and the nominal case, highlighting that the performance of the system is not degraded by these parametric variations.

E. Time Comparison With Existing Approaches

Fig. 13(a) shows the time spent with the proposed approach with different number of levels compared with the "B and B Approach" [18]. The performance of the "Fast MPC" [15] is omitted since it quickly exceeds the 50 μ s sampling time for n=3 and 100 μ s for n=4. To make a fair comparison, the methods were implemented on the same FPGA platform with the same technological choices, i.e., the computations were fully implemented on the FPGA, and only fixed-point arithmetic

operations were used (only the division in the "B and B Approach" in [18] was implemented with floating point arithmetic since the division is an ill-conditioned operation), the same degree of parallelism was employed by using 12 multipliers and accumulators. Fig. 13(a) also shows the time spent by the overall control in both cases, by including the time for samplings, computing the PLL, i_d^{ref} , and the voltage balancing procedure, which was implemented starting from [25]. Even if the proposed current control requires constant time, the overall time increases due to the voltage balance. However, it is clear that, with the proposed approach, we can still control an inverter with $n \ge 20$ within the 50 μ s sampling interval, whereas the approach in [18] fails if n > 10, forcing the design of a larger sampling time that leads to performance degradation for both steady-state and transient operations. Fig. 13(b) highlights the time reduction of our approach, which shows a time reduction of 97% for the current control and 57% for the overall control for n = 10, which remains stable for n = 20.

VI. CONCLUSION

The article presented a simple explicit solution for FCS-MPC of a CHB converter. A computational cost analysis was carried out and the number of individual operations was computed. The proposed method was compared with two well-known approaches in the literature. The method was tested using a five-level CHB-STATCOM. The computational time for the control algorithm was determined, and the hardware resources utilization on FPGA was presented. The proposed method overcomes the existing ones since it computed the optimum solution by requiring a few simple operations that did not depend on the number of levels of the converter.

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Open Access funding provided by 'Università degli Studi dell'Aquila' within the CRUI CARE Agreement