# Analysis and Experimental Validation of Current-Fed Switched Capacitor - based Modular DC Transformer

Qianhao Sun, *Student Member IEEE*, Yalou Li, Xiaolin Shen, Fan Cheng, Gen Li, *Member IEEE*, Jun Liang, *Senior Member, IEEE,* Qing Mu and Jingwei Meng

***Abstract*—Medium voltage dc (MVDC) power distribution grid is a key link to build dc power networks. In this paper, a novel input-series-output-parallel (ISOP) modular dc transformer (DCT) with the high-frequency-link (HFL) voltage buck-boost-matching strategy is proposed for MVDC grids application. The proposed DCT is composed of a current-fed switched capacitor structure and corresponding dual-active-bridge (DAB) converters, and they need to operate collaboratively to achieve the great property. Comparing with the traditional switched capacitor-based DCT (SCDCT), the most salient merits of the proposed DCT include the HFL voltage buck-boost adaptive regulation, the low conducting and switching current in switches and the capacitor voltages self-balance characteristic. These merits are all beneficial for the improvement of efficiency, operating reliability, switching performance and cost of DCT systems. Meanwhile, the proposed DCT reserves the advantages of SCDCT including redundant sub-module (SM) design and dc fault isolating capability. The topology, buck-boost modulation principle, capacitor voltage self-balance analysis, switching behaviors and comprehensive comparison with the traditional SCDCT are completed in detail. At last, the experimental results validate the effectiveness and correctness of the proposed solution.**

***Index Terms*—MVDC, dc transformer, current-fed converter, switched capacitor, buck-boost-matching strategy, dc fault ride-through, on-line redundant SM design, ISOP, dc/dc**

## I. Introduction

THE medium-voltage direct-current (MVDC) distribution power grid is one of the key technologies for building smart and strong power systems with its supreme characteristics as high power quality and reliability, small floor space, flexible operating modes, easy connecting with the renewable energy systems and energy storage systems, etc [1]-[3].

In MVDC, the dc transformer (DCT) is an important device to connect MVDC and low-voltage dc (LVDC) buses and realize the necessary galvanic isolation and power delivery [4] - [5]. Besides, the modular technology is a very promising and feasible solution to achieve the MVDC interface for DCT systems, considering the power and voltage level of single power electronic switch and technical difficulties of series connection of several power electronic switches [6]-[7].

For the MVDC DCT, two main schemes based on the modular technology are compared as follow. The first popular scheme is the MMC-based DCT, which is extended from the emerging modular multilevel converters (MMCs) [8]-[10]. This scheme is realized by replacing the single-switch with the corresponding series modular structure, such as half-bridge, full-bridge or hybrid topology [11]-[12]. A lot of literature have developed the optimal controls and modulations for the mentioned MMC-based DCTs. The sinusoidal -waveform controls are investigated for MMC-based DCT in [13]-[14]. However, the complex control of SM capacitor voltages decreases the system stability and practicability. Besides, the switching frequency can just be increased in a limited range, influencing the improvement of power density. To solve the above issues, the phase-shift control with different modulations are developed for MMC-based DCT [15]-[17]. However, the operating efficiency of MMC-based DCT still needs to be enhanced, and the technological difficulty in manufacture of the concentrated high-voltage large-capacity HF ac transformer also remains to be solved. Moreover, the unbalance power hinder the practical application of MMC-based DCTs [18].

To solve the above issues of MMC-based DCTs, the scheme of input-series-output-parallel multiple modular DCT (ISOP -DCT) is proposed as an alternative solution. Generally, the HFL dual- active-bridge (DAB) is selected as the typical dc/dc unit because of the merits of high power density, galvanic isolation, ease of realizing soft switching, small volume and noise, and flexible modulation, etc [19]-[21]. However, the redundant SMs design and dc fault isolating capability can not be obtained by the DAB-based DCTs, therefore, a dc breaker (DCB) is required in practical application. These demerits will lead to a large dc fault current, long fault-recovery time and high capital cost for MVDC power grids. In fact, it is impossible for MVDC distribution power grid to employ a

Manuscript received Jul.15, 2019; revised Sep. 21, 2019; accepted Nov. 21, 2019. This work was supported by the National Natural Science Foundation of China under grant no. 51877116, and the Project of Science and Technology of State Grid Economic and Technological Research Institute Co., Ltd under grant no. 524414190001. (*Corresponding author: Qianhao Sun.*)

Q. Sun, and J. Meng are with the Department of Electrical Engineering, Tsinghua University, Beijing 100084, China (e-mail: sxsunqianhao@163.com; 15600932170@163.com).

Y. Li, F. Cheng and Q. Mu are with the China Electric Power Research Institute, Beijing 100192, China (e-mail: liyalou@epri.sgcc.com.cn; chengfan 5566@163.com; muqing@epri.sgcc. com.cn).

X. Shen is with the State Power Economic Research Institute, Beijing 102209, China (e-mail: 874573376@qq.com).

G. Li and J. Liang are with the School of Engineering, Cardiff University, Cardiff, CF24 3AA, U.K. (e-mail: LiG9; LiangJ1{@cardiff.ac.uk}).

DCT without redundant SMs. Therefore, to further address the above issues of ISOP-DCTs, the hybrid-full-bridge and isolated-full-bridge DC/DC SM are proposed in [22]. However, similar to the MMC-based DCT, the unbalance power still occurs in above solution due to the parameter difference of arm inductance. Meanwhile, the dc current spike may occur in the operation, which will damage the switching devices. In addition, the capacitor voltage balance control is required in each SM due to the influence of arm inductors. Under above research background, the traditional switched capacitor (SC) -based SM is developed for ISOP-DCT [23]. However, the operating efficiency of traditional SC-based DCT (SCDCT) is lower due to the hard-switching and multi-step conversion. From the view of HFL voltages, the SCDCT is actually a boost converter. This increases the difficulty of the design and cost for ISOP-DCT systems due to the parameters are not related with the rated dc voltage values but the operating boundary values.

To address the above-mentioned issues of SCDCT and promote the development of MVDC distribution power network, a novel current-fed ISOP-DCT (abbreviated as CFSC) is proposed and analyzed in this paper. Meanwhile, the proper HFL voltage buck-boost adaptive matching switching strategy (B2AM) with the dc capacitor voltages self-balance is also developed for CFSC. All of the proposed solutions are validated by the experimental results including the steady-state operations, dc terminal voltage dynamic regulations, redundant SMs on-line switching and dc fault isolation based on a CFSC prototype with 4 (3+1) SMs.

## II. Topology and Operating Modes of CFSC

The topology of CFSC is shown in Fig. 1(a), where there are $n$ inserted SMs and $m$ on-line redundant SMs. Meanwhile, the value of $n$ and $m$ can be regulated according to the requirement of power and voltage levels. When CFSC is just composed of one SM, the evolutionary topology is presented in Fig. 1(b). In each SM, there are four switches and four switched capacitors (SCs), and each SC is isolated by the corresponding switch. Moreover, the midpoints of the SC structure in each SM are connected with two ac outputs of the corresponding DABs, which endows the proposed CFSC with the dc fault isolation capability, on-line redundant SMs design, and HFL voltages buck-boost adaptive regulating function. Based on the above advantages, the efficiency, operating reliability, practicability, switching performance and economic benefit of DCT system can be improved.

In CFSC, each SM works under three different operating states: the inserted state, on-line redundant state and blocking state.

(1)When SMi is under the inserted state, all switches are triggered by the corresponding pulses which are generated by the control and modulation system of CFSC.

(2) When SMi is under the on-line redundant state, $S_{ai1}$~ $S_{ai4}$ are under the ON states and $S_{bi1}$~ $S_{bi4}$, $Q_{i1}$~ $Q_{i4}$ are under the OFF state, leading to the dc terminal voltage $V_{api}$ of SMi is 0, and the capacitor voltages $V_{Ci1}$~ $V_{Ci4}$ can be maintained during the on-line redundant period. That is to say, the on-line

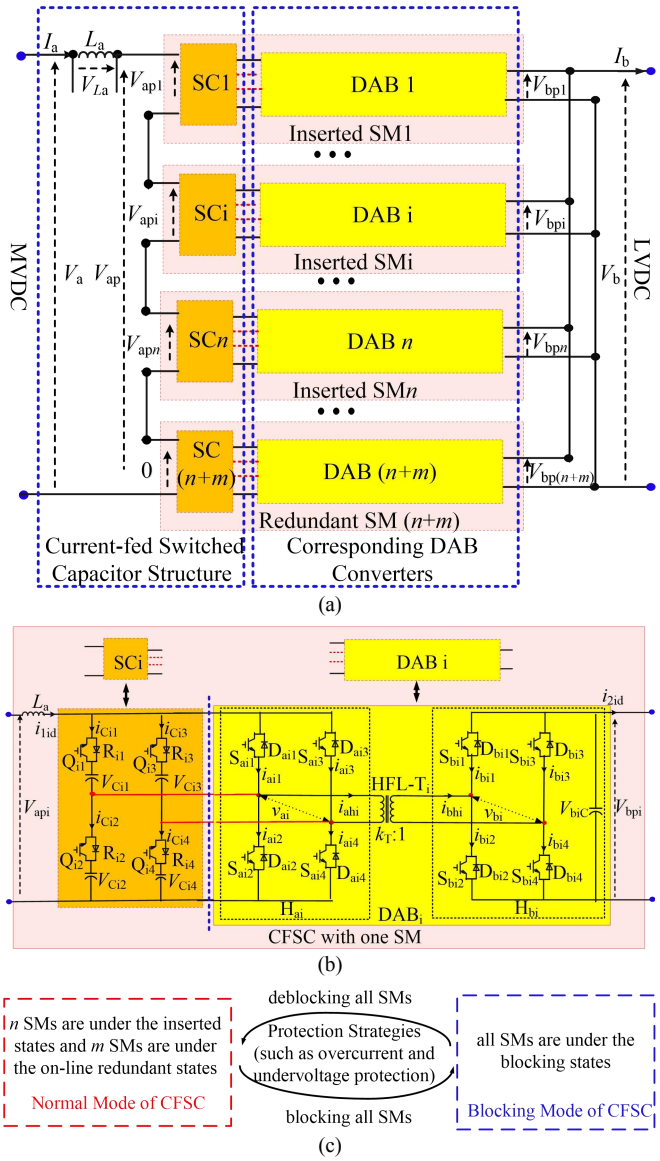



Fig.1. Topology and operating modes of CFSC. (a) CFSC with $(n+m)$ SMs, (b) CFSC with one SM (c) operating modes of CFSC.

redundant SMs do not influence the voltage balance control in MVDC side of CFSC. Therefore, the location order of inserted SMs and on-line redundant SMs can be arranged randomly. Moreover, because the capacitor voltages can be maintained during this operating state, the design of on-line redundant SMs can be obtained for CFSC. Then, the operating reliability can be improved obviously.

(3)When SMi is under the blocking state, all switches including $S_{ai1}$~ $S_{ai4}$, $S_{bi1}$~ $S_{bi4}$ and $Q_{i1}$~ $Q_{i4}$ are under the OFF states. Similar to the on-line redundant state, $V_{Ci1}$ ~ $V_{Ci4}$ can also be maintained during this period, decreasing the dc fault discharge current and bringing the fast fault recovery.

According to above analysis, there are two operating modes defined for CFSC in this paper: the normal mode and blocking mode, as shown in Fig. 1(c). When $n$ SMs are under the inserted states and $m$ SMs are under the on-line redundant states, the operating mode is defined as the normal mode. When all SMs are under the blocking states, the operating mode is defined as the blocking mode.

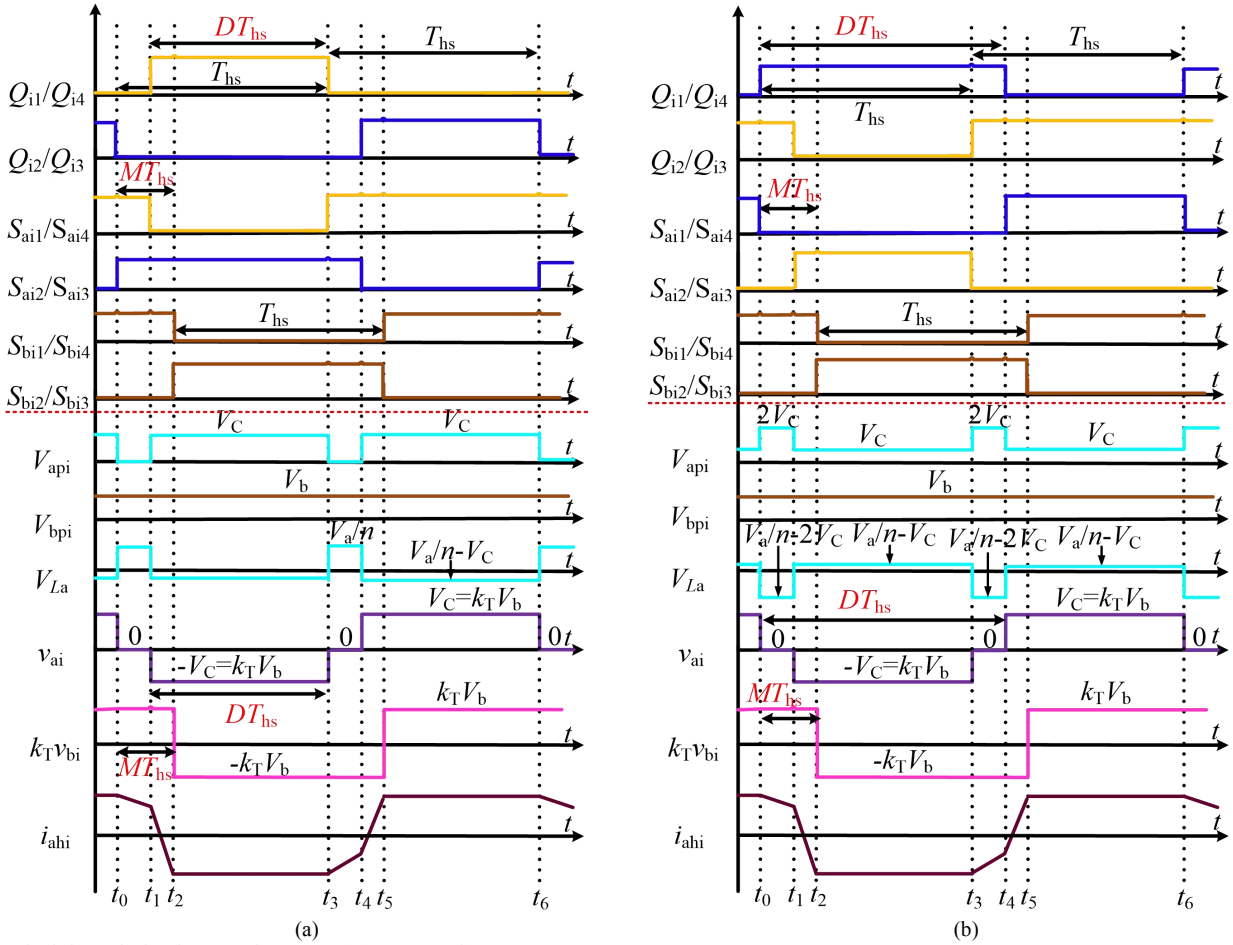



Fig. 2. Principle analysis of B2AM for CFSC. (a) 0 <$D$ ≤1 (b) 1 <$D$ <2

## III. HFL Voltage Amplitudes Buck-Boost Adaptive Matching Switching Strategy for CFSC

To avoid the mismatch issue of dc terminal voltages and improve the efficiency and operating performance of CFSC, a proper HFL voltage amplitudes buck-boost adaptive matching strategy (B2AM) is proposed for CFSC in this paper. In the following analysis, $T_{hs}$ is the half switching period, $D$ is the high-level duty of half switching period (0 <$D$ <2), $M$ is the phase-shift ratio between $H_{ai}$ and $H_{bi}$, $V_C$ is the average capacitor voltage of each SC structure, $k_T$ is the transformer ratio of each DAB, $k_{dc}$ =$V_a$/($nV_b$) is the dc terminal voltages ratio of each SM, $k_{ac}$= $A(v_{ai})$/ $A(k_Tv_{bi})$ is the HFL voltages ratio where $A(x)$ is the amplitude function of $x$. Then, the principle of B2AM for CFSC can be described as follows.

Firstly, differing with the typical HFL modulations only include constant high-level duty $D$ ($D$ = 1) for all switches, the high-level duties in the current-fed SC structure, $H_{ai}$ and $H_{bi}$ are variable and different. In the current-fed SC structure, the high-level duty $D$ is controlled adaptively by CFSC based on the relationship between the dc terminal voltages ratio $k_{dc}$ and transformer ratio $k_T$. The modulation pulses of $Q_{i1}$ and $Q_{i4}$ are identical while $Q_{i2}$ and $Q_{i3}$ are also identical. In $H_{ai}$, the pulses of $S_{ai1}$ and $S_{ai4}$ are identical and complementary with $Q_{i1}$, while the pulses of $S_{ai2}$ and $S_{ai3}$ are identical and complementary with $Q_{i2}$. Accordingly, the high-level duties of switches in $H_{ai}$ are (2-$D$). In $H_{bi}$, the high-level duties of switches are fixed at 1 which is the same with the typical HFL modulations. Meanwhile, the pulses of $S_{bi1}$ and $S_{bi4}$ are identical, and the pulses of $S_{bi2}$ and $S_{bi3}$ are also identical. Secondly, there is a 180° phase-shift angle between the pulses of $Q_{i1}$ and $Q_{i2}$, as well as $S_{bi1}$ and $S_{bi2}$. Based on the above principle of B2AM, the HFL voltage buck-boost adaptive control can be achieved by adjusting $D$. With different value of $D$, there are two kinds of operating states for CFSC, as shown in Fig. 2(a) and (b).

When 0 < $D$ ≤ 1, the waveforms are presented in Fig. 2(a), and there are six stages in each switching period. Because of the operation symmetry, the first three stages are analyzed, and the last three stages can be analyzed similarly.

During $t_0$~$t_1$, $Q_{i1}$~$Q_{i4}$, $S_{bi2}$ and $S_{bi3}$ are under the OFF states while $S_{ai1}$ ~ $S_{ai4}$, $S_{bi1}$ and $S_{bi4}$ are under the ON states. The HFL voltages $v_{ai}$, $v_{bi}$ and the dc terminal voltages $V_{api}$, $V_{bpi}$ can be derived from

$$\begin{cases} v_{ai} = 0 \\ v_{bi} = V_b \end{cases} \text{ and } \begin{cases} V_{api} = 0 \\ V_{bpi} = V_b \end{cases} \tag{1}$$

During $t_1$~$t_2$, $Q_{i2}$, $Q_{i3}$, $S_{ai1}$, $S_{ai4}$, $S_{bi2}$ and $S_{bi3}$ are the under OFF states while $Q_{i1}$, $Q_{i4}$, $S_{ai2}$, $S_{ai3}$, $S_{bi1}$ and $S_{bi4}$ are under the ON states. Accordingly, $v_{ai}$, $v_{bi}$, $V_{api}$, and $V_{bpi}$ can be derived from:

$$\begin{cases} v_{ai} = -V_C \\ v_{bi} = V_b \end{cases} \text{ and } \begin{cases} V_{api} = V_C \\ V_{bpi} = V_b \end{cases} \tag{2}$$

During $t_2$~$t_3$, $Q_{i2}$, $Q_{i3}$, $S_{ai1}$, $S_{ai4}$, $S_{bi1}$ and $S_{bi4}$ are under the OFF

states, $Q_{i1}$, $Q_{i4}$, $S_{ai2}$, $S_{ai3}$, $S_{bi2}$ and $S_{bi3}$ are under the ON states. Then, $v_{ai}$, $v_{bi}$, $V_{api}$, and $V_{bpi}$ can be derived from:

$$\begin{cases} v_{ai} = -V_C \\ v_{bi} = -V_b \end{cases} \text{ and } \begin{cases} V_{api} = V_C \\ V_{bpi} = V_b \end{cases} \tag{3}$$

From (1) ~ (3), $v_{ai}$, $v_{bi}$, $V_{api}$, and $V_{bpi}$ in one switching period can be derived from:

$$\begin{cases} v_{ai} = \begin{cases} 0 & [t_0, t_1] \text{ and } [t_3, t_4] \\ -V_C & [t_1, t_3] \\ V_C & [t_4, t_6] \end{cases} \\ v_{bi} = \begin{cases} V_b & [t_0, t_2] \text{ and } [t_5, t_6] \\ -V_b & [t_2, t_5] \end{cases} \\ V_{api} = \begin{cases} 0 & [t_0, t_1] \text{ and } [t_3, t_4] \\ V_C & \text{other} \end{cases} \\ V_{bpi} = V_b \end{cases} \tag{4}$$

As the average voltage drop of dc inductor $L_a$ is 0 in one period, the following relationship can be derived:

$$D\left(\frac{V_a}{n} - V_C\right) + (1-D)\frac{V_a}{n} = 0 \tag{5}$$

Therefore, $V_C$ can be derived from $V_a$

$$V_C = \frac{V_a}{nD} \tag{6}$$

According to (6) and $0 < D \le 1$, the capacitor voltage is larger than $V_a/n$ in this situation. Therefore, the HFL voltage amplitude of $v_{ai}$ is larger than $V_a/n$. The CFSC is a boost converter from the view of HFL voltage.

Similarly, when $1 < D < 2$, the relationship between HFL voltages $v_{ai}$, $v_{bi}$ and $V_a$, $V_b$ are same with them in $0 < D \le 1$ while the dc voltages $V_{api}$, $V_{bpi}$ in one switching period are different

$$\begin{cases} V_{api} = \begin{cases} 2V_C & [t_0, t_1] \text{ and } [t_3, t_4] \\ V_C & \text{other} \end{cases} \\ V_{bpi} = V_b \end{cases} \tag{7}$$

Accordingly, the following relationship can be derived:

$$(2-D)\left(\frac{V_a}{n} - V_C\right) + \left(\frac{V_a}{n} - 2V_C\right)(D-1) = 0 \tag{8}$$

According to (7) and (8), $V_C$ can be still derived from (6). When $1 < D < 2$, CFSC is a buck converter in this condition from the view of HFL voltage.

From the above analysis, CFSC is a buck-boost converter under B2AM. From the analysis in [23], the HFL voltage amplitudes of $v_{ai}$ and $v_{bi}$ should be equivalent to obtain great HFL performance. Therefore, the following equation can be obtained:

$$\frac{V_a}{nD} = k_T V_b \tag{9}$$

The Eq. (9) can be maintained adaptively with different value of $k_{dc}$. Thus:

$$D = \frac{V_a}{k_T n V_b} = \frac{k_{dc}}{k_T} \tag{10}$$

and Eq. (10) is always correct under B2AM.

According to (10), the $D$ in B2AM is only depended on the dc terminal voltages $V_a$ and $V_b$ of CFSC. Because $V_a$ and $V_b$ can be measured conveniently, B2AM can be achieved for CFSC easily. Meanwhile, the HFL voltages $v_{ai}$ and $k_T v_{bi}$ of B2AM in one switching period can be described as:

$$\begin{cases} v_{ai} = \begin{cases} 0 & [t_0, t_1] \text{ and } [t_3, t_4] \\ -k_T V_b & [t_1, t_3] \\ k_T V_b & [t_4, t_6] \end{cases} \\ v_{bi} = \begin{cases} V_b & [t_0, t_2] \text{ and } [t_5, t_6] \\ -V_b & [t_2, t_5] \end{cases} \end{cases} \tag{11}$$

From (11), the amplitudes of $v_{ai}$ and $v_{bi}$ satisfy $A(v_{ai}) = k_T A(v_{bi}) = k_T V_b$ in the whole operating range, thus optimizing the HFL and switching performance.

## IV. Comprehensive Operating Performance Analysis for CFSC Under B2AM

The HFL voltage amplitudes of CFSC can be regulated actively to match the dc terminal voltages by B2AM from the analysis in Section III. This merit will bring the optimization for the switching performance, operating efficiency and reliability for CFSC.

Assuming the equivalent leakage inductance value of HFL transformer in SMi is $L$, the HFL currents $i_{ahi}$ and $i_{ahi}$ can be obtained:

$$\begin{cases} i_{ahi}(t) = \int_{t_0}^{t} \frac{v_{ai} - k_T v_{bi}}{L} dt + i_{ahi}(t_0) \\ i_{bhi}(t) = k_T i_{ahi}(t) \end{cases} \tag{12}$$

According to the operating symmetry and (12), the HFL current $i_{ahi}$ in one switching period can be presented as:

$$i_{ahi}(t) = \begin{cases} \frac{k_T V_b T_{hs}}{2L}(2M - D') - \frac{k_T V_b}{L}(t - t_0) & [t_0, t_1] \\ \frac{k_T V_b T_{hs}}{2L}(2M - 3D') - \frac{2k_T V_b}{L}(t - t_1) & [t_1, t_2] \\ \frac{k_T V_b T_{hs}}{2L}(D' - 2M) & [t_2, t_3] \\ \frac{k_T V_b T_{hs}}{2L}(D' - 2M) + \frac{k_T V_b}{L}(t - t_3) & [t_3, t_4] \\ \frac{k_T V_b T_{hs}}{2L}(3D' - 2M) + \frac{2k_T V_b}{L}(t - t_4) & [t_4, t_5] \\ \frac{k_T V_b T_{hs}}{2L}(2M - D') & [t_5, t_6] \end{cases} \tag{13}$$

where

$$D' = \begin{cases} 1 - D & 0 < D \le 1 \\ D - 1 & 1 < D < 2 \end{cases} \tag{14}$$

Then, the transmission power of CFSC can be derived as:

$$P_{CFSC} = nP_{SMi} = \frac{n}{T_{hs}}\int_0^{T_{hs}} v_{ai}(t) i_{ahi}(t) dt = \frac{n}{T_{hs}}\int_0^{T_{hs}} v_{bi}(t) i_{bhi}(t) dt \tag{15}$$
$$= \frac{n(k_T V_b)^2 T_{hs}}{2L}\left[2M - D' - M^2 - (M - D')^2\right]$$

Based on (15), the dc current $I_a$ and $I_b$ can be calculated as:

$$\begin{cases} I_a = \frac{P_{CFSC}}{V_a} = \frac{n(k_T V_b)^2 T_{hs}}{2LV_a}\left[2M - D' - M^2 - (M - D')^2\right] \\ I_b = \frac{P_{CFSC}}{V_b} = \frac{n(k_T)^2 T_{hs} V_b}{2L}\left[2M - D' - M^2 - (M - D')^2\right] \end{cases} \tag{16}$$

### A. Capacitor voltage self-balance analysis

With operating symmetry of CFSC, only dynamic performances of $C_{i1}$ and $C_{i2}$ are analyzed, and the dynamic performances of $C_{i3}$ and $C_{i4}$ can be analyzed similarly.

The current flows $C_{i1}$ and $C_{i2}$ in one switching period are:

$$\begin{cases} 0<D\le 1 \begin{cases} i_{Ci1}(t)=\begin{cases} \dfrac{I_a(t)+i_{ahi}(t)}{2} & [t_1,t_3] \\ 0 & [t_0,t_1]\text{and}[t_3,t_6] \end{cases} \\ i_{Ci2}(t)=\begin{cases} 0 & [t_0,t_4] \\ \dfrac{I_a(t)-i_{ahi}(t)}{2} & [t_4,t_6] \end{cases} \end{cases} \\ 1<D<2 \begin{cases} i_{Ci1}(t)=\begin{cases} \dfrac{I_a(t)+i_{ahi}(t)}{2} & [t_0,t_4] \\ 0 & [t_4,t_6] \end{cases} \\ i_{Ci2}(t)=\begin{cases} \dfrac{I_a(t)-i_{ahi}(t)}{2} & [t_0,t_1]\text{and}[t_3,t_6] \\ 0 & [t_1,t_3] \end{cases} \end{cases} \end{cases} \tag{17}$$

Based on (13) and (17), the charging variation of $C_{i1}$ and $C_{i2}$ in one switching period can be calculated:

$$\begin{cases} 0<D\le 1 \begin{cases} \int_0^{2T_{hs}} i_{Ci1}(t)dt=\int_{t_1}^{t_3}\dfrac{I_a+i_{ahi}(t)}{2}dt=\dfrac{1}{2}\left[I_aDT_{hs}+\int_{t_1}^{t_3}i_{ahi}(t)dt\right] \\ =\dfrac{k_TV_bT_{hs}^{\ 2}}{4L}\left\{\left[-D'^2+MD'\right]+\int_{t_1}^{t_2}i_{ahi}(t)dt\right\}=0 \\ \int_0^{2T_{hs}} i_{Ci2}(t)dt=\int_{t_4}^{t_6}\dfrac{I_a(t)-i_{ahi}(t)}{2}dt=\dfrac{1}{2}\left[I_aDT_{hs}-\int_{t_4}^{t_6}i_{ahi}(t)dt\right] \\ =\dfrac{1}{2}\left[I_aDT_{hs}+\int_{t_1}^{t_3}i_{ahi}(t)dt\right]=0 \end{cases} \\ 1<D<2 \begin{cases} \int_0^{2T_{hs}} i_{Ci1}(t)dt=\int_{t_0}^{t_4}\dfrac{I_a(t)+i_{ahi}(t)}{2}dt \\ =\dfrac{1}{2}\left[I_aDT_{hs}+\int_{t_0}^{t_4}i_{ahi}(t)dt\right]=0 \\ \int_0^{2T_{hs}} i_{Ci2}(t)dt=\int_{t_0}^{t_1}\dfrac{I_a(t)-i_{ahi}(t)}{2}dt+\int_{t_3}^{t_6}\dfrac{I_a(t)-i_{ahi}(t)}{2}dt \\ =\dfrac{1}{2}\left[I_aDT_{hs}+\int_{t_0}^{t_4}i_{ahi}(t)dt\right]=0 \end{cases} \end{cases} \tag{18}$$

From (18), the energy variation of $C_{i1}$ and $C_{i2}$ in one switching period are always 0 no matter what the operating condition of CFSC is. That is to say, the voltages of $C_{i1}$ and $C_{i2}$ can be balanced naturally by the B2AM. Based on the self-balanced characteristic, the closed loop control system architecture of traditional SCDCT can also be employed for CFSC to delivery power.

### B. Switching performance analysis

When $0<D\le 1$, the first switching behavior occurs at $t_0$. The current path at $t_0^-$ is described in Fig. 3(a), where the current flows through $Q_{i2}$, $Q_{i3}$, $S_{ai1}$, $S_{ai4}$, $D_{bi1}$ and $D_{bi4}$. Meanwhile, the current path $t_0^+$ is described in Fig. 3(b), where the current flows through $S_{ai1}$, $S_{ai4}$, $D_{ai2}$, $D_{ai3}$, $D_{bi1}$ and $D_{bi4}$. From this commutation procedure the $S_{ai1}$ and $S_{ai4}$ turn-on with the zero-voltage switching (ZVS) while $Q_{i2}$ and $Q_{i3}$ turn-off with the hard-switching (HS) at $t_0$. Meanwhile, different with the SCDCT, the turn-off current of $Q_{i2}$ and $Q_{i3}$ in CFSC under B2AM is just the small discharge current ($t_0$) of the switched-capacitor, which is much smaller than that in SCDCT. This will increase the operating efficiency. The second switching behavior occurs at $t_1$, where the switching states of $Q_{i1}$, $Q_{i4}$, $S_{ai1}$ and $S_{ai4}$ are changed. The current path at $t_1^-$ is illustrated in Fig. 3(b), and the current path at $t_1^+$ is illustrated in Fig. 3(c), where the current flows through $R_{i1}$, $R_{i4}$, $D_{ai2}$, $D_{ai3}$, $D_{bi1}$ and $D_{bi4}$. Therefore, $Q_{i1}$ and $Q_{i4}$ turn-on with the ZVS while $S_{ai1}$ and $S_{ai4}$ turn-off with the HS at $t_1$ in this commutation procedure. The third switching behavior occurs at $t_2$, where the switching states of $S_{bi1}$, $S_{bi2}$, $S_{ai3}$, and $S_{ai4}$ are changed. The current paths of $t_2^-$ and $t_2^+$ are described in Figs. 3 (d) and (e), respectively. Because the current in Fig. 3(d) flows through $Q_{i1}$, $Q_{i4}$, $S_{ai2}$, $S_{ai3}$, $S_{bi1}$ and $S_{bi4}$, the current in Fig. 3(e) flows through $Q_{i1}$, $Q_{i4}$, $S_{ai2}$, $S_{ai3}$, $D_{bi2}$ and $D_{bi3}$, the $S_{bi2}$ and $S_{bi3}$ turn-on with the ZVS while the $S_{bi1}$ and $S_{bi4}$ turn-off with the HS at $t_2$.

For the next half switching period, the switching behavior can be analyzed similarly. According to the above analysis, all switches turn-on with the soft-switching while their turn-off procedures are the HS when $0<D\le 1$.

Meanwhile, we know the ZVS behavior connot be owned by SCDCT due to the turn-on and turn-off behaviors of switches in traditional SC both are with HS. From this view, the proposed CFSC has better turn-on performance than SCDCT. Besides, the power of SCDCT can be derived as:

$$P_{SCDCT}=\frac{n\left(k_TV_b\right)^2T_{hs}}{L}\left(M-M^2\right) \tag{19}$$

Then, the turn-off currents in one switching period of SCDCT and CFSC can be derived as:

$$\begin{cases} T_{off\_SCDCT\_SC}=\dfrac{k_TV_bT_{hs}}{L}\dfrac{M-M^2}{D} \\ T_{off\_SCDCT\_DAB}=\dfrac{k_TV_bT_{hs}}{L}M \end{cases} \tag{20}$$

and

$$\begin{cases} T_{off\_CFSC\_SC}=\dfrac{k_TV_bT_{hs}}{L}\dfrac{\left[1-\left(D+M\right)\right]^2}{2D} \\ T_{off\_CFSC\_DAB}=\dfrac{k_TV_bT_{hs}}{L}\dfrac{(1-D)^2+\left(D+M\right)^2-D-2M}{2D} \end{cases} \tag{21}$$

respectively. In (20) and (21), $T_{off\_SCDCT\_SC}$ and $T_{off\_SCDCT\_DAB}$ are the turn-off currents of switches in SC and DAB of SCDCT, respectively; $T_{off\_CFSC\_SC}$ and $T_{off\_CFSC\_DAB}$ are the turn-off currents of switches in SC and DAB of CFSC, respectively.

The turn-off current comparison of CFSC and SCDCT with the same transmission power can be described in Fig. 4(a) based on (15) and (19) ~ (21). According to Fig. 4(a), the CFSC has lower turn-off currents for switches both in SC and DAB with the same transmission power, which brings the better turn-off current performance. When $1<D<2$, the analysis is similar with $0<D\le 1$, and the above-mentioned conclusions are still effective. Form the above analysis, the CFSC has better switching performance than SCDCT, and this will be benefit to improve the efficiency of DCT system.

### C. Operating efficiency analysis

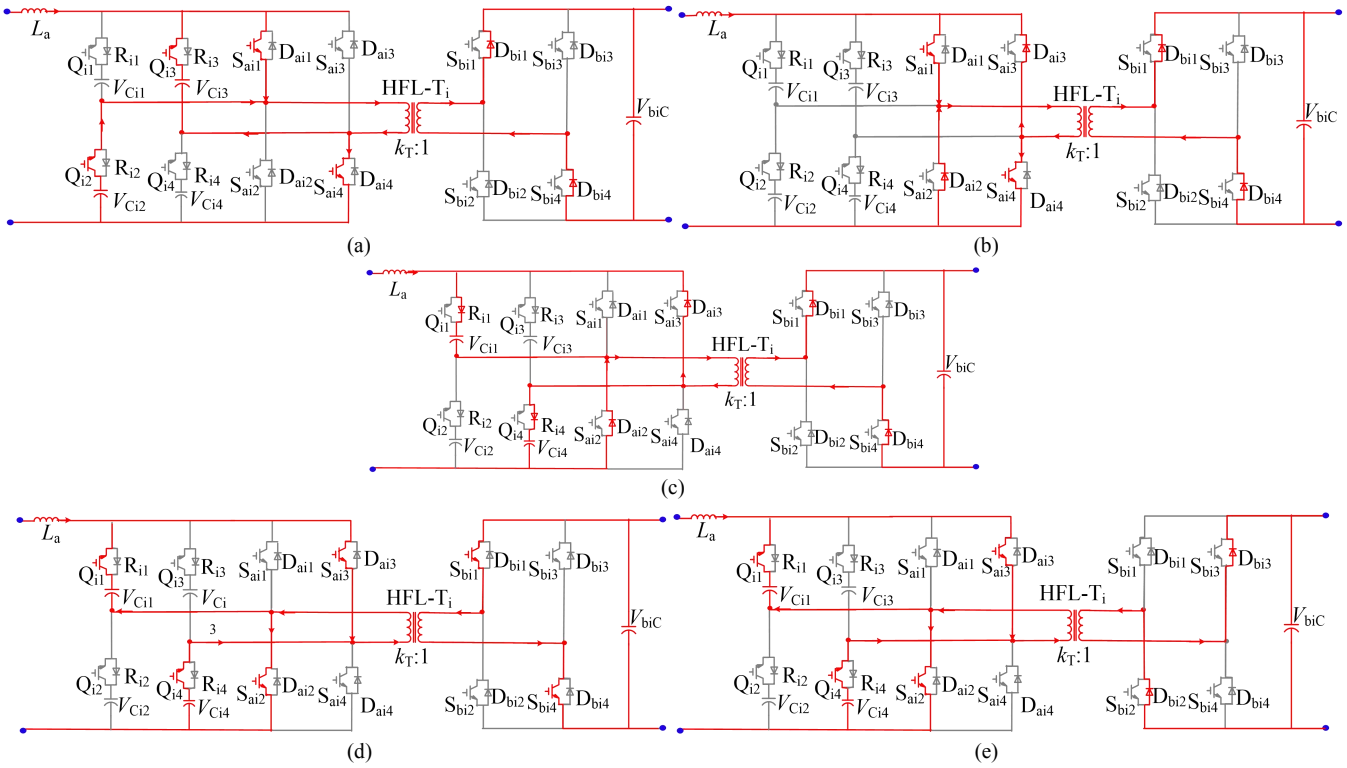



Fig.3. The circuits of switching performance analysis. (a) $t_0^-$ ($0<D\leq1$) (b) $t_0^+$ or $t_1^-$ ($0<D\leq1$) (c) $t_1^+$ ($0<D\leq1$) (d) $t_2^-$ ($0<D\leq1$) (e) $t_2^+$ ($0<D\leq1$)

The efficiency of CFSC and SCDCT can be calculated by the unified equation:

$$\eta = P/\left(P + P_{\text{loss}}\right) \tag{22}$$

where $P$ is the transmission power of DCT system, and $P_{\text{loss}}$ is the power loss of DCT system.

According to (22), there is a negative correlation between the efficiency and power loss of DCT system. To compare the operating efficiency of CFSC and SCDCT, the power loss with the same transmission power is considered. Similar to SCDCT, the total power loss of CFSC can be calculated as:

$$\begin{aligned} P_{\text{loss}} &= P_{\text{L\_dc-link}} + P_{\text{L\_HFL}} + P_{\text{L\_SW}} + P_{\text{L\_CON}} \\ &= R_{L_a} I^2_{\text{a\_RMS}} + n(P_{\text{L\_SW\_i}} + P_{\text{L\_CON\_i}} + P_{\text{L\_HFL}}) \\ &= R_{L_a} I^2_{\text{aRMS}} + nC_{\text{tr}} i^2_{\text{ahi\_RMS}} + n(P_{\text{L\_SW\_i}} + P_{\text{L\_CON\_i}}) \end{aligned} \tag{23}$$

where $P_{\text{L\_dc\_link}}$ and $P_{\text{L\_HFL}}$ are the power loss of dc-link and HFL of CFSC, respectively; $P_{\text{L\_SW}}$ and $P_{\text{L\_CON}}$ are switching and conduction power loss of switches of CFSC; $P_{\text{L\_SW\_i}}$ and $P_{\text{L\_CON\_i}}$ are the switching and conduction power loss of switches of one SM; $R_{\text{La}}$ is the equivalent resistances of $L_a$, $I_{\text{a\_RMS}}$ and $i_{\text{ahi\_RMS}}$ are the root-mean-square (RMS) value of $I_a$ and $i_{\text{ahi}}$, respectively; $C_{\text{tr}}$ are the equivalent coefficient of HF transformer, which is a constant for a specific HF transformer [24]-[26].

Because CFSC and SCDCT have the equivalent $I_{\text{a\_RMS}}$ and $i_{\text{ahi\_RMS}}$ with the same transmission power, the differences of power loss between CFSC and SCDCT are mainly composed of switching and conduction power loss in switches. Assuming each IGBT and diode have the same voltage drop $V_{\text{CE}}$, and the turn-off power loss of each switch with unit current is $e_{\text{SW}}$ [7].

The ratio of total switching and conduction power loss of CFSC and SCDCT can be derived as:

$$\begin{cases} R_{\text{L\_SW}} = \dfrac{nP_{\text{L\_SW\_i\_CFSC}}}{nP_{\text{L\_SW\_i\_SCDCT}}} = \dfrac{e_{\text{SW}}(4T_{\text{off\_CFSC\_SC}} + 4T_{off\_\text{CFSC\_DAB}})}{e_{\text{SW}}(2T_{\text{off\_SCDCT\_SC}} + 4T_{off\_\text{SCDCT\_DAB}})} \\ \quad = \dfrac{T_{\text{off\_CFSC\_SC}} + T_{off\_\text{CFSC\_DAB}}}{0.5T_{\text{off\_SCDCT\_SC}} + T_{off\_\text{SCDCT\_DAB}}} \\ R_{\text{L\_CON}} = \dfrac{nP_{\text{L\_CON\_i\_CFSC}}}{nP_{\text{L\_CON\_i\_SCDCT}}} = \dfrac{\dfrac{V_{\text{CE}}\int_0^{T_{\text{hs}}}\left(\left|I_{\text{a}} + i_{\text{ahi}}(t)\right| + \left|I_{\text{a}} - i_{\text{ahi}}(t)\right|\right)dt}{T_{\text{hs}}}}{\dfrac{V_{\text{CE}}\int_0^{T_{\text{hs}}}\left(2\left|i_{\text{ahi}}(t)\right|_{D=0}\right| + \left|I_{\text{a}}\right|\right)dt}{T_{\text{hs}}}} \\ \quad = \dfrac{\int_0^{T_{\text{hs}}}\left(\left|I_{\text{a}} + i_{\text{ahi}}(t)\right| + \left|I_{\text{a}} - i_{\text{ahi}}(t)\right|\right)dt}{\int_0^{T_{\text{hs}}}\left(2\left|i_{\text{ahi}}(t)\right|_{D=0}\right| + \left|I_{\text{a}}\right|\right)dt} \end{cases} \tag{24}$$

Based on (15), (19) and (24), the values of $R_{\text{L\_CON}}$ and $R_{\text{L\_SW}}$ with the varied transmission power are described in Fig. 4(b). It can be known from the figure that CFSC always has lower switching and conduction power loss due to the value of $R_{\text{L\_CON}}$ and $R_{\text{L\_SW}}$ in CFSC are always smaller than 1. Thus, the CFSC has the higher efficiency than SCDCT.

### *D. Application reliability analysis*

The proposed CFSC and traditional SCDCT both improve the reliability of DCT system due to the fault SM can be replaced by the on-line redundant SM. However, the realizable probability of on-line redundant state of each SM in CFSC and SCDCT are different. The on-line redundant state of CFSC and SCDCT are described in Fig. 4(c). The feasibility of on-line redundant state in SCDCT only depended on $Q_{i2}$ while that in

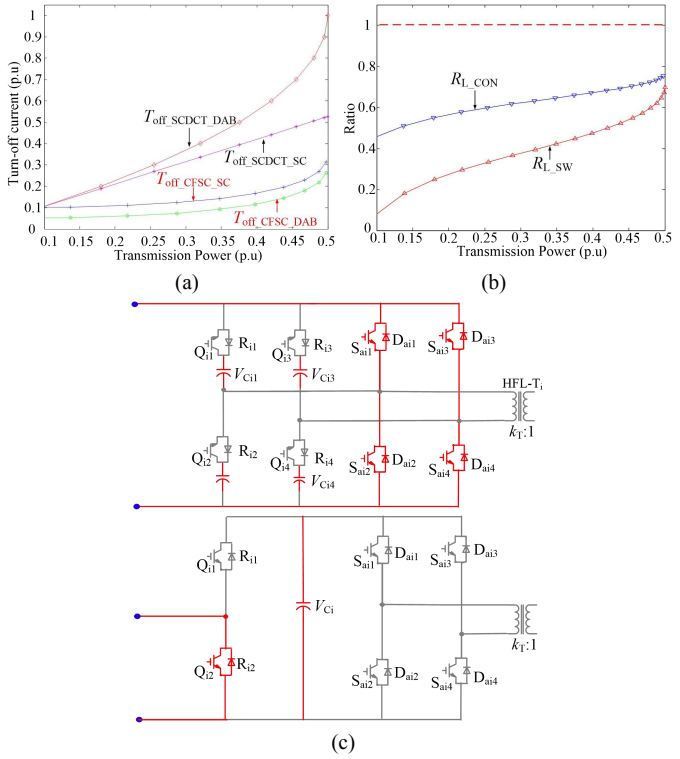



Fig. 4. Operating performance of CFSC under B2AM. (a) Turn-off current in switches (b) Ratios of power loss of CFSC and SCDCT (c) Comparison of the on-line redundant state of CFSC and SCDCT

CFSC depended on the combination of $Q_{i1}$~ $Q_{i4}$. Assuming the fault rate of each switch is $a$%, the realizable probability of on-line redundant state of each SM in SCDCT and CFSC can be obtained as:

$$\begin{cases} \mathrm{Re}_{CFSC} = 2(1-a\%)^2\left[1-(1-a\%)^2\right]+(1-a\%)^4 \\ \qquad = (1-a\%)(1+a\%-3*a\%*a\%-a\%*a\%*a\%) \\ \mathrm{Re}_{SCDCT} = 1-a\% \end{cases} \tag{25}$$

From (25), because $a\% < 5\%$ is convenient to be achieved for IGBT (or other switches), the $\mathrm{Re}_{CFSC}$ is always larger than $\mathrm{Re}_{SCDCT}$, therefore, CFSC has higher reliability than SCDCT.

## V. Control System Design and Main Parameter Calculation for CFSC Under B2AM

### A. Control system design of CFSC under B2AM

Based on the analysis in Section IV. A, the closed loop control system of CFSC is shown as Fig. 5, where $V_{Cr}$ is the reference value of capacitor voltage in MVDC, $V_{Ca}$ is the average value of all sampled SM capacitor voltage, $V_{Cai}$ is sampled capacitor voltage of SM$i$, $V_{br}$ is the reference voltage of LVDC, $V_{bi}$ is sampled LVDC voltage of SM$i$, $I_{ai}$ and $I_{bi}$ are sampled MVDC and LVDC currents of SM$i$, respectively. According to Fig. 5, the dc capacitor voltage is regulated by SC controller while LVDC voltage is controlled by the DAB controller. Thus, the $V_{Cr}$, $V_{Ca}$ and $V_{Cai}$ in CFSC can be obtained from:

$$\begin{cases} V_{Cai} = \dfrac{V_{Ci1}+V_{Ci2}+V_{Ci3}+V_{Ci4}}{4} \\ V_{Ca} = \sum_{i=1}^{n} V_{Cai} \Big/ n \quad V_{Cr} = k_T V_{bi} \end{cases} \tag{26}$$

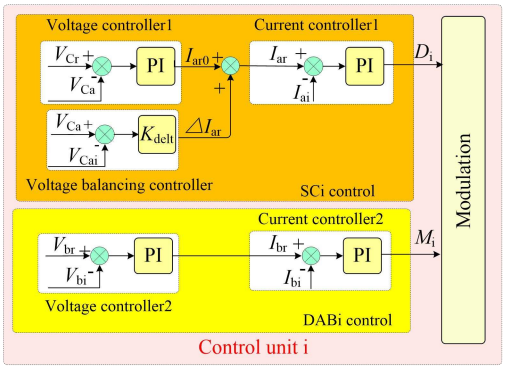



Fig. 5. Control system of SM$i$ of CFSC.

### B. Main parameter calculation of CFSC under B2AM

The transmission power of CFSC mainly depends on the following parameters: $V_a$, $V_b$, $k_T$, $L$ (HFL transformer leakage inductance), $n$ and $T_{hs}$ ($f_s$). When the CFSC is employed for MVDC power grid, the number of SM $n$ and the switching period $T_{hs}$ are usually determined by the withstand voltage of power switch which is employed in MVDC. Meanwhile, the HFL transformer ratio $k_T$ is also determined by the withstand voltage of power switch which is employed in LVDC. In this case, the transmission power of CFSC depends on $V_a$, $V_b$, and $L$. Assuming the rated power of CFSC is $P_{N\_CFSC}$, the minimum value of dc terminal voltages are $V_{amin}$ and $V_{bmin}$ ($V_{amin}$ $=nk_TV_{bmin}$), respectively. Considering $b$% overload, the HFL transformer leakage inductance $L$ should satisfy:

$$L < \frac{n\left(k_T V_{b\_min}\right)^2 T_{hs}\left(M_{max}-M_{max}^{\ 2}\right)}{(1+b\%)P_{N\_CFSC}} = \frac{n\left(k_T V_{b\_min}\right)^2 T_{hs}}{4(1+b\%)P_{N\_CFSC}} \tag{27}$$

In practical application, $L$ should also not be too small to obtain the great stability. Therefore, $L$ can be derived from:

$$L = (0.8 \sim 0.95)\frac{n\left(k_T V_{b\_min}\right)^2 T_{hs}}{4(1+b\%)P_{N\_CFSC}} \tag{28}$$

Meanwhile, to decrease the ripple of MVDC current and dc capacitor voltage, the values of dc inductor and switched capacitor should satisfy:

$$\begin{cases} \mathrm{MAX}\left[\left.\dfrac{\left(nk_T V_a V_b - V_a^{\ 2}\right)T_{hs}}{k_T n V_b c\%}\right|_{V_a<nk_TV_b}\right] < L_a \\ \& \\ \mathrm{MAX}\left[\left.\dfrac{\left(3nk_T V_a V_b - V_a^{\ 2} - 2\left(nk_T V_b\right)^2\right)T_{hs}}{k_T n V_b c\%}\right|_{V_a>nk_TV_b}\right] < L_a \end{cases} \tag{29}$$

and

$$\begin{cases} \mathrm{MAX}\left[\left.\dfrac{(1+b\%)P_{N\_CFSC}\left(nk_T V_b - V_a\right)}{k_T n V_a V_b d\%}\right|_{V_a<nk_TV_b}\right] < C_{SC} \\ \& \\ \mathrm{MAX}\left[\left.\dfrac{(1+b\%)P_{N\_CFSC}\left(V_a - nk_T V_b\right)}{k_T n V_a V_b d\%}\right|_{V_a>nk_TV_b}\right] < C_{SC} \end{cases} \tag{30}$$

where $V_a$ changes form $V_{amin}$ and $V_{amax}$, $V_b$ changes form $V_{bmin}$ and $V_{bmax}$, $c$% and $d$% are the ripple requirement of MVDC current and capacitor voltage, $C$sc is the value of switched capacitor, and MAX[•] is the maximum function.

In fact, the value of $L_a$ and $C$sc should be considered comprehensively with the volume, waveform of ripple and economy, etc. However, the equations (29) and (30) give the basic values about $L_a$ and $C$sc which is the main limitation for the selection of parameter.

## VI. Experimental Validation

To validate the proposed solution, a CFSC prototype is set up, as shown in Fig.6. The dc inductor $L_a$ = 1.5 mH, switched capacitors $C_{i1}$= $C_{i2}$ = $C_{i3}$= $C_{i4}$ = $C_{sc}$= 2200μF, HFL transformer leakage inductance $L_T$ = 200 μH, HFL transformer ratio $k_T$ = 1:1, and switching frequency is 20 kHz. In the CFSC, there are 4 SMs including 3 inserted SMs and 1 on-line redundant SM. Meanwhile, the main devices which are employed to measure the waveforms are shown in Table I.

When the dc voltages $V_a$ = 450V, $V_b$ = 150V ($V_a/n$ = 450V/3 = 150V = $k_TV_b$, $D$ = 1) and the transmission power $P$ = 650W, the experimental results of CFSC under B2AM are shown in Fig.7. In Fig. 7(a), $V_1$ = 450V, $V_2$ =150V, $I_1$ = 1.45A and $I_2$ = 4.2A, respectively. Thus, the actual input and output power of CFSC under this situation are about 652.5W and 630.5W, respectively, and the efficiency of CFSC is about 96.6%. Besides, $D$ is controlled at 1 because of the dc voltage ratio is matching the transformer ratio in this case. Meanwhile, the terminal voltages of SMs under the inserted states (SM1 ~ SM3) are balanced at 150V by the control of CFSC while the terminal voltage of on-line redundant SM (SM4) is 0 from Fig. 7(b). Besides, HFL voltages $v_{a1}$ and $v_{b1}$ are both square waveforms in Fig. 7(c). The results validate the correctness of CFSC under B2AM when $V_a/n = k_TV_b$.

When the dc voltages $V_a$ = 400V, $V_b$ = 150V ($V_a/n$ =400V/3< 150V= $k_TV_b$) and the transmission power $P$ = 650W, the experimental results of CFSC under B2AM are shown in Fig. 7. In Fig.8(a), $V_1$ = 400V, $V_2$ = 150V, $I_1$ = 1.63A and $I_2$ = 4.15A, respectively. Thus, the actual input and output power of CFSC in this situation are about 652W and 622.5W, respectively, and the efficiency of CFSC is about 95.5%. Besides, $D$ is controlled at 0.89 to match the dc voltage ratio with the transformer ratio. Meanwhile, the terminal voltages of SMs under the inserted states (SM1 ~ SM3) is changed from 150V to 0V as to regulate the switched capacitor voltages as shown in Fig.8 (b). Notably, the HFL voltage $v_{a1}$ is not a two-level but a three-level waveform in this case as shown in Fig.8(c). The results validate the correctness of CFSC under B2AM when $V_a/n < k_TV_b$.

When the dc voltages $V_a$ = 520V, $V_b$ = 150V ($V_a/n$ =520V/3 > 150V = $k_TV_b$) and the transmission power $P$ = 650W, the experimental results of CFSC under B2AM are shown in Fig.9. In Fig. 9(a), $V_1$ =520V, $V_2$ =150V, $I_1$= 1.25A and $I_2$= 4.1A, respectively. Thus, the actual input and output power of CFSC in this situation are about 650W and 615W, respectively, and the efficiency of CFSC is about 94.6%. Besides, $D$ is controlled at 1.15 to match the dc voltage ratio with the transformer ratio. The terminal voltages of SM1 ~ SM3 is changed from 150V to 300V to regulate the switched capacitor voltages, as shown in Fig.9(b). Meanwhile, the HFL voltage $v_{a1}$ is also a three-level waveform in this case as shown in Fig.9(c). The results validate the correctness of CFSC under B2AM when $V_a/n > k_TV_b$.

TABLE I
Experiment Devices

| Application | Devices |
|---|---|
| Voltage measurement | Tektronix P5200 |
| Current measurement | Fluke 80i-110s<br>Rogowski coil CWT03 |
| Power measurement | YokogawaWT210 |
| MVDC power supply | Full-bridge –based MMC |
| LVDC power supply | Photovoltaic simulator |
| Gate drive optocoupler of SM | FOD3180 |
| Driving power source of SM | DCH010515SN7 |
| Type of the switches | SiC |

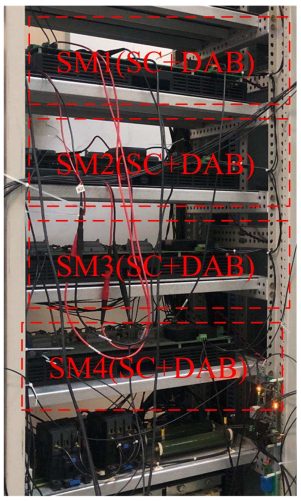


Fig. 6. The photograph of prototype in laboratory

Moreover, the dc switched capacitor voltages of CFSC with $V_a/n = k_TV_b$, $V_a/n < k_TV_b$, and $V_a/n > k_TV_b$ are presented in Fig. 10 (a) ~ (c). From the figures, the capacitor voltage of CFSC are always maintained at 150V no matter what the voltage value of MVDC bus is because of the adaptive regulation of $D$ in B2AM. Meanwhile, the arm currents of SC and DAB with $V_a/n < k_TV_b$ are shown in Fig. 10 (e) ~ (f), where the current in $H_{ai}$ of DABi are obviously different with $H_{bi}$ of DABi. The reason is that the SC and DAB need to operate cooperatively to deliver the power so as the waveform in $H_{ai}$ will be changed. That is to say, unlike the traditional SCDCT, the SC and DAB in CFSC are no longer two independent converters but just a whole dc/dc, which improves the efficiency.

The experimental results of MVDC bus voltage changes from 520V to 400V are shown in Fig.11. When the MVDC bus voltage changes, the capacitor voltages are not changed because it is adaptively regulated under B2AM. However, the duty ratio $D$ is changed in this case. Thus, the SM terminal voltage and HFL voltage and current are changed accordingly, as shown in Figs.11 (a) ~ (d). The above results validate the correctness and effectiveness of B2AM.

The operating mode switching results are shown in Figs.12 (a) ~ (c), where the dynamic procedure of SM cut-in and cut-out are fast and stable, validating the effectiveness of SM switching strategy of CDCT. Moreover, Figs. 13 (a) ~ (b) give the results of a pole-to-pole fault occurs at MVDC bus of CFSC. The MVDC voltage decreases immediately when the dc fault

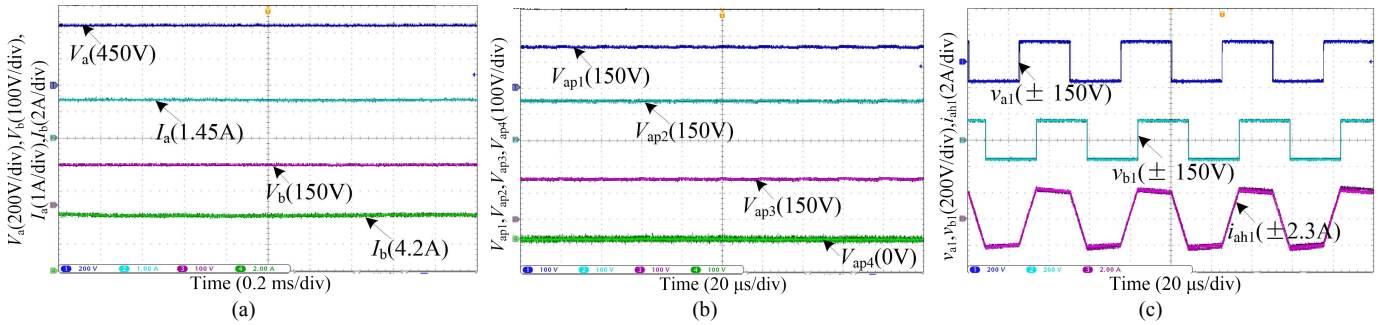



Fig.7. Results of CFSC under B2AM when $V_a/n = k_T V_b$ (a) dc voltages and currents, (b) SM terminal voltages, (c) HFL waveforms.

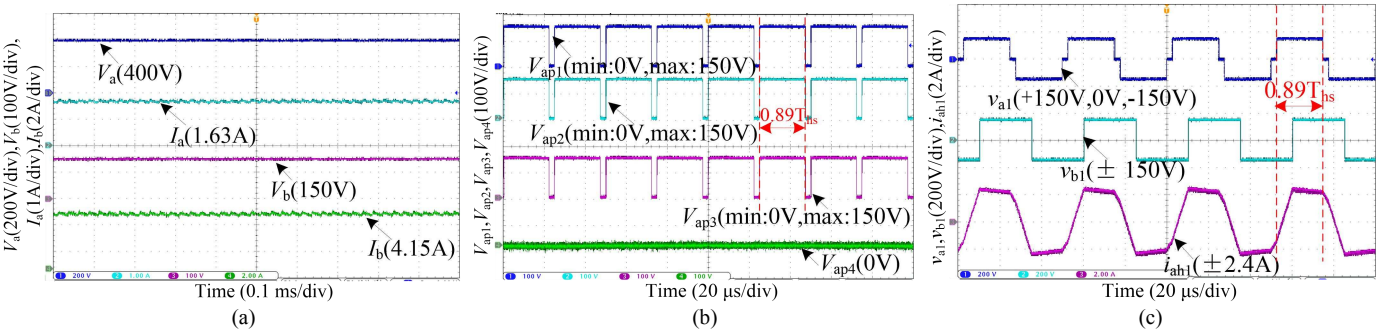



Fig.8. Results of CFSC under B2AM when $V_a/n < k_T V_b$ (a) dc voltages and currents, (b) SM terminal voltages, (c) HFL waveforms.

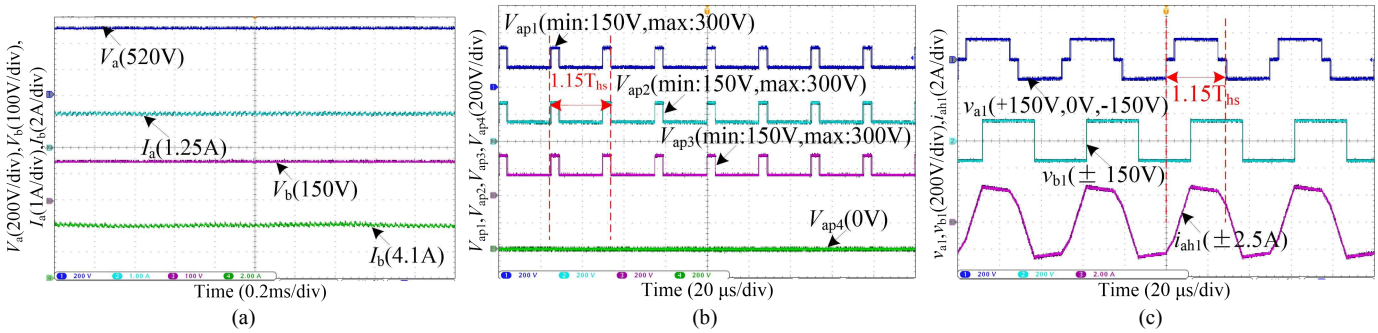



Fig.9. Results of CFSC under B2AM when $V_a/n > k_T V_b$ (a) dc voltages and currents, (b) SM terminal voltages, (c) HFL waveforms.

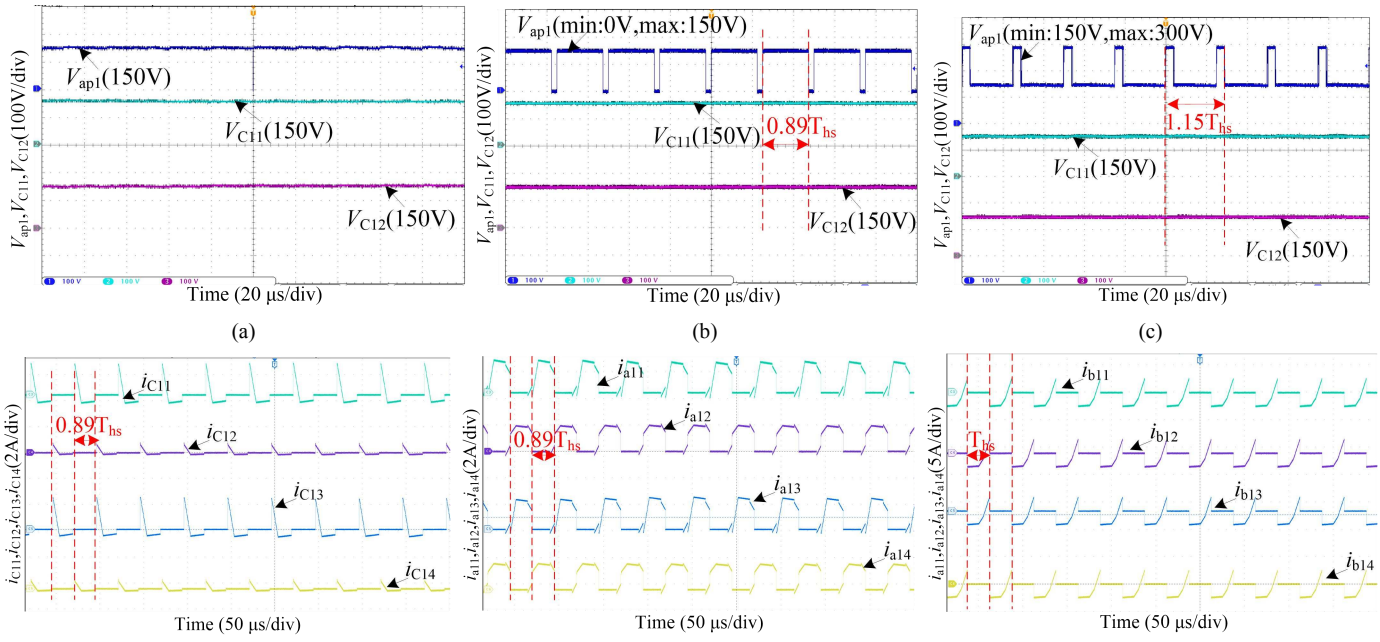



Fig.10. Capacitor voltages and currents of switches (a) capacitor voltages when $V_a/n = k_T V_b$, (b) capacitor voltages when $V_a/n < k_T V_b$, (c) capacitor voltages when $V_a/n > k_T V_b$, (d) currents of switches in SC when $V_a/n < k_T V_b$, (e) currents of switches in $H_a$ of DAB when $V_a/n < k_T V_b$, (f) currents of switches in $H_b$ of DAB when $V_a/n < k_T V_b$.

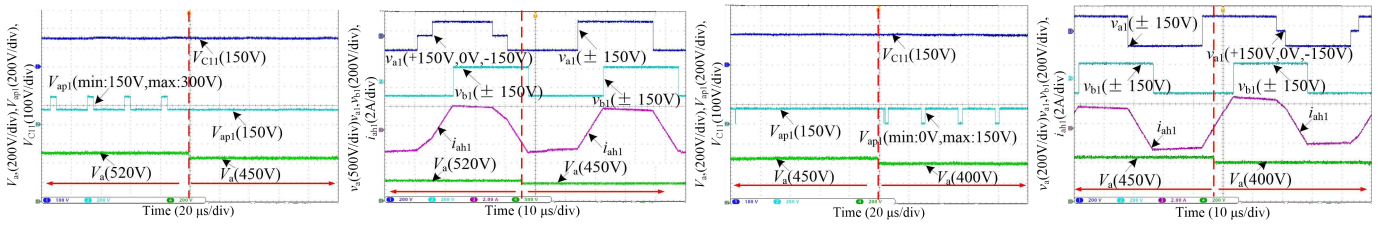



Fig.11. Results of the voltage change in MVDC bus (a) changing from 520V to 450V, (b) HFL waveforms, (c) changing from 450V to 400V, (d) HFL waveforms.

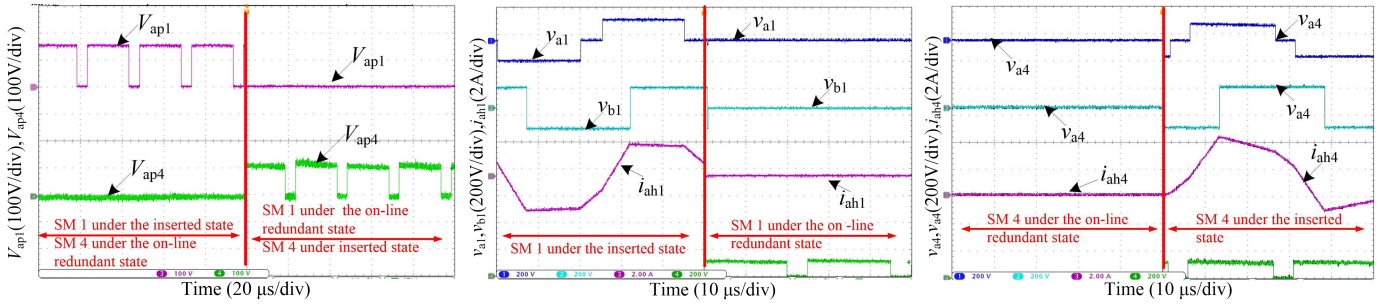



Fig.12. Results of redundant submodule switching. (a) SM terminal voltages, (b) HFL waveforms of cut-out SM, (c) HFL waveforms of cut-in SM

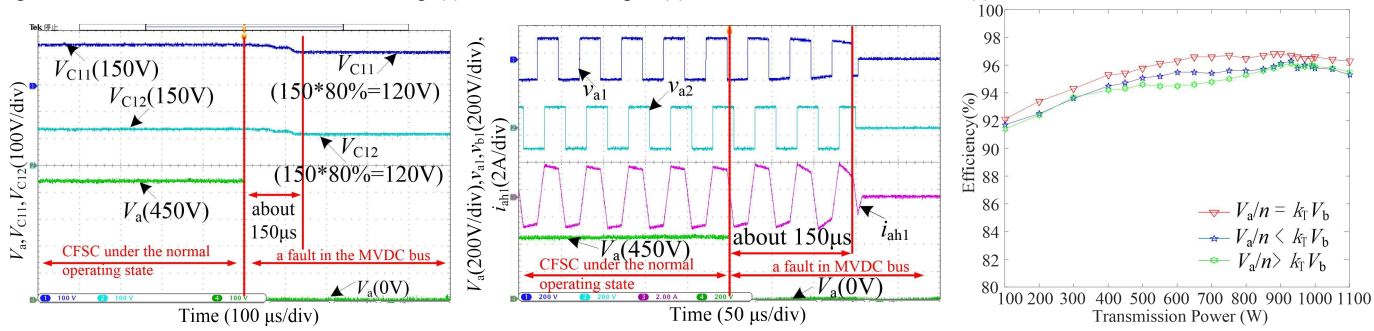



Fig.13. Results of MVDC bus fault. (a) capacitor voltages (b) HFL waveforms

Fig.14. Efficiency performance of CFSC under B2AM

occurs, and the CFSC is locked after about 0.15ms due to the under-voltage protection (the protection value in this paper is 120V, about 80% rated capacitor voltage). Therefore, the dc capacitor voltages in CFSC are maintained during the MVDC bus fault period, providing a fast recovery ability which is crucial for the improvement in power quality of MVDC grids.

Fig. 14 presents the efficiency performance of CFSC with the variation of the transmission power. It can be seen that the maximum efficiency of CFSC under B2AM can reach to 97.3%. Besides, the efficiency of CFSC under B2AM is stable no matter how is the relationship between dc voltage ratio and transformer ratio, which is better than that in the traditional two -level HFL modulation. Meanwhile, the average efficiency of CFSC under B2AM is about 94.9% ($V_a$ = 400V, $V_b$ = 150V) which is higher than that in SCDCT.

## VII. Conclusion

The CFSC based on current-fed switched capacitor structure is proposed and analyzed in this paper. The proposed CFSC integrates the advantages of DAB, MMC–based DCTs and traditional SCDCTs including modularity, flexible operation, redundant SM design, and dc fault ride-through capability. Meanwhile, the capacitor voltages self-balance characteristic and convenient control system can be achieved by the proposed B2AM, which regulates the HFL voltages adaptively to match the transformer ratio. All these merits above are meaningful for decreasing the difficulty of design and the cost, as well as increasing the efficiency, switching performance and reliability of DCT and MVDC systems. Besides, the effectiveness and correctness of the proposed solution both are validated by the comprehensive experimental results based on a prototype.

## References

[1] H. Suryanarayana and S. D. Sudhoff, "Design paradigm for power electronics-based DC distribution systems," *IEEE Journal of Emerging and Selected Topics in Power Electron*., vol. 5, no. 1, pp. 51-63, Mar. 2017.

[2] K. Mathuria, I. Hussain and N. Kumar, "A quadrature oscillator-based DT for accurate estimation of fundamental load current for PV system in distribution network," *IEEE Trans. Ind. Informat.,* vol. 15, no. 6, pp. 3324–3333, Jun. 2019.

[3] J. Esch, "High-power wind energy conversion systems: state-of-the-art and emerging technologies," *Proceedings of the IEEE.*, vol.103, no.5, pp.736–739, May. 2015.

[4] Y. Ji, Z. Yuan, J. Zhao, at el, "Overall control scheme for VSC-based medium-voltage DC power distribution networks," IET Generation, Transmission & Distribution, vol. 12, no. 6, pp. 1438-1445, Mar. 2018.

[5] B. Zhao, R. Zeng, Z. Yu, Q. Song, Y. Huang, Z. Chen, and T. Wei, "A more prospective look at IGCT: uncovering a promising choice for dc grids," *IEEE Industrial Electronics Magazine.*, vol. 12, no. 3, pp. 6–18, Sept. 2018.

[6] I. Gowaid, G. P. Adam, S. Ahmed, D. Holliday, and B. W. Williams, "Analysis and design of a modular multilevel converter with trapezoidal modulation for medium and high voltage DC-DC transformers," *IEEE Trans. Power Electron*., vol. 30, no. 10, pp. 5439–5457, Oct. 2015.
[7] D. Jovcic, and H. Zhang, "Dual channel control with DC fault ride through for MMC-based isolated DC/DC converter," *IEEE Trans. Power Delivery*, vol. 32, no. 3, pp. 1574-1582, Jan. 2017.
[8] A. M. Shotorbani , X. Meng , L. Wang and B. Mohammadi-Ivatloo. "A decentralized multiloop scheme for robust control of a power flow controller with two shunt modular multilevel converters," *IEEE Trans. Ind. Informat.,* vol. 14, no. 10, pp. 4309–4321, Oct. 2018.
[9] B. Fan, Y. Li, K. Wang, Z. Zheng, and L. Xu. "Hierarchical system design and control of an MMC-based power-electronic transformer," *IEEE Trans. Ind. Informat.,* vol. 13, no. 1, pp. 238–247, Feb. 2017.
[10] L. Mathe, P.D. Burlacu, and R. Teodorescu. "Control of a modular multilevel converter with reduced internal data exchange," *IEEE Trans. Ind. Informat.,* vol. 13, no. 1, pp. 238–247, Feb. 2017.
[11] A. Lesnicar and R. Marquardt.: 'An innovative modular multilevel converter topology suitable for a wide power range', in *Proc. IEEE Power Tech. Conference*, vol. 3, Bologna, June 2003.
[12] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed , and B. W. Williams, "Hybrid and modular multilevel converter designs for isolated HVDC–DC converters," *IEEE Journal of Emerging and Selected Topics in Power Electron*., vol. 6, no. 1, pp. 188-202, Mar. 2018.
[13] R. Zeng, L. Xu, L. Yao, and S. J. Finney, "Analysis and control of modular multilevel converters under asymmetric arm impedance conditions," *IEEE Trans. Ind. Electron*., vol. 63, no. 1, pp. 71–81, Jan. 2016.
[14] C. A. Rojas, S. Kouro, M. A. Perez and J. Echeverria, "DC-DC MMC for HVdc grid interface of utility-scale photovoltaic conversion systems, *IEEE Trans. Ind. Electron*., vol. 65, no. 1, pp. 352 – 362, Jan. 2018
[15] Q. Sun, Y. Wei, Y. Wang, at el, "Optimized control strategy of modular multilevel DC transformer for high-frequency-link voltages matching in the whole operation range," *IEEE Journal of Emerging and Selected Topics in Power Electron*. early access.
[16] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales and Y. R. de Novaes, " Isolated DC/DC structure based on modular multilevel converter," *IEEE Trans. Power Electron*., vol. 30, no. 1, pp. 89-98, Jan. 2015.
[17] B. Zhao, Q. Song, J. Li, Y. Wang and W. Liu, "High-frequency-link modulation methodology of DC-DC transformer based on modular multilevel converter for HVDC application: comprehensive analysis and experimental verification," *IEEE Trans. Power Electron*., vol. 32, no. 5, pp. 3413– 3424, May 2017.
[18] C. Sun, J. Zhang, X. Cai, and G..Shi. "Analysis and arm voltage control of isolated modular multilevel DC – DC converter with asymmetric branch impedance," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 5978-5990, Aug. 2017.
[19] A. K. Jain and R. Ayyanar, "PWM control of dual active bridge: comprehensive analysis and experimental verification," *IEEE Trans. Power Electron*., vol. 26, no. 4, pp. 1215-1227, Apr. 2011.
[20] P. Zumel, L. Ortega, A. Lázaro, A. Barrado, A. Rodríguez, and M. María Hernando, "Modular dual-active bridge converter architecture," *IEEE Trans. Ind. App*., vol. 52, no. 3, pp. 2444-2455, May/Jun 2016.
[21] S. P. Engel, M. Stieneker, N. Soltau, S. Rabiee, H. Stagge and R. W. De Doncker, "Comparison of the modular multilevel DC converter and the dual-active-bridge converter for power conversion in HVDC and MVDC Grids," *IEEE Trans. Power Electron*., vol. 30, no. 1, pp. 124–137, Jan. 2015.
[22] B. Zhao, X. Li, Y. Wei, et al, "Modular hybrid-full-bridge DC transformer with full-process matching switching strategy for MVDC power distribution application," *IEEE Trans. Ind. Electron*., 2019, early access.
[23] B. Zhao, Q. Song, J. Li, and W. Liu, "A modular-multilevel-dc-link front-to-front dc solid state transformer based on high-frequency dual active phase-shift for HVDC grid integration," *IEEE Trans. Industrial Electronics.* , vol. 64, no. 11, pp. 8919–8927, Nov. 2017.
[24] G. G. Oggier, G. O. Garcia, and A. R. Oliva, "Switching control strategy to minimize dual active bridge converter losses," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1826–1838, Jul. 2009.
[25] S. Inoue and H. Akagi, "A bidirectional isolated DC-DC converter for an energy storage system with galvanic isolation," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2299–2306, Nov. 2007.
[26] W. A. Roshen, "A practical, accurate and very general core loss model for nonsinusoidal waveforms," *IEEE Trans. Power Electron.*, vol. 22, no. 1,pp. 30–40, Jan. 2007.

**Qianhao Sun** was born in Shanxi, China in 1993. He received the B.S. degree in Electrical Engineering from Northeast Electric Power University, Jilin, China, in 2014, and M.S. degree in Electrical Engineering from Tsinghua University, Beijing, China, in 2017, where he is currently pursuing the Ph.D. degree in Electrical Engineering. From May to November, 2019, he has been a visiting Ph.D. student at Cardiff University, Cardiff, UK.

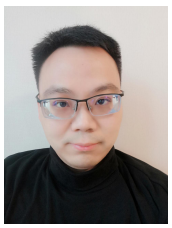
His current research interests include the high-frequency dc-dc converter and flexible dc transmission and distribution system.

**Yalou Li** was born in Henan, China in 1974. He received the B.S. degree in Electrical Engineering from Huazhong University of Science and Technology, Wuhan, China, in 1997, and the M.S. and Ph.D. degrees in Electrical Engineering from the China Electric Power Research Institute in 2000 and 2003, respectively.

He is currently a Chief Engineer in the Power System Department, China Electric Power Research Institute, Beijing, China. His current research interests include the AC and DC power system and key devices digital simulation, analysis and control.

**Xiaolin Shen** was born in Shanxi, China, in 1985. He received the B.S. degree in Electrical Engineering from North China Electric Power University, Beijing, China, in 2008, and M.S. degree in Electrical Engineering from Tsinghua University, Beijing, China, in 2011. He is currently an engineer in State Grid Economic and Technological Research Institute, Beijing, China.

His main research interests are in HVDC transmission system and DC transmission equipment.



**Fan cheng** received the B.S. degree in electric engineering and automation from South China University of Technology, Guangzhou, Guangdong province, China in 2014 and the M.Eng. degree in electric engineering from Southeast University, Nanjing, Jiangsu province, China, in 2010. He is currently pursuing the Ph.Eng. degree in electric engineering at China electric power research institute, Beijing, China.

His research interest includes the high voltage direct current technology based on power electronic, large scale renewable

energy integration and interaction stability analysis of electronic power system.

**Gen Li** (M'18) received the B.Eng. degree from Northeast Electric Power University, Jilin, China, in 2011, the M.Sc. degree from Nanyang Technological University, Singapore, in 2013 and the Ph.D. degree from Cardiff University, Cardiff, U.K., in 2018.

From 2013 to 2016, he was a Marie Curie Early Stage Research Fellow funded by the European Union's MEDOW project. He has been a Visiting Researcher at China Electric Power Research Institute and Global Energy Interconnection Research Institute, Beijing, China, at Elia, Brussels, Belgium and at Toshiba International (Europe), London, U.K.. He has been a Research Associate at the School of Engineering, Cardiff University since 2017. His Ph.D. thesis received the First CIGRE Thesis Award in 2018. He is a Chartered Engineer in the UK. He is an Associate Editor of the CSEE Journal of Power and Energy Systems. His research interests include control and protection of HVDC and MVDC technologies, power electronics, reliability modelling and evaluation of power electronics systems.

**Jun Liang** (M'02-SM'12) received the B.Sc. degree from Huazhong University of Science and Technology, Wuhan, China, in 1992 and the M.Sc. and Ph.D. degrees from the China Electric Power Research Institute (CEPRI), Beijing, in 1995 and 1998, respectively.

From 1998 to 2001, he was a Senior Engineer with CEPRI. From 2001 to 2005, he was a Research Associate with Imperial College London, U.K.. From 2005 to 2007, he was with the University of Glamorgan as a Senior Lecturer. Currently, he is a Professor at the School of Engineering, Cardiff University, Cardiff, U.K.. He is a Fellow of the Institution of Engineering and Technology (IET). He is the Chair of IEEE UK and Ireland Power Electronics Chapter. He is an Editorial Board Member of CSEE JPES. He is the Coordinator and Scientist-in-Charge of two EC Marie-Curie Action ITN/ETN projects: MEDOW (€3.9M) and InnoDC (€3.9M). His research interests include HVDC, MVDC, FACTS, power system stability control, power electronics, and renewable power generation.

**Mu Qing** was born in Changzhou, China, in 1983. He received his B.Sc. degree in Automatic Control from the Institute of Electrical Engineering, Zhejiang University, Hangzhou, China, in 2005 and his M.Sc. and Ph.D. degrees from the China Electric Power Research Institute, Beijing, China, in 2010 and 2013, respectively.

He is currently an engineer with the power system department of the China Electrical Power Research Institute. His research interests include power systems, HVDC, renewable energy generation.

**Jingwei Meng** was born in Liaoning, China in 1990. He received the B.S. degree from the Department of Electrical Engineering, Tianjin University, Tianjin, China, in 2015, and the M.S. degrees from the Department of Electrical Engineering, Tsinghua University, Beijing, China, in 2018, where he is currently pursuing the Ph.D. degree in electrical engineering.

His current research interest is VSC-HVDC system.