Behavioral Models of I/O Ports from Measured Transient Waveforms

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Igor S. Stievano, *Member, IEEE*, Ivan A. Maio, *Member, IEEE*, and Flavio G. Canavero, *Senior Member, IEEE*

***Abstract*—This paper addresses the development of accurate and efficient behavioral models of digital integrated circuit ports from measured transient responses. The proposed approach is based on the estimation of parametric models from port voltage and current waveforms. The modeling process is described and applied to the modeling of output ports. Its feasibility is demonstrated by the identification of a real device from actual measurements, and by the comparison of the predicted device response with the measured one.**

***Index Terms*—Circuit modeling, digital integrated circuits, electromagnetic compatibility, I/O ports, macromodeling, radial basis function models, signal integrity, system identification.**

I. Introduction

EXTENDED band behavioral models of digital integrated circuit (IC) ports are key elements for the simulation of sensitive signal integrity (SI) and electromagnetic compatibility (EMC) effects in fast digital circuits. The most common approach to behavioral modeling of IC ports is via simplified equivalent circuits, because they allow physical insight and facilitate the implementation of models. An important example of the equivalent circuit approach to behavioral modeling is the widely adopted input/output buffer information specification (IBIS) [1]. IBIS offers high numerical efficiency, large data library and commercial software tools handling models and complex modeling problems.

The equivalent circuit approach to behavioral modeling, however, has also inherent limitations. In fact, the estimation of model parameters is readily done by means of virtual measurements only (i.e., if the transistor-level model of the device is available). In addition, the circuit structure defining the model decides *a-priori* the physical effects to be considered, leaving no possibilities to reproduce other effects inherent to a specific device.

An alternative approach to behavioral modeling of IC ports is their identification by means of nonlinear dynamic parametric models. In this approach, the parameters of a suitable model are estimated from the voltage and current waveforms measured at the device ports. The modeled device is considered as a black-box, i.e., in principle, no knowledge of the internal structure is required and the modeling information is completely contained in the device external responses. Owing to this feature, parametric models can be effectively estimated from measured transient responses or from simulated responses computed for detailed reference transistor-level models. Besides, since the structure of the parametric models is partially selected by the identification process itself, they automatically include all significant physical effects relating input and output waveforms.

In this paper, we shortly review the modeling of IC ports via the identification approach and apply it to the modeling of an IC output port from measured transient waveforms, thereby demonstrating the feasibility and advantages of the method. The process for the construction of IC port parametric models is outlined in Section II, and the modeling example involving a real device is described in Section III.

Manuscript received May 29, 2001; revised June 10, 2002.

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Digital Object Identifier 10.1109/TIM.2002.808019

II. Modeling Process

Since in system level SI and EMC simulations, the aim is the prediction of signals on board and on cables, for a specified logic activity of their drivers, the internal operation of ICs is neglected. Thus, the device ports act as receivers or signal pattern generators loading the interconnect. The required IC models, therefore, are relations between the voltages and the currents of the IC ports for a known internal logical activity. The generic model is a constitutive relation of the form

$$i(t) = F(v(t), w(t)) \tag{1}$$

where $i(t)$ and $v(t)$ are the port current and voltage, respectively, F is a nonlinear dynamic operator and $w(t)$ is an extra input needed to specify the port transitions.

In the identification approach addressed in this paper, the operator F in (1) is a (discrete-time) nonlinear parametric model, and its construction relies on the well-established theory of system identification [2]. For the problem at hand, the complete modeling process can be divided into three parts: A) the selection of a suitable parametric model; B) the estimation of the model parameters; C) the implementation of the model as a subcircuit of a circuit simulation environment. In this section, the above modeling process is detailed for the general case of output ports. Input ports can be handled by a simplified version of the process for output ports, and are explicitly addressed in [3].

A. Model Selection

The structure of a generic output port is shown in Fig. 1, where $\overline{v}$ is the buffer input voltage (i.e., the output of the functional part of the IC), $\overline{v}_\ell$ is the input of the last inverter stage, v and i are the voltage and current at the buffer output pin, respectively, and V_{dd} and V_{ss} are the power supply voltages (assumed constant in this paper). The external behavior of this structure can be described by a constitutive relation of the form

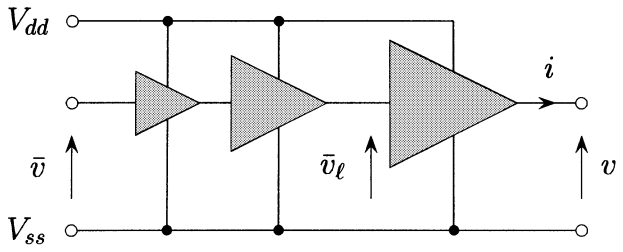

Fig. 1. Generic multistage output buffer and its relevant electric variables.

$i = F(v, \overline{v}_\ell)$, i.e., $\overline{v}_\ell$ is used as w of (1). Several parametric models (or, more properly, several model representations) can be exploited to represent the above F operator (e.g., see [4] for a comprehensive overview of nonlinear parametric models used in system theory, neural networks and other technical areas). For typical output ports of CMOS devices, we obtain good results by using Gaussian radial basis function (RBF) model representations [4]. This choice leads to accurate and simple models, that can be easily implemented in circuit simulators and whose parameters are readily estimated by standard algorithms [5], [6].

The construction of two input models, however, requires the knowledge of some internal variable, like $\overline{v}_\ell$, that is not directly measurable. In order to be able to estimate the model from external measured transient waveforms only, we use a two-piece model representation, where the change of logic state is described by the switching between the two submodels.

Such a representation is

$$i(k) = w_1(k)i_1(k) + w_2(k)i_2(k) \tag{2}$$

where $i(k)$ is the sampled output current waveform [$i(k) = i(t = kT)$, T being the sampling time], $w_1(k)$ and $w_2(k)$ are time-varying weight sequences for state switchings, and submodels $i_1(k)$ and $i_2(k)$ are RBF parametric models accounting for the port behavior in the High and in the Low logic states, respectively. Submodels $i_n(k)$, $n = 1, 2$ are defined by [4]

$$\begin{aligned} i_n(k) &= f_n(\mathbf{\Theta}_n, \mathbf{x}_n(k)) \\ &= \sum_j \alpha_{nj} \exp\{-(\mathbf{x}_n(k)-\mathbf{c}_{nj})^T(\mathbf{x}_n(k)-\mathbf{c}_{nj})/(2\beta_n^2)\} \\ \mathbf{x}_n(k) &= [i_n(k-1), \ldots, i_n(k-r), v(k), \ldots, v(k-r)]^T \\ \mathbf{\Theta}_n &= [\alpha_{n1}, \ldots, \mathbf{c}_{n1}^T, \ldots, \beta_n]^T \end{aligned} \tag{3}$$

where r is the dynamic order of the model, and vector $\mathbf{\Theta}_n$ collects the unknown submodel parameters.

It can be shown that this time-varying two-piece representation arises as an approximation of a single-piece time-invariant RBF model predicting the output current i as a function of the evolution of v and of the (not measurable) input voltage $\overline{v}_\ell$ [3]. Model (2), however, can be estimated simply from $v(t)$ and $i(t)$ transient waveforms and inherits most of the strengths of the mentioned single-piece RBF model. Its estimation is easy and, even with few basis functions (e.g., [5, 20]), estimated models track accurately the behavior of most output buffer circuits. Moreover, since the single-piece RBF model holds for arbitrary loads, the accuracy of the two-piece model turns out to be fairly insensitive to the loads it drives. Of course, such a simplified model holds only for logic state transitions spaced enough in time, so that every new transition starts after the previous one has been completed. However, since the above validity condition is satisfied in properly working digital circuits, it does not limit the use of the model in EMC simulation problems.

B. Parameter Estimation

This subsection describes the estimation of the parameters of model (2), i.e., the parameter vectors $\mathbf{\Theta}_1$ and $\mathbf{\Theta}_2$ of submodels i_1 and i_2, respectively, the dynamic order r, and the weight coefficients w_1 and w_2.

The vector of parameters $\mathbf{\Theta}_n$, $n = 1, 2$ defining the RBF submodels i_n, is computed from a set of port transient voltage and current waveforms (named identification signals) by means of a suitable estimation algorithm [5], [6]. According to the definition of i_1 (i_2), its identification signals should be obtained by forcing the port in the high (low) logic state and by recording the port current response (submodel output) to a voltage signal (submodel input). The design of the input identification signal, i.e., the voltage signal stimulating the output port, is a key point of the modeling process. Such a signal should be able to excite every possible dynamic behavior of the modeled port taking place in the frequency bandwidth and in the current and voltage ranges of interest [2]. For linear systems, this is accomplished by using white noise or pseudorandom binary signals as input identification signals. For nonlinear systems, instead, only qualitative guidelines are available for the design of input identification signals, leading to noisy multilevel signals. Taking into account that the input identification waveform must be obtained in a real measurement setup, we look for the simplest input identification signal ensuring successful estimation. Our optimum choices are voltage waveforms composed of three to six level transitions spanning the range of operation voltages, i.e., [$V_{ss} - \Delta$, $V_{dd}+\Delta$], where Δ is the accepted overvoltage. The flat parts of the waveform should last enough time to allow the port to reach steady-state operation, whereas the edges are linear and have rise/fall times comparable to the switching times of the port.

Once the identification signals have been obtained, the estimation of the model parameters requires the knowledge of the model dynamic order r, that defines the size of the regressor vectors of (3). The dynamic order is an inherent property of the modeled system, and it should be estimated *a-priori* directly from the system response [7]. We carried out *a-priori* dynamic order estimations for several example CMOS output ports, and we always found r values in the range 1–2. This means that, for practical purposes, models can be estimated by postulating the value of r, and the accuracy of the estimated models indicates whether or not the assumed r value is sufficient.

For a given r value, we estimate the parameters of i_n submodels by means of the algorithms of [5], [6]. The algorithms are based on the observation that, for known positions (centers $\mathbf{c}_{nj}$) and spreadings (scale parameters β_n) of the basis functions composing the model, the linear coefficients α_{nj} are the solutions of a standard least square problem. In order to estimate the centers, every point explored by the regressor vector $\mathbf{x}_n(k)$ is considered as a possible center $\mathbf{c}_{nj}$, and the common scale parameter β_n is preset to a value ensuring a good overlapping of all

basis functions. Then, for models composed of $p = 1, 2, 3\cdots$ basis functions, the following steps are repeated:

- a model with p functions is built by adding a new basis function to the model with $p-1$ functions; the center of the added basis function is the point $\mathbf{x}_n(k)$ giving rise to the largest decrease of the model fitting error;
- the statistical significance of the new model is assessed by computing suitable statistical indexes, and the process is terminated when the most significant model is reached.

In [6], the estimation process is improved by allowing for the elimination of basis functions already included in the model. The estimation of submodels i_1 and i_2 by means of such algorithms is very efficient; it takes a few seconds on a Pentium PC to estimate submodels with some tens of radial basis functions.

As a last step of the estimation process, the weight coefficients w_1 and w_2 are obtained from a set of switching experiments by linear inversion of (2), i.e.

$$\begin{bmatrix} w_1(k) \\ w_2(k) \end{bmatrix} = \begin{bmatrix} i_1(k) & i_2(k) \\ i_1(k) & i_2(k) \end{bmatrix}^{-1} \begin{bmatrix} i_a(k) \\ i_b(k) \end{bmatrix} \tag{4}$$

where waveforms $\{i_a, v_a\}$ and $\{i_b, v_b\}$ are switching signals recorded while the output port drives two different loads [load (a) and load (b)] and complete state switchings are caused by variations of the logic input.

In principle, there are no restrictions on load (a) and load (b), which can also be real sources stimulating the output port. The best loads would be those allowing $\{i_a, v_a\}$ and $\{i_b, v_b\}$ to explore the widest possible region of the v–i plane. We use the same loads recommended by IBIS to characterize port switchings, i.e., load (a) is a resistor and load (b) is a series connection of a resistor and a V_{dd} battery. Within the class of resistive loads, it can be proven that this is the best possible choice.

C. SPICE Implementation

The last part of the modeling process is the synthesis of the estimated discrete-time model defined by (2) and (3) as an equivalent circuit to be implemented in standard simulation environments. This synthesis is carried out by converting the discrete-time model into a continuous-time state-space representation and by replacing the state equations with their equivalent circuits. Such a process is detailed below.

Submodels $i_n(k)$, $n = 1, 2$ in (3) are rewritten in the following discrete-time state-space form

$$\begin{cases} \mathbf{y}_n(k) - \mathbf{y}_n(k-1) &= \mathbf{A}_r \mathbf{y}_n(k-1) + \mathbf{e}_r i_n(k-1) \\ \mathbf{z}(k) - \mathbf{z}(k-1) &= \mathbf{A}_r \mathbf{z}(k-1) + \mathbf{e}_r v(k-1) \\ i_n(k) &= f_n(\mathbf{\Theta}_n, \mathbf{x}_n(k)) \end{cases} \tag{5}$$

where $\mathbf{x}_n(k) = [\mathbf{y}_n^T(k), v(k), \mathbf{z}^T(k)]^T$, $\mathbf{e}_r$ is the $r \times 1$ matrix $\mathbf{e}_r = [1, 0, \ldots, 0]^T$ and $\mathbf{A}_r$ is the $r \times r$ matrix

$$\mathbf{A}_r = \begin{bmatrix} -1 & 0 & \cdots & 0 \\ 1 & -1 & \cdots & 0 \\ \vdots & \ddots & \ddots & \vdots \\ 0 & \cdots & 1 & -1 \end{bmatrix}.$$

Then, the continuous-time variable t is replaced in (5) and (2). This is achieved by approximating the difference operator in (5) with the differential one (e.g., $\dot{z}(t) \simeq (1/T)[z(k) - z(k-1)]$). In such a way, the following continuous-time state-space representation arises:

$$\begin{cases} \dfrac{d}{dt}\mathbf{y}_1(t) &= \dfrac{1}{T}\mathbf{A}_r \mathbf{y}_1(t) + \dfrac{1}{T}\mathbf{e}_r f_1(\mathbf{\Theta}_1, \mathbf{x}_1(t)) \\ \dfrac{d}{dt}\mathbf{y}_2(t) &= \dfrac{1}{T}\mathbf{A}_r \mathbf{y}_2(t) + \dfrac{1}{T}\mathbf{e}_r f_2(\mathbf{\Theta}_1, \mathbf{x}_2(t)) \\ \dfrac{d}{dt}\mathbf{z}(t) &= \dfrac{1}{T}\mathbf{A}_r \mathbf{z}(t) + \dfrac{1}{T}\mathbf{e}_r v(t) \\ i(t) &= w_1(t) f_1(\mathbf{\Theta}_1, \mathbf{x}_1(t)) + w_2(t) f_2(\mathbf{\Theta}_2, \mathbf{x}_2(t)). \end{cases} \tag{6}$$

Finally, the first three rows in (6), defining the state equations, are synthesized by means of RC circuits with controlled sources, and the output equation, i.e., the last one, is simply synthesized as a current controlled source.

III. Modeling Example

The proposed approach has been tuned by applying it to the modeling of several virtual devices, that are either transistor-level models of typical CMOS output buffers [8], or transistor-level models of commercial drivers and receivers [3], [9]. In order to verify its practical feasibility, i.e., that measurement errors and noise do not prevent its application to measured data, we verify it on a real device: the output port of a NAND gate of an HC7400 IC connected as inverter, i.e., our device under modeling (DUM). Such a device is both sufficiently simple and representative to be an easy and significant test case.

In this example, the identification signals for the estimation of model (2) are excited and measured by means of the test fixture shown in Fig. 2. The equivalent circuit used to describe the test fixture is shown in Fig. 3. In this equivalent, DUM represents the port being modeled, R_s the SMD resistor of Fig. 2, terminal T is the pin of the port being modeled, and T_1 and T_2 are the input and output terminals used to stimulate the circuit via sources S_1 and S_2, respectively. Terminals T and T_2 are connected to SMA connectors on the back of the board of Fig. 2, that are used to inject the signals of source S_2 and to connect scope probes. The scope probes detect the voltage waveforms $v(t)$ and $v_2(t)$, and their presence is taken into account by the shunt capacitors C_p.

The identification signals described in Section II-B are generated as follows. The port responses $v(t)$ and $i(t)$ are obtained from the voltages recorded via the probes connected to terminals T and T_2. The scope is a Tektronix TDS380 with 400 MHz bandwidth (2 Gs/s sampling rate), and the probes are passive voltage probes P6114B (attenuation factor 10×, input resistance 10 MΩ, nominal value of the parasitic capacitance 14.1 pF). Current $i(t)$ is indirectly obtained from the voltage drop on the SMD series resistor R_s (see Fig. 3) as

$$i(t) = C_p\, dv(t)/dt + [v(t) - v_2(t)]/R_s.$$

In this application, the port switching times are sufficiently slow to allow the modeling of the SMD resistor by means of the ideal element R_s. However, an accurate characterization of the SMD

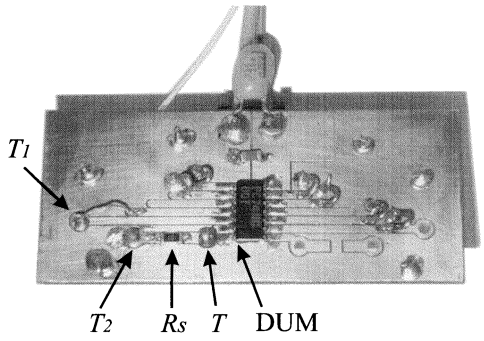

Fig. 2. Test fixture for the experimental characterization of the output port of the HC7400 IC. The DUM is the port being modeled, R_s is the SMD resistor, and T, T_1 and T_2 are the terminals shown in the equivalent circuit of Fig. 3.

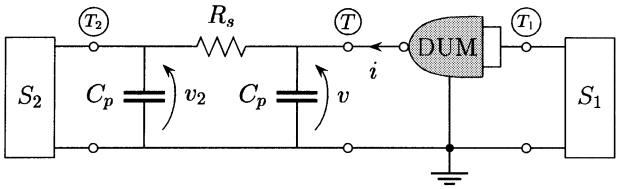

Fig. 3. Equivalent circuit of the identification setup. $R_s = 100\ \Omega$ and $C_p = 14.1$ pF represent the SMD resistor and the passive voltage probe, respectively. S_1 and S_2 are the sources of the identification signals.

resistor by means of a network analyzer is needed for devices that exhibit faster transition times.

The identification signals for the estimation of the RBF submodels i_1 and i_2 are generated by using a multifunction waveform synthesizer connected as S_2 while the port being modeled is set, via the source S_1, to either the High or the Low logic output state. The generator S_2 is tuned to obtain a voltage waveform $v(t)$ with the required shape, i.e., a multilevel waveform spanning the range of possible operating voltages. As an example, the identification signals for submodel i_2 obtained in this way are shown in Fig. 4. The waveform generator to excite such signals is not a critical element. In this setup, the block S_2 producing the waveform of Fig. 4 is a Rhode and Schwarz AFS multifunction generator connected to a suitable stub element (i.e., a 2–6 m long RG58 cable) and generating a 20-MHz square wave with adequate duty-cycle, offset and amplitude. In a setup for routine measurements, the waveform generator could be provided by a dedicated circuit composed of discrete logic gates.

As a second step, the switching signals for the estimation of weight coefficients w_1 and w_2, are obtained by replacing S_2 with a 50-Ω coax resistor and with a 60-Ω carbon resistor connected to V_{dd} as load (a) and load (b), respectively, and by driving (via S_1) the port to produce a high pulse. Fig. 5 shows the identification signals for the above switching experiment obtained while the port is connected to load (a).

It is worth noting that an accurate characterization of loads and instruments (block S_2 in the setup of Fig. 3) is not needed. Once S_2 is tuned to produce the desired shape of the port voltage waveform $v(t)$, the port current waveform $i(t)$ required for the estimation process can be accurately measured by means of the voltage drop on the series resistor R_s, only.

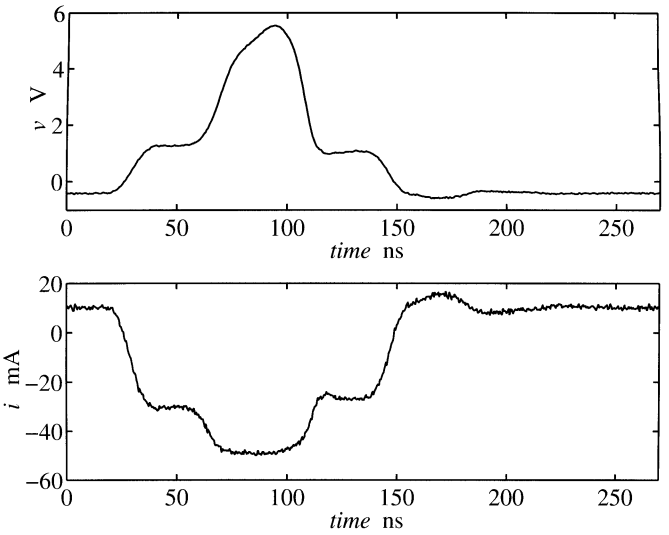

Fig. 4. Measured switching identification signals $v(t)$ and $i(t)$ for the estimation of submodel i_2.

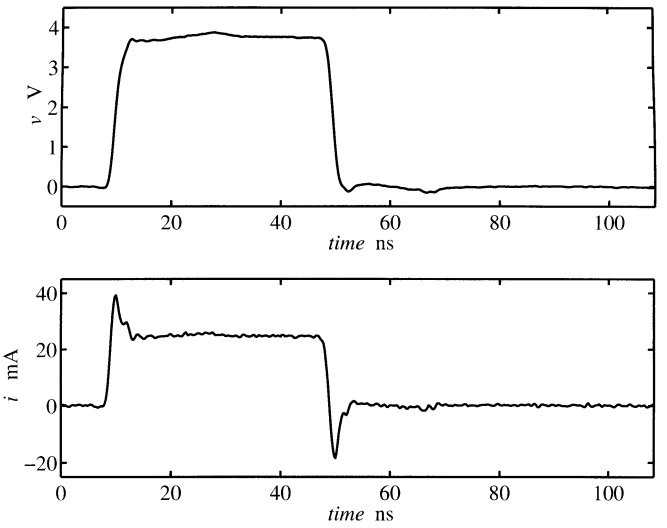

Fig. 5. Measured identification signals for the estimation of weight coefficients w_1 and w_2 while the port is connected to load (a), i.e., the series connection of $R_s = 100\ \Omega$ and a 50 Ω coax resistor.

The recorded identification signals are sampled by a sampling period $T = 200$ ps (1350 samples) and are processed by the estimation algorithm [6] to compute the submodel parameters $\boldsymbol{\Theta}_n$, $n = 1, 2$. Then the weight coefficients are computed by using the switching signals and the estimated submodels i_n, $n = 1, 2$ as explained in Section II-B. For this example, model (2) is estimated in some tens of seconds on a Pentium II PC, and its submodels turn out to have dynamic order one ($r = 1$) and five basis functions each. The model is implemented as a SPICE subcircuit by the procedure described in Section II-C and is validated by predicting the responses of test circuits different from those involved in the generation of the identification signals.

As an example, Fig. 6 shows the measured and the predicted responses of the modeled port when it sends a pulse on the series connection of R_s and an open-ended RG58 coaxial cable. The accuracy of the model is clearly appreciable. In all tests carried out, the model turns out to accurately reproduce both

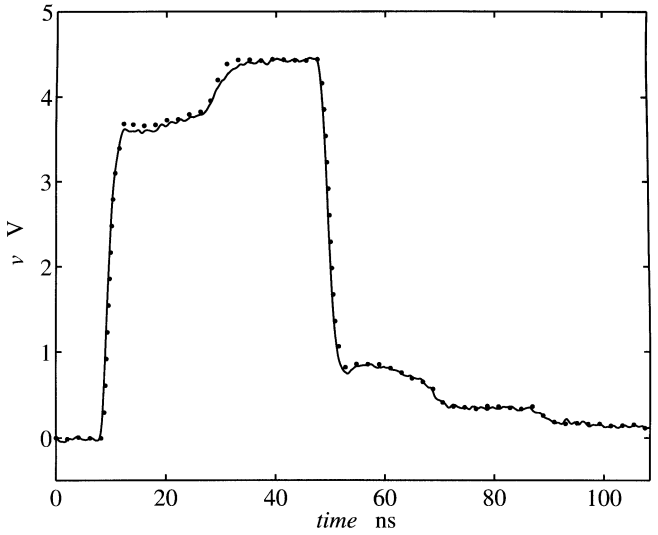

Fig. 6. Output voltage waveform of the port being modeled driving a series connection of a 100 Ω resistor and an open-ended 1.5-m long RG58 coaxial cable ($Z_0 = 50\ \Omega$). Solid line: measured reference response; dotted line: response of the two-piece RBF model.

the static (steady-states) and the dynamic (transitions) behavior of the actual port, leading to timing errors always less than the sampling period used in the estimation process. In our tests, the timing error is defined as the maximum delay between the reference and the model responses measured at one-half of the signal swing. These results show that the estimated model performs at a very good accuracy level, even if the measurement of identification signals and the validation are based on a rather idealized equivalent circuit of the test fixture. On the other hand, the structure of the model is simple and has the numerical efficiency required for the simulation of realistic problems.

IV. Conclusion

The behavioral modeling of IC ports via black-box identification leads to simple and reliable models that can be easily included in a standard simulation environment. Identification methods provide a rigorous framework to handle the problem, and the proposed procedure indeed enables final users to build their own IC models from actual measurements. In conclusion, the black-box approach could be a useful complement to the conventional circuit-oriented ones for the development of models to be used in the simulation of EMC and SI problems.

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