Effective and Economic Phase Noise Testing for Single-Chip TV Tuners

James Chien-Mo Li, Po-Chou Lin, Chih-Ming Chiang, Chuo-Jan Pan, and Chao-Wen Tseng

***Abstract*—Phase noise testing for TV tuners is time consuming and expensive because of the large number of TV channels. This paper presents a hierarchical simulation method for a complex single-chip TV tuner. Based on the simulation results, an effective and economic test method is proposed to save the test application time. This method determines the most effective channels and frequencies to test so that the number of phase noise measurements is reduced. Experimental results on commercial chips show that our proposed method reduces the test time by a factor of ten without test escapes.**

***Index Terms*—Phase lock loops (PLLs), phase noise, RF testing, tuner, TV channels.**

I. Introduction

A TV TUNER is an RF front-end component key to all TV systems and has two major functions: 1) channel selection and 2) frequency conversion. Fig. 1 shows a block diagram of a simplified TV system. Channel selection means the selection of one of approximately 150 channels in total. Each is 6 MHz in bandwidth; thus, the input RF signal bandwidth is on the average about 900 MHz (ranging from 48 MHz to 1 GHz). In frequency conversion, the RF signal of the selected channel is converted to the 44-MHz intermediate frequency (IF). The IF signal is then processed by the digital baseband IC to produce videos on the screen. TV tuners used to consist of discrete components. Single-chip TV tuners, which are much smaller and more power efficient than discrete tuners, are now available for mobile applications thanks to the advance in VLSI technologies.

Phase noise is one of the key parameters that must be measured in a production test. Exhaustive testing of all channels is time consuming due to the large number of TV channels. Specifically, it takes up to 18 s to measure the phase noise of 150 TV channels on automatic test equipment (ATE). Since TV tuners are key components in consumer electronics, test cost and test effectiveness are both important concerns for production tests. Unfortunately, there is very limited past research in TV tuner phase noise testing. A phase noise test solution for the mixed-signal ATE is proposed in [1]. Nam *et al.*'s research proposes to add a delay-line FM demodulator as an extension so that the existing mixed-signal ATE can be used for accurate RF phase noise measurement. Design-for-testability (DFT) techniques for voltage-controlled oscillators (VCOs) are proposed [2]–[4]. Their proposed DFT techniques are usually not suitable for RF circuits, which are very sensitive to the parasitic RLC induced by DFT. A theoretical study of the phase noise can be found in [5]–[7], but none of these papers provides an effective and economic test methodology for production tests.

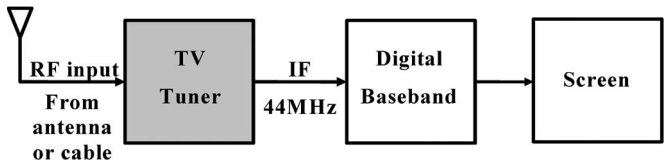

Fig. 1. TV tuner in a system.

This paper proposes a practical simulation and test methodology for a single-chip TV tuner. First, a hierarchical method is presented to avoid the simulation on the whole chip. This hierarchical simulation method is a general approach that can also be applicable to other tuner chips that are too large to be simulated by traditional electronic design automation (EDA) tools. Based on the simulation results, an economic test methodology is presented to test only a small subset of TV channels instead of all channels. The proposed test technique reduces the phase noise test time by a factor of ten. This test methodology can be implemented in a typical production test environment using a regular RF tester. Neither an extra test fixture nor DFT is required. Our test methodology is validated by experimental results on more than 200 commercial TV tuners. The second contribution of this paper is to propose a test methodology that has been insufficient in past research. It has to be noted that no test method guarantees the detection of all defective chips. The best we can do is to reduce the probability of test escapes at a reasonable test cost. Our proposed simulation method provides a mathematical guideline to make a smart decision when reducing the test cost.

The organization of the proposed technique is given as follows. Section II introduces some basic knowledge about the TV tuner and its phase noise. Section III describes the proposed test method in detail. Section IV shows experimental data and discusses related issues of the proposed technique. Finally, Section V concludes this paper.

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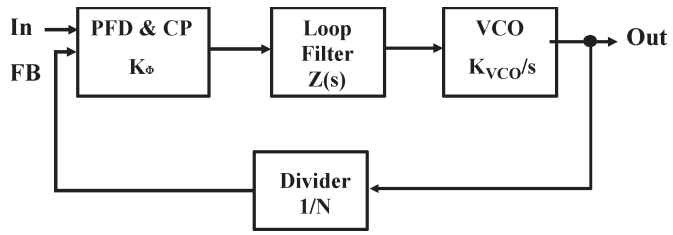

Fig. 2. PLL block diagram.

II. Background

A. Circuit Structure

The key components in a single-chip TV tuner are phase lock loops (PLLs). Frequency conversion is done by mixing the received RF signal with the PLL-generated local oscillation (LO) signals. In this particular TV tuner chip, there are two types of PLL: 1) tunable PLL and 2) fixed PLL. The oscillation frequency of the former is adjustable to select the desired channel; the oscillation frequency of the latter is fixed. Since PLLs are key contributors to the noise of the TV tuner, their structure and behavior have to be studied carefully.

Fig. 2 shows a typical model of PLL. The phase frequency detector (PFD) compares the frequency and phase of the input signal (In) and the feedback signal (FB). The charge pump (CP) transforms the phase error into current. The low-pass filter, which usually consists of resistors and capacitors, is modeled as a transfer function Z(s). The low-pass filter converts the current to voltage and rejects the high-frequency noise to stabilize the closed-loop system. The VCO transforms the voltage into frequency. The divider closes the loop by dividing the output frequency (Out) by N and feeding the divided signal to the PFD.

Equation (1) shows the *open-loop gain* $G(s)$ of the PLL. The PFD and CP are represented by a constant gain K_Φ. The impedance of the loop filter is represented by $Z(s)$, which is a low-pass transfer function. The VCO is considered as a linear time-invariant integrator with transfer function $K_{\rm VCO}/s$. Overall, $G(s)$ is a low-pass transfer function, and its *loop bandwidth* (ω_c) is the frequency where the magnitude of the loop gain is one.

$$G(s) = \frac{K_\Phi \cdot K_{\rm VCO}}{s} \cdot Z(s). \tag{1}$$

Fig. 3 shows a simplified schematic of the *LC* tank VCO, which is a popular implementation of the VCO because of its good phase noise performance. The oscillation frequency (2) is determined by the inductors and the varactor array; the former is fixed, and the latter is adjustable. The varactor array is made up of several identical varactors, each of which is turned on/off by one bit of digital input channel selection signal. By turning on (or off) the varactors, the capacitance is decreased (or increased), and the VCO oscillation frequency is increased (or decreased). The bias negative-channel MOS (NMOS) provides the dc operation current for the VCO. The actual bias circuitry can be more complex than what is shown in the figure.

$$\omega 0 = \frac{1}{\sqrt{L \cdot C}}. \tag{2}$$

B. Phase Noise

An ideal oscillator produces a noise-free single-frequency output, which corresponds to a spike at the center frequency ω_0 in the spectrum. Real oscillators, however, produce noisy output with phase noise, which corresponds to a "skirt" around the carrier spike in the spectrum. For a receiver, the phase noise from the local oscillator causes unwanted signals to be mixed with the desired signal. This phenomenon is known as *reciprocal mixing* [8]. In the case of TV tuners, phase noise is one key factor that determines video quality. The phase noise is usually characterized by a ratio of the noise power over the carrier power. Quantitatively, the phase noise is calculated by dividing the noise power per hertz at an offset frequency $\Delta\omega$ over the power of the carrier, as in (3), shown at the bottom of the page. The phase noise is measured in the unit of decibels relative to the carrier per Hertz (dBc/Hz). For the particular TV tuner under test, it is required that the phase noise of the output signal is lower than -85 dBc/Hz at 10-kHz offset frequency and -100 dBc/Hz at 100-kHz offset frequency, respectively. More details about the phase noise can be found in [8].

Fig. 4 shows an example of the phase noise measured from the output of a good TV tuner. The phase noise is measured by the Agilent 8591C cable TV analyzer. The center frequency is 44 MHz, and the frequency span is ± 10 kHz. It is seen from the picture that the noise power is about 65 dB lower than the signal power. Because the noise power is integrated over an interval of 300 Hz (known as the *resolution bandwidth*), the phase noise at 10-kHz offset is therefore about $(-65) - 10\log[300] = -90$ dBc/Hz, which meets the specification.

1) Open-Loop VCO: The open-loop VCO phase noise can be modeled by the Leeson equation [9]

$$L(\Delta\omega) = \frac{2FkT}{P_{\rm carrier}} \left[1 + \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \left(1 + \frac{\Delta\omega 1/f3}{|\Delta\omega|}\right) \tag{4}$$

where ω_0 is the oscillation center frequency, and $\Delta\omega$ is the offset frequency. The term $P_{\rm carrier}$ represents the carrier power. Fig. 5 shows the spectrum of phase noise calculated by the Leeson equation. At the low offset frequency, the phase noise rolls off at a rate of $1/f^3$ due to the flicker noise. At the medium offset frequency, the phase noise roll off at a rate of $1/f^2$ due to the white thermal noise. At the high offset frequency, the phase noise becomes flat due to nonideal factors such as the

$$\text{PhaseNoise}(\Delta\omega) = 10\log\left[\frac{\text{Noise Power Per Hertz(at offset } \Delta\omega)}{\text{Carrier Power}}\right] \text{ (dBc/Hz)} \tag{3}$$

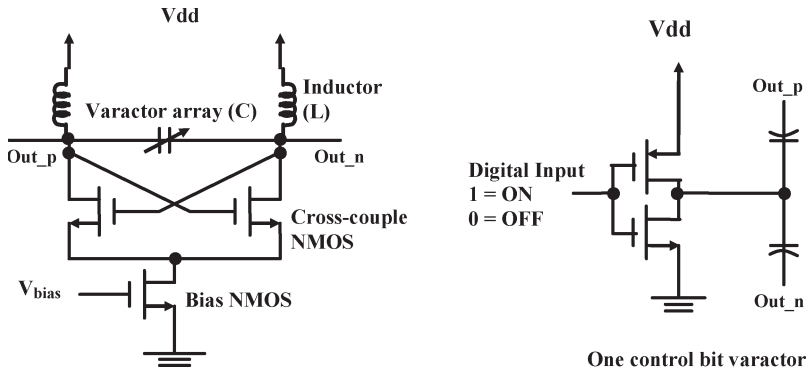

Fig. 3. *LC* tank VCO and varactor.

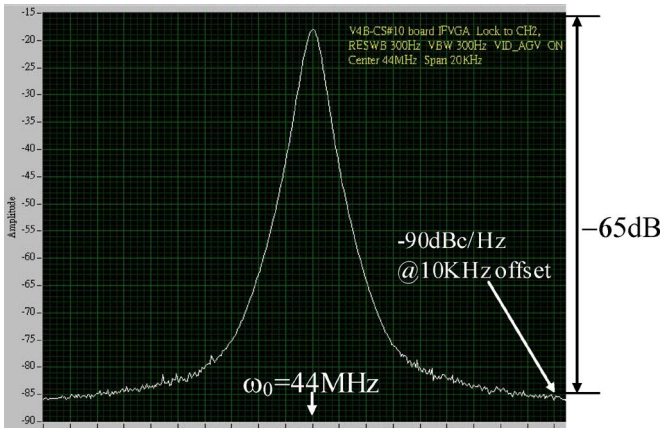

Fig. 4. Phase noise of a TV tuner.

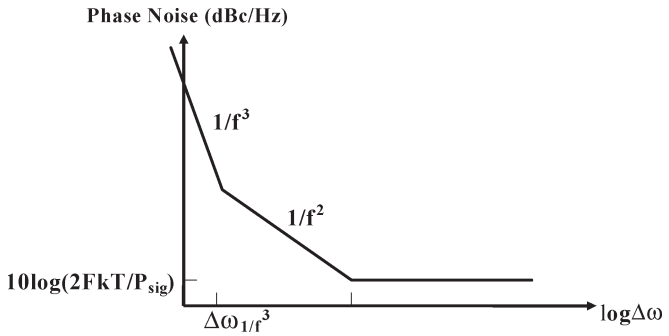

Fig. 5. Phase noise of an open-loop VCO [6].

equipment limitation. The factor F is a fitting parameter that has to be determined by experiment. The $\Delta\omega_{1/f3}$ parameter is the corner frequency of MOS. More accurate models than the Leeson equation have been proposed in the recent literature, such as [6] and [10].

2) Closed-Loop VCO: The phase noise of a closed-loop PLL can be derived from that of an open-loop VCO. Fig. 6 shows a PLL noise mode with two phase noise sources: 1) the VCO noise and 2) the input noise. Equations (5a) and (5b) show the derivation of the transfer function of the VCO noise, where $G(s)$ is the loop gain, and ω_c is the loop bandwidth. Since $N/G(s)$ is small at a low frequency, (5b) is a high-pass transfer function. The VCO noise is suppressed at a low frequency but becomes significant at a high frequency. On the contrary, the

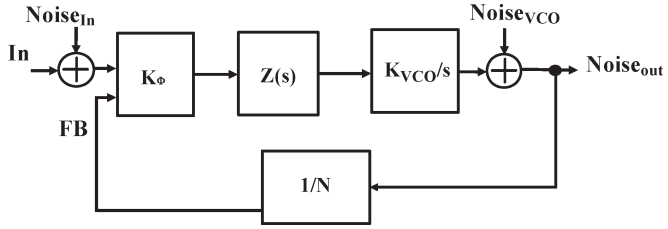

Fig. 6. PLL noise model.

input noise (6) is a low-pass transfer function. The input noise is suppressed at a high frequency but becomes significant at a low frequency. The derivation of (5) and (6) is based on the concept of linear feedback systems. See the books on control systems [11] or PLL [12] for more details.

$$\begin{aligned}\text{Noise}_{\text{out}} &= \text{Noise}_{\text{VCO}} - \text{Noise}_{\text{out}} \\ &\quad \times (K_\Phi \cdot Z(s) \cdot K_{\text{VCO}}/sN) \end{aligned} \tag{5a}$$

$$\begin{aligned}\frac{\text{Noise}_{\text{out}}}{\text{Noise}_{\text{VCO}}} &= \frac{1}{1 + K_\Phi \cdot Z(s) \cdot K_{\text{VCO}}/sN} \\ &= \frac{1}{1 + G(s)/N} \\ &\cong \begin{cases} N/G(s), & \text{for} \quad \omega \ll \omega_c \\ 1, & \text{for} \quad \omega \gg \omega_c \end{cases} \end{aligned} \tag{5b}$$

$$\begin{aligned}\frac{\text{Noise}_{\text{out}}}{\text{Noise}_{\text{in}}} &= \frac{K_\Phi \cdot Z(s) \cdot K_{\text{VCO}}/s}{1 + 1/N \cdot K_\Phi \cdot Z(s) \cdot K_{\text{VCO}}/sN} \\ &= \frac{G(s)}{1 + G(s)/N} \\ &\cong \begin{cases} N, & \text{for} \quad \omega \ll \omega_c \\ G(s), & \text{for} \quad \omega \gg \omega_c. \end{cases} \end{aligned} \tag{6}$$

Table I summarizes the transfer functions of various noise sources. The derivation of the other phase noise is similar to what is shown in (5) and (6). It is observed that only the VCO noise has the high-pass transfer function; all the other noise sources have a low-pass transfer function. Fig. 7 shows

TABLE I
NOISE TRANSFER FUNCTIONS OF VARIOUS NOISE SOURCES

Source	Transfer Function	Characteristic
Reference Input	$\frac{G(s)}{1+G(s)/N}$	Low Pass
N Divider	$\frac{G(s)}{1+G(s)/N}$	Low Pass
Phase Frequency Detector	$K_\Phi \cdot \frac{G(s)}{1+G(s)/N}$	Low Pass
VCO	$\frac{1}{1+G(s)/N}$	High Pass

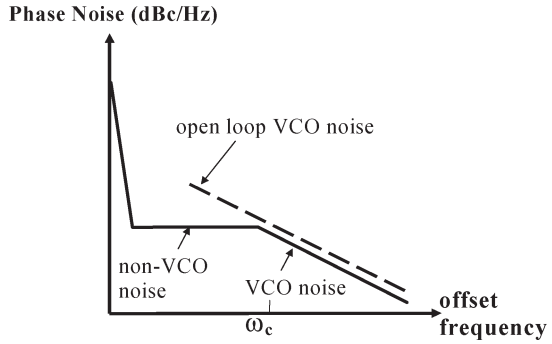

Fig. 7. Phase noise of a closed-loop PLL.

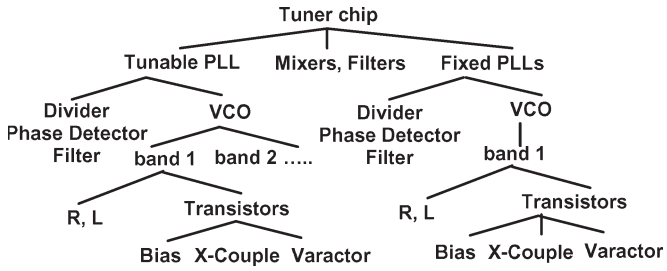

Fig. 8. Hierarchical simulation model.

a conceptual phase noise spectrum of a closed-loop PLL. The dotted straight line is the phase noise of its open-loop VCO. At a low offset frequency, the VCO noise is suppressed, and only non-VCO noise remains. At a high offset frequency, the PLL phase noise is dominated by the VCO phase noise, which decays with the offset frequency. Note that this figure is not drawn to scale for clarity. See other publications for more details about the closed-loop PLL phase noise modeling [7], [13].

III. PROPOSED METHODOLOGY

A. Hierarchical Simulation Method

Simulators based on the Leeson equation are commercially available to simulate a single open-loop VCO. Due to the complexity of the TV tuner chip, however, it is very difficult to perform phase noise simulations on the whole tuner chip. The following hierarchical simulation method is proposed to obtain the phase noise of the tuner chip. Fig. 8 shows the breakdown of phase noise sources of the TV tuner chip. The tuner chip

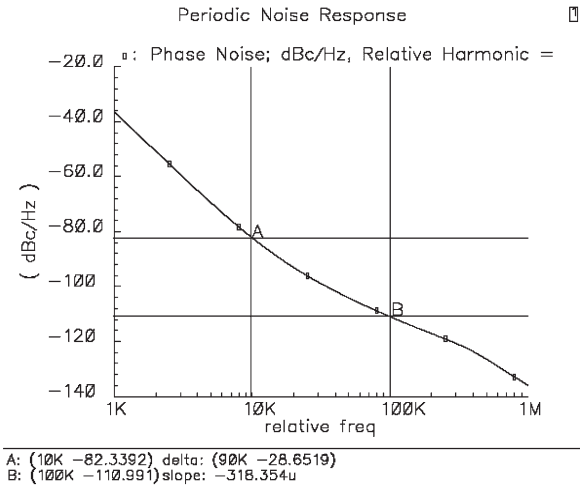

Fig. 9. Phase noise plot.

Device	Param	Noise Contribution	% Of Total
/V7	ext_file_noise	2.29783e-08	84.54
/V13	ext_file_noise	2.62686e-09	9.66
M3.mds	fn	7.3449e-10	2.70
M3.mds	id	1.40537e-10	0.52
M4.mds	id	1.38401e-10	0.51
M4.mds	fn	1.06558e-10	0.39
M5.mds	fn	5.0207e-11	0.18
/R9	rn	1.71709e-11	0.06
/R8	rn	1.64008e-11	0.06

Spot Noise Summary (in V^2/Hz) at 10K Hz Sorted By Noise Contributors
Total Output Noise = 2.71819e-08
No input referred noise available

Fig. 10. Noise summary table.

is composed of a tunable PLL, mixers, and fixed PLLs. Since mixers do not oscillate, their contribution to phase noise is very small and can be ignored. Only the PLLs are considered in the phase noise simulation.

A tunable PLL consists of a frequency divider, a phase detector, a filter, and a VCO. Because of the wide frequency range of input TV channels, the VCO of the tunable PLL is made up of several identical *bands*, each of which is tunable over a relatively small number of TV channels. One VCO band can be further divided into passive devices (such as resistors and inductors) and active devices (transistors). The structure of fixed PLLs is similar to that of the tunable PLL, except that the former has only one band.

The phase noise of the whole tuner is calculated in a bottom-up fashion. The phase noise spectrum of an open-loop VCO is first simulated by a commercial RF simulator. For the tunable PLL, each VCO band has to be separately simulated. Second, the PLL loop bandwidth is determined by an equivalent circuit simulation using the Cadence Virtuoso. The closed-loop PLL phase noise spectrum is obtained by putting together the loop bandwidth and the open-loop VCO phase noise spectrum. Finally, the phase noise of the whole tuner chip is calculated by the convolution of the phase noise spectrum. The details of every step are explained in the following three sections.

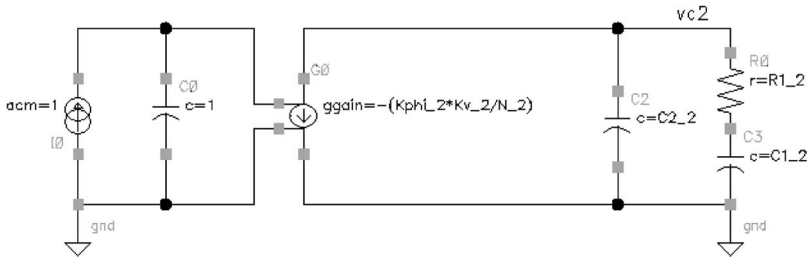

Fig. 11. Simulation of a low-pass filter.

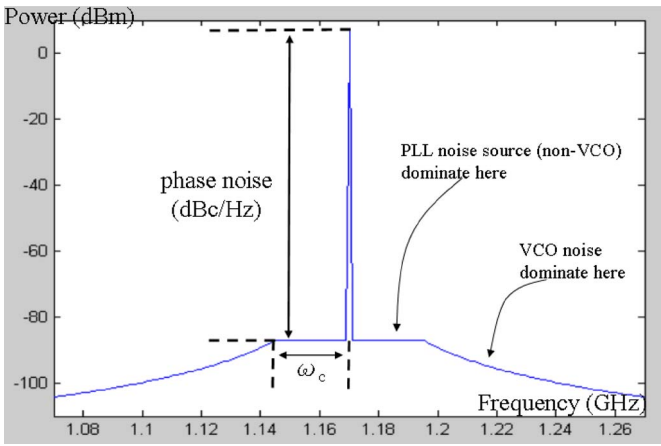

Fig. 12. Phase noise of a closed-loop PLL.

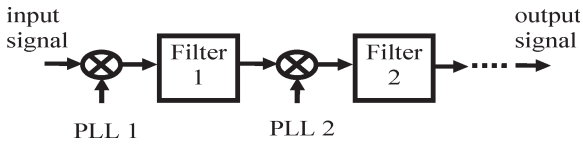

Fig. 13. Tuner chip block diagram.

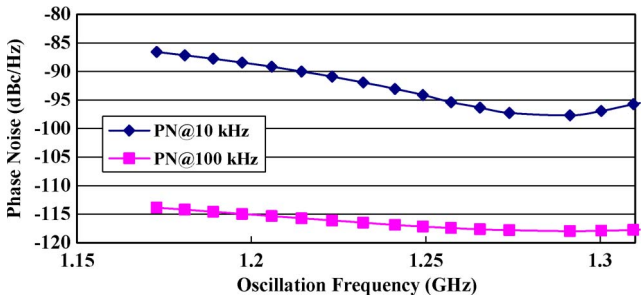

Fig. 14. Phase noise versus frequency (simulation).

1) VCO: The open-loop VCO of each band is simulated by a commercial EDA tool: the Cadence Virtuoso Spectre [Cadence www]. This RF circuit simulator is capable of performing various phase noise analyses. First of all, it produces the phase noise as a function of the offset frequency. A sample phase noise plot is shown in Fig. 9. Second, the noise contribution of every component (such as a transistor and a resistor) is broken down. One example of a noise summary table is shown in Fig. 10. The simulation model is provided by the IC foundry, so the results are accurate and proven by silicon data. However, due to the design complexity, it is not possible to perform a whole-chip simulation using this commercial tool.

2) Closed-Loop PLL: The next step is the simulation of the closed loop for the loop gain and loop bandwidth. Fig. 11 shows the simulation setup for one particular PLL. The PLL is modeled by its equivalent circuit—the loop filter is represented by resistors and capacitors; the other components (PFD, divider, and VCO) are modeled by current sources. Many commercial circuit simulators are available to perform this task, and we choose to use the Cadence Virtuoso [14]. The exact numbers in the design are removed to protect the intellectual property (IP).

Once the loop gain and loop bandwidth is available, we can now calculate the phase noise of the closed-loop PLL. Fig. 12 shows an example of the phase noise of a PLL. The phase noise is dominated by (6) and (5b) for an offset frequency lower and higher than ω_c, respectively. This calculation can be easily done using any mathematical software such as Matlab [15].

3) Whole Chip: Fig. 13 shows the block diagram of the tuner chip, which is a serial connection of mixers and filters. The mixers modulate the input signal by up/down frequency conversion. The filters select the desired video signal by removing the unwanted signal and noise. The mixers and filters are mostly passive devices, so their noise contribution is nearly negligible.

For a linear time-invariant system, mixers can be regarded as a multiplier in the time domain. Therefore, the spectrum of mixer output is obtained by the convolution of the spectrum of two input signals [16]. The convolution can be easily calculated using mathematical software such as Matlab. Because there are multiple stages of mixers, the convolution has to be done in a stage-by-stage manner. Finally, the phase noise of the whole chip is obtained.

B. Determine TV Channels to Test

The most effective TV channels are those channels that have the worst phase noise. Fig. 14 shows the simulation results of one open-loop VCO of the tunable PLL. The x-axis shows the input frequencies that corresponds to the TV channels, and the y-axis shows the phase noise in dBc/Hz. The simulations are performed on two offset frequencies, i.e., 10 kHz and 100 kHz, which are in the product specification of this TV tuner IC.

At first glance, the phase noise in Fig. 14 appears to be inconsistent with the Leeson equation, which predicts that phase noise increases with ω_0. The reason for this mismatch is because we assume a constant VCO output power [P_{carrier} in (2)] over all ω_0, which is not true for this particular VCO

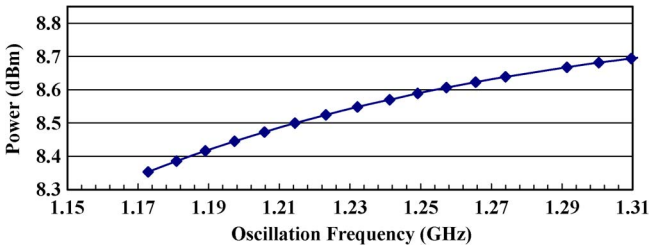

Fig. 15. VCO output power increases with frequency.

TABLE II
PHASE NOISE CONTRIBUTION (CHANNEL C1)

offset	X-couple NMOS	Varactor MOS	Bias	Rest
10 kHz	89.12%	7.10%	2.43%	1.35%
100 kHz	54.92%	33.64%	2.24%	9.16%

design. Fig. 15 shows how the VCO output amplitude increases with the oscillation frequency ω_0. When calculating the closed-loop PLL (Section III-A2), our simulator takes this output amplitude into consideration. Fig. 14 can now be explained by the Leeson equation: Because P_{carrier} becomes larger at a high oscillation frequency, the phase noise actually decreases at a high frequency.

Without our simulator, test engineers would think that testing the *high*-frequency channels is more effective. However, based on our simulation results, it is suggested that testing *low*-frequency channels is more important than testing high-frequency channels because the former has worse phase noise than the latter.

C. Determine Offset Frequencies

Another important decision to make is which offset frequency to test. Initially, 10 kHz and 100 kHz are two possible candidates to measure the phase noise. The first reason for choosing these two particular frequencies is that they are in the specification of the TV tuner chip. Second, phase noise higher than 100 kHz is too low to be accurately measured by the equipment; phase noise lower than 10 kHz is so close to the center frequency that accurate measurement is difficult.

Table II shows the phase noise contribution at 10 kHz and 100 kHz. The phase noise contribution of a component is the percentage of phase noise contributed by that component out of the total phase noise. The noise contribution is provided by the Cadence Virtuoso Spectre (see Section III-A1 and Fig. 10). The simulation is performed on the lowest frequency TV channel, which is referred to as channel C1. From the simulation data, the optimal offset frequency to test the cross-coupled transistors is 10 kHz because they contribute nearly 90% of phase noise at 10 kHz. The phase noise is sensitive to the quality of cross-coupled transistors at 10 kHz. If the cross-coupled transistors are defective, it is easier to detect the abnormal phase noise at 10 kHz. The varactor transistors, on the contrary, should be tested at 100 kHz because their noise contribution at 100 kHz is nearly five times higher than that at 10 kHz. The bias transistors are relatively insensitive to the offset frequency because their contributions are relatively constant for two offset frequencies. Other than transistors, the remaining components (such as resistors and inductors) of the VCO contribute a relatively small percentage of phase noise, and therefore, they are not broken down into details. From the simulation results, it is suggested that both 10-kHz and 100-kHz measurements are needed because they are effective for different groups of transistors. Although no offset frequencies can be skipped, the simulation results provide a good understanding of the relationship between the phase noise and the circuit devices (including transistors, resistors, and capacitors).

TABLE III
SIMULATION RESULTS OF FIRST THREE CHANNELS

Phase Noise	Center Frequency	Level	@10 kHz (dBc/Hz)	@100 kHz (dBc/Hz)
C1	57 MHz	VCO1	-82.34	-110.99
		PLL1 (ω_c=25 kHz)	-93.74	-110.99
		System	-89.16	-102.75
C2	63 MHz	VCO1	-82.40	-111.03
		PLL1 (ω_c=25 kHz)	-93.79	-111.03
		System	-89.18	-102.76
C3	69 MHz	VCO1	-82.45	-111.05
		PLL1 (ω_c=25 kHz)	-93.83	-111.05
		System	-89.20	-102.76

IV. EXPERIMENTAL RESULTS

A. Confirmation of Simulation Results

Table III shows the simulation results of the first three channels of the TV tuner under test. Channels C1, C2, and C3 are the three lowest frequency TV channels, each of which has a bandwidth of 6 MHz. The detail numbers of the intermediate VCOs and PLLs are hidden for IP protection. Their center frequencies are listed for reference. In the open-loop VCO simulation, the transistor noise models and parameters are obtained from the IC manufacturer. It is observed that the phase noise decreases as the channel center frequency increases.

To demonstrate the effectiveness of the proposed methodology, 204 commercial TV tuner chips were tested using bench-top test equipment. The TV signals were generated by Agilent E4432B, and the phase noise was measured by the Agilent 8591C cable TV analyzer. These two pieces of equipment were connected, and the whole test process was automated by a LabVIEW program. Out of the 204 chips, 19 of them did not produce any output at all (gross failure); the other 185 produced measurable output signals. Note that these prototype chips were direct from the manufacturer without being previously tested. The phase noise measurement results are therefore unbiased. Table IV compares the simulation results with the measurement results. The measurement results are obtained from the average of all 185 working chips. It is seen from the table that simulation results are very close to the measurement results at 100-kHz offset. Unfortunately, the phase noise measurement for high-frequency channels could not be finished on all 185 chips due to time constraints. Based on our limited data, the phase noise at 10 kHz is about -93 dBc/Hz. In spite of the limited data, we

TABLE IV
SIMULATION AND MEASURED PHASE NOISE

Channel	Simulation		1st Measurement (without cap.)		2nd Measurement (with cap.)*		Error % (w.r.t 2nd Meas.)	
	10 kHz	100 kHz	10 kHz	100 kHz	10 kHz	100 kHz	10 kHz	100 kHz
C1	-89.16	-102.75	-80.45	-101.69	-86.72	-102.69	2.82	0.06
C2	-89.18	-102.76	-80.96	-101.77	-87.23	-102.99	2.24	-0.23
C3	-89.20	-102.76	-81.35	-101.83	-87.44	-103.11	2.01	-0.34

*only 10 IC tested

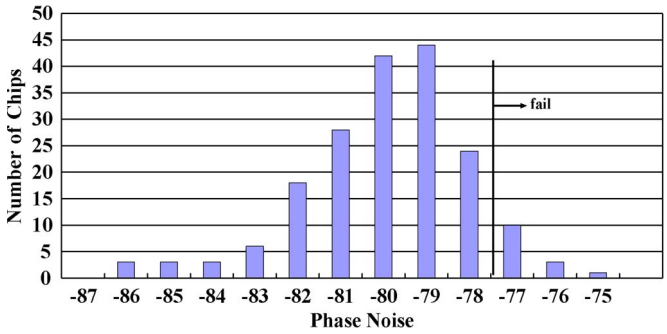

Fig. 16. Histogram of phase noise (10 kHz, C1).

can see the trend that phase noise decreases with frequency on tested chips.

The measurement results at 10-kHz offset, however, were about 9 dB worse than the simulation results. After a long debugging process, it was discovered that the power supply of the board was noisy. The problem was finally solved by attaching a 470-μF decoupling capacitor to the board. After fixing the board problem, the phase noise at 10 kHz greatly improved by 6 dB, and the second measurement results now match the simulation results very well. The error between the simulation results and the retest results is less than 3%. Unfortunately, many of the boards have already been sent to customers for evaluation before the board problem was identified. Only 10 boards were available for the retest with decoupling capacitors. Nevertheless, a consistent improvement of the retest results with respect to the original results is observed for every retested chip.

One possible source of error is the noise floor of the equipment. The noise floor of Agilent 8591C is –105 dBc/Hz at 30-kHz offset. It can be seen that the equipment noise floor is closer to the simulation results at 10-kHz offset than it is at 100-kHz offset. This can be one explanation why the error at 10 kHz is larger than that at 100 kHz.

B. Test Results

Fig. 16 shows the histogram of the phase noise of channel C1 at 10-kHz offset. This histogram shows the data of the 185 working chips in the first measurement (without decoupling capacitors). The required phase noise was originally −85 dBc/Hz at 10-kHz offset. To account for the board problem and the measurement error, 6-dB and 1-dB margins are allowed. The 6-dB guard band is obtained by experiment, and 1 dB is recommended based on past experience in production tests. Therefore, the pass/fail thresholds are chosen to be −78 dBc/Hz and −98 dBc/Hz at 10-kHz and 100-kHz offset, respectively.

Table V shows the mean and standard deviation of the first four channels of the 185 working chips. The confidence intervals of 99.5% confidence level are calculated based on the normal distribution assumption. In the future production test, the chance that the mean of the phase noise would fall in the confidence interval is as high as 99.5%. The confidence interval is very tight (only about 1 dB), so the measurement data are quite representative of the volume production data, as long as the manufacture process remains stable.

Table VI shows the number of chips that passed or failed the phase noise testing. The bottom row shows the results of exhaustive testing—measuring the phase noise of all channels. In the exhaustive testing, a chip passed the test only if its phase noise of all channels was lower than the threshold; a chip failed the test if its phase noise of any single channel was higher than the threshold. In addition to the 19 gross failure chips, 23 chips failed the exhaustive testing at 10 kHz, and one chip failed at 100 kHz. If only channel C1 was tested, one chip would fail the 100-kHz testing, and 14 chips would fail the 10-kHz testing (excluding the 19 gross failures). There would be no test escape at 100 kHz but nine test escapes at 10 kHz. If only two channels (C1 and C2) were tested, then 22 chips would fail the 10-kHz testing. If only three channels (C1, C2, and C3) were tested, then all 23 chips would fail the 10-kHz testing. Based on the results, it is therefore recommended that testing the first three channels is effective.

Fig. 17 shows the Venn diagram of the failed chips. The 19 gross failure chips failed both 10-kHz and 100-kHz testings. The chip that failed the 100-kHz testing is not included in the 23 chips that failed the 10-kHz testing. The experimental data show that both 100-kHz and 10-kHz testings are needed because they detect phase noise of different circuit components.

Table VII shows the estimated test time on ATE for the future production test. The test time is estimated based on the typical phase noise measurement time on an RF automatic tester. On the average, it takes 0.6 s to perform two phase noise measurements for a channel: 1) one at 100 kHz and 2) the other one at 10 kHz. If we test all the channels, the total test time would be around 18 s, which is too long. However, if we test only the first three channels, the test time would be only 1.8 s. The proposed test method reduces the test time by a factor of ten.

V. SUMMARY

This paper presents an effective and economic test method for single-chip TV tuners. This method determines the most effective channels and frequencies to reduce the number of phase noise measurements. The proposed hierarchical

TABLE V
MEAN, STD., AND CONFIDENCE INTERVAL

	@10 kHz			@100 kHz		
	Mean	Standard deviation	Confidence Interval (99.5% Conf. Level)	Mean	standard deviation	Confidence Interval (99.5% Conf. Level)
C1	-80.45	1.93	(-80.84 , -80.05)	-101.69	0.94	(-101.88, -101.50)
C2	-80.96	2.23	(-81.44 , -80.51)	-101.77	0.86	(-101.95, -101.60)
C3	-81.35	2.11	(-81.79 , -80.92)	-101.83	0.93	(-102.02, -101.64)
C4	-82.53	2.57	(-83.06, -82.00)	-101.95	1.63	(-102.02, -101.61)

TABLE VI
NUMBER OF PASS/FAIL CHIPS (TOTAL 204 CHIPS)

Channel	10 kHz			100 kHz		
	pass	gross fail	PN fail	Pass	gross fail	PN fail
C1	171	19	14	184	19	1
C1+C2	163	19	22	184	19	1
C1+C2+C3	162	19	23	184	19	1
C1+C2+C3 +C4	162	19	23	184	19	1
ALL	162	19	23	184	19	1

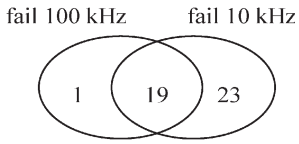

Fig. 17. Venn diagram of failed chips (total 204 chips).

TABLE VII
ESTIMATED TEST TIME ON ATE

Channel Tested	Test Time (Sec.)
C1	0.6
C1+C2	1.2
C1+C2+C3	1.8
C1+C2+C3+C4	2.4
exhaustive	18

simulation method produces good results that match well with the measurement results. Experimental data on commercial chips show that our proposed method reduces the test time by a factor of ten without test escapes.

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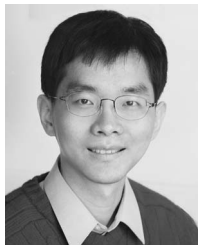

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Chuo-Jan Pan, photograph and biography not available at the time of publication.

Chao-Wen Tseng, photograph and biography not available at the time of publication.