Fully Integrated Seven-Order Frequency-Range Quadrature Sinusoid Signal Generator

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Abstract—A compact wide-frequency-range quadrature sinusoid signal generator tailored to on-chip impedance spectroscopy instrumentation applications is described. Using a new hybrid structure, it provides seven orders of frequency-tuning range (1 mHz to 10 kHz) appropriate for impedance characterization of many sensor materials. The signal generator exhibits very accurate frequency tuning through digital control, and the new structure inherently guarantees good phase and amplitude matching between sine and cosine outputs across the supported frequency range. The circuit has been fabricated in a 0.5-μm CMOS process and occupies 1 mm^2. It consumes only 60 μA with a 3-V supply. Measurements show that the phase mismatch is less than 0.8° and that the amplitude mismatch is less than 3%. The total harmonic distortion is below 0.6% over the seven-order frequency range.

Index Terms—Analog filter, impedance measurement, quadrature signal generator, sinusoid signal generators, wide-frequency-range frequency tuning.

I. INTRODUCTION

QUADRATURE sinusoid signals are two sinusoid signals with the same frequency and amplitude but with a 90° phase difference. They are necessary for signal processing in many applications. To suppress image channel interference in wireless communication systems, quadrature sinusoid signals enable complex signal processing with in-phase and quadrature-phase signals. In instrumentation applications, they are used to extract impedance/admittance information. Some applications require only square-wave quadrature signals [1], whereas applications with tighter accuracy constraints demand high-quality continuous-time quadrature sinusoid signals to guarantee performance. Typically, the quality of a quadrature sinusoid signal is measured by the frequency accuracy, linearity, and phase/amplitude matching between the two signal outputs.

This paper introduces a quadrature sinusoid signal generator (QSSG) designed for a low-frequency on-chip impedance spectroscopy (IS) instrument that is suitable for characterizing a wide range of sensor interfaces. The frequency range of the IS instrument, and therefore the QSSG, was broadened to meet the low-frequency requirements of biochemical sensors based on biomimetic interfaces with membrane proteins [2], [3]. The

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Fig. 1. Block diagram of a DSP-based sinusoid signal generator.

resulting challenge is providing a tunable frequency range from 1 mHz to 10 kHz, seven decades, with good frequency accuracy and phase/amplitude matching between sine and cosine outputs. Circuit size is also a critical constraint in the QSSG design to support the implementation of a fully on-chip IS instrument suitable for sensor arrays.

Many methods for sinusoid signal generation can be found in commercial products and research papers. Generally speaking, these methods can be categorized into three groups, namely, DSP-, oscillator-, and nonlinear-circuit-based solutions.

DSP-based solutions generate a sinusoid signal using digitally stored information [4], [5]. As shown in Fig. 1, they consist of a digital memory bank, a digital signal processor, a digital-to-analog converter (DAC), and analog output circuits. Frequency turning is achieved by different strategies [6] to vary the memory updating clock. They are very flexible, and nearly all waveform shapes can be obtained by changing the memory bank contents. However, their value becomes limited at very low frequencies. To relax the design requirements of the analog filter, the update clock frequency cannot be very low. Thus, a very high signal oversampling ratio (OSR) is expected for low-frequency outputs. To store the waveform for each sampling point over the whole cycle, prohibitively large memory is needed. Although this memory is easily achievable with modern IC technology, the size of the memory would bar implementation of a compact signal generator for on-chip IS instrumentation.

Oscillators are the most widely used circuits to generate pure sine waves. Quadrature oscillators have also been reported for generating quadrature signals [7], [8]. In an oscillator-based sinusoid signal generator, the frequency is controlled by a tunable component in the circuit, such as a resistor, a capacitor, or a transconductor. The limitation with these oscillator-based signal generators lies in their narrow frequency-tuning range; the tuning component values, which control the output frequency, cannot be controlled over a very wide range (seven to eight orders, as desired). Although a subthreshold tunable CMOS transconductance that provides a frequency-tuning range over seven decades has been reported [9], the high-frequency accuracy is limited because it is impractical to precisely tune the transconductance over that wide of a range.

In nonlinear-transfer-function-based signal generators [10], a nonlinear transformation is utilized to convert the triangle wave to a sine waveform, as shown in Fig. 2(a). MOS transistors can
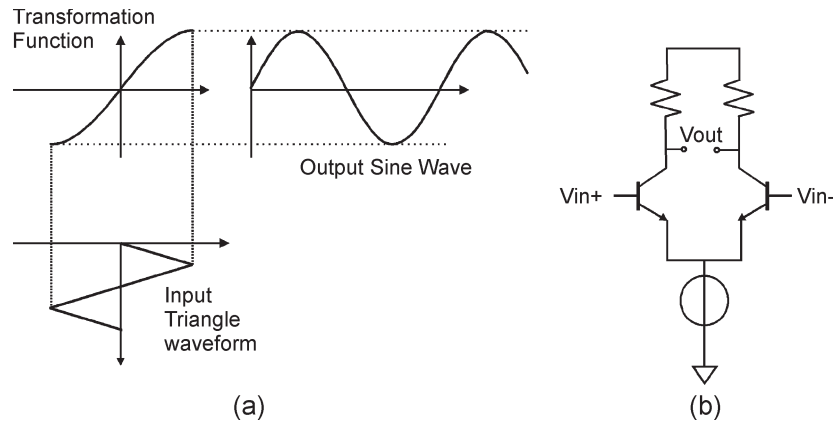
Fig. 2. Principles of the triangle-to-sine signal generator. (a) Transformation from a triangle waveform to a sine waveform. (b) Typical circuit performing the transformation.

also be used to realize the nonlinear functions [11]. Because a triangle wave can easily be generated, these nonlinear-transfer-function-based methods provide a simple means of realizing a sinusoid signal generator. However, the main drawback of the triangle-to-sine generator is its linearity, which is limited by how well the nonlinear function approximates half of the sine wave. In addition, both the peak value and the common-mode bias voltage of the triangle wave are very critical to the quality of the sinusoid output. For on-chip applications, the nonlinear transfer function is adversely affected by process and temperature variations of semiconductor devices, making it hard to control its quality in terms of linearity. Furthermore, if this type of generator were employed for quadrature outputs, two *identical* nonlinear transfer functions would be required, and any mismatch between them would directly contribute to the mismatch between sine and cosine outputs.

All of these traditional signal generators are not suited to construct a compact QSSG circuit covering from 1 mHz to 10 kHz due to their limitations in frequency range, physical size, or quality of the waveform. In this paper, a new hybrid structure QSSG was designed and tested. The new circuit can generate quadrature sinusoid signals covering from 1 mHz to 10 kHz with inherently good phase (0.8°) and amplitude matching (3%). Section II describes the architecture of the new signal generator. Its VLSI realization is presented in Section III, and measurement results of the fabricated circuit are provided in Section IV. Section V gives conclusions.

II. New Architectures and Principles

Of the aforementioned traditional signal generator topologies, none are well suited to construct a compact QSSG circuit covering from 1 mHz to 10 kHz due to their limitations in frequency range, physical size, or quality of the waveform. To overcome these limitations, a new architecture is introduced here that can generate high-quality outputs over seven decades of the frequency range. The new signal generator topology employs a hybrid architecture, integrating two different structures for low- and high-frequency outputs. It is purely controlled by digital signals, and its output frequency is set with respect to a single master clock to achieve high-frequency accuracy. A system-level view of the proposed signal generator is shown in Fig. 3.
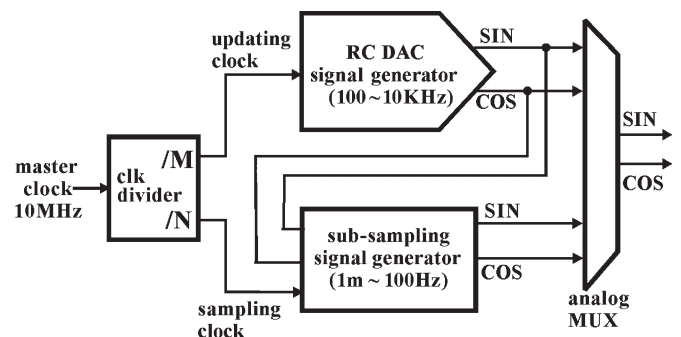

Fig. 3. Principle schematic of the new hybrid quadrature signal generator.

For the frequency range between 100 Hz and 10 kHz, a signal generator based on a resistor-chain DAC (RCDAC) is employed to generate the quadrature sinusoid signals. It provides exact frequency control for the output sinusoid signal by controlling the frequency of a digital updating clock. It also guarantees good matching between output sine and cosine signals because both of them are generated from the same resistor chain.

To generate low frequencies (1 mHz to 100 Hz), the outputs of the RCDAC signal generator are subsampled, i.e., sampled at lower frequencies. To our knowledge, this is the first time that the subsampling technique has been utilized in signal generators. As will be detailed later in this paper, this subsampling signal generator provides very good coverage for low frequencies with a minimal chip area.

As will be detailed in Section III-C, both circuit paths will require low-pass filters (LPFs) at their outputs to suppress the replicas and remove high-frequency switching glitches. It will be shown that the RCDAC requires at least 17-dB replica suppression, whereas the subsampling circuit requires up to 13-dB replica suppression.

A. QSSG Based on a Sinusoidally Tapped RCDAC for 100 Hz to 10 kHz

For high-frequency (100 Hz to 10 kHz) sinusoid signals, an RCDAC is unevenly tapped so that its output steps a sinusoid waveform. The sinusoid output is generated by sequentially activating these taps at a rate determined by the master clock signal. A simplified example of the RCDAC, as shown in Fig. 4, illustrates this operation principle. Here, by sampling
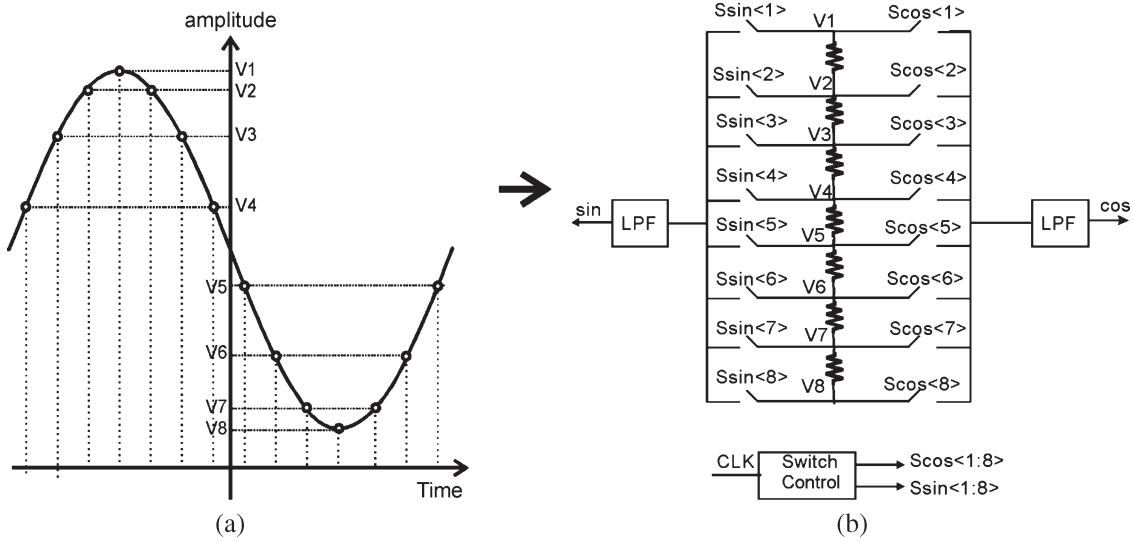
Fig. 4. Principles of a sinusoidally tapped RCDAC quadrature sinusoid signal generator. A resistor chain with only eight taps is demonstrated for illustration; the real system has 33 taps.

one period of the sinusoid at 14 regular intervals, the eight sample points for a sine wave [Fig. 4(a)] can be stored in only eight DAC taps [Fig. 4(b)] by setting appropriate values for resistors in the chain. The top and bottom voltages of the resistor chain determine the peak and valley of the sinusoid wave, respectively. To simultaneously generate cosine and sine waveforms, a separate set of switches is employed on each side of the chain and activated out of phase. At any time, only one switch on each side is turned on to pick the appropriate tap in the chain. The sequence of turning on the switches is 1–2–3–4–5–6–7–8–7–6–5–4–3–2, and the frequency is determined by the updating clock. By periodically repeating this sequence, a sinusoid waveform is generated. The sequence is the same for both sine and cosine outputs, except that switch activation is offset by four switches (in this example) to introduce a 90° phase difference. An LPF is included at the DAC output to smooth the output waveform and filter out replicas. Because both sine and cosine waveforms are generated from the same resistor chain, quadrature matching is very good.

Clock jitter in the digital control circuitry will introduce variations in the switching time of the RCDAC. Based on reported jitter values [12], this variation should only be on the order of picoseconds. Because the maximum output frequency of the signal generator is ∼10 kHz, this clock jitter should have a negligible effect.

Comparing this RCDAC-based sinusoid signal generator with that based on the DSP techniques briefly reviewed in Section II [4], [5], we see that both utilize an updating clock to generate the sine wave and control the frequency. However, in our new design, the "sinusoidally coded" RCDAC replaces the waveform memory and general DAC in Fig. 1, thus eliminating the need for digital memory and saving a significant silicon area. Similar to its DSP counterpart, the RCDAC-based QSSG cannot generate a very low frequency because the number of taps available in the R-chain, representing its "memory size," is limited by physical routing and other practical issues.

In the current implementation of the RCDAC-based high-frequency QSSG, we have set the number of taps to 33, which

corresponds to a 64× OSR. The lowest output frequency is set to 100 Hz, where the low-frequency sinusoid signal generator (see succeeding discussion) takes over.

B. Subsampling QSSG for 1 mHz to 100 Hz

In contrast to Nyquist sampling techniques, where the sampling frequency is required to be more than twice the signal frequency, the subsampling technique relies on a sampling frequency that is less than twice the signal frequency. The sample-and-hold results have a fundamental signal and many replicas in the frequency spectrum. The desired output is one of the replicas. This technique is often used in communication systems to down convert the information from radio to low intermediate frequency, enabling signal processing [13]. In our design, a novel sinusoid generator topology based on the subsampling concept was developed to produce very low frequency outputs.

The "reference" inputs to the subsampling signal generator are the quadrature sinusoid signals produced by the RCDAC-based signal generator. These signals are sampled at a frequency that is very close to the signal frequency, i.e., the frequency difference is very small. The output of the sampling circuit contains a low-frequency replica that represents the frequency difference between the input signal and the sampling clock. This replica can be extracted to obtain the desired low-frequency sinusoid outputs. The sequence of a sampled sinusoid input is given by

$$f(n) = \sin\left(2\pi f_0 \frac{n}{f_s}\right) \qquad (1)$$

where n is the index of the discrete sequence, f_0 is the signal frequency, and f_s is the sampling frequency. Assuming that f_s is very close to f_0 and letting $\Delta f = f_0 - f_s$, (1) can be expressed as

$$f(n) = \sin\left(2\pi n + 2\pi \Delta f \frac{n}{f_s}\right) = \sin\left(2\pi \Delta f \frac{n}{f_s}\right). \qquad (2)$$

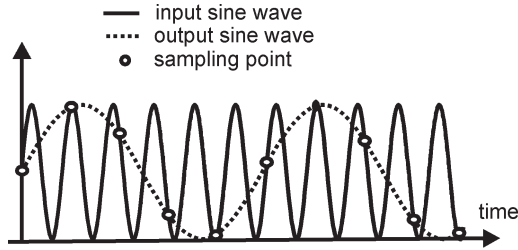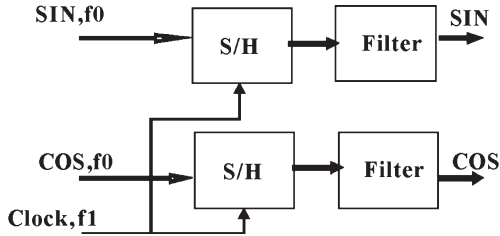Fig. 5. Illustration of the subsampling concept.

Fig. 6. Functional block diagram of the subsampling signal generator.

TABLE I
OUTPUT FREQUENCY AND SIGNAL GENERATOR SETTINGS

f_{out} Output frequency (Hz)	f_0 RCDAC frequency (Hz)	M	N	Output source
100- 10k	varies	1562 -16	N/A	RCDAC
10 − 100	10k	16	1025 - 1035	
0.1 − 10	1k	156	9985 − 10085	Sub-sampling
1m − 0.1	100	1562	100033-104218	

Fig. 7. Frequency step size over the operational frequency range.

Compared with (1), (2) still represents a discrete sinusoid signal, but its frequency is Δf. This principle is graphically shown in Fig. 5, where the sinusoid input (solid line) is sampled (dots) by a frequency very close to the signal frequency and a sinusoid output signal (dashed line) can be formed. A functional block diagram for the circuit to implement this new subsampling signal generator scheme is shown in Fig. 6.

To achieve a constant frequency sinusoid output using subsampling, it is critical to maintain a constant frequency difference between the sampling and input signals. Thus, both the RCDAC updating clock and the subsampling clock have been based on the same 10-MHz master clock, dividing them by factors of M and N, respectively. This permits a stable and very well controlled relationship between the two frequencies.

C. Frequency Range and Coverage Density

In the 100-Hz to 10-kHz range, the sinusoid output frequency of the QSSG is controlled by setting the frequency of the RCDAC updating clock, which is derived by dividing the master clock. With the RCDAC OSR set to 64×, the QSSG output frequency can be expressed as

$$f_O = \frac{f_M}{64M} \quad (3)$$

where f_M is the frequency of the master clock, and M is the updating clock division factor. By setting M from 16 to 1562, the QSSG (with a 10-MHz master clock) can generate sufficient frequency points between 100 Hz and 10 kHz for impedance characterization applications.

The output frequency of the subsampling QSSG is determined by

$$f_{out} = f_O - f_s = \frac{f_M}{64M} - \frac{f_M}{n} \quad (4)$$

where N is the subsampling division factor, and f_{out}, f_o, f_s, and f_M are the frequency of the subsampling output, the RCDAC QSSG output, the sampling signal, and the master clock, respectively, as shown in Fig. 3. For a given f_M and M,

if both M and N are integers, the minimum f_{out} is achieved by setting $N = 64M + 1$ and can be expressed by

$$f_{out,min} = f_M \left(\frac{1}{64M} - \frac{1}{64M + 1} \right)$$
$$= \frac{f_M}{(64M)(64M + 1)} \approx \frac{f_O^2}{f_M} \quad (5)$$

which shows that, to lower the output frequency, either the master clock frequency can be increased or the output frequency of RCDAC signal generator can be decreased. However, f_o cannot be very low for two reasons: First, similar to the DSP-based signal generator, the RCDAC signal generator with very low output frequencies would add significant complexity to the analog filter design because the sampling clock will be very close to the signal frequency. Second, because f_s must be close to f_o, the sample-and-hold circuit would suffer significant leakage at a very low updating frequency. To avoid these problems, the lowest f_o was set to 100 Hz in our implementation. Thus, to achieve a 1-mHz QSSG output frequency, (5) shows that the master clock should be 10 MHz.

Table I defines the RCDAC output frequency and the signal generator settings that will cover the desired 1-mHz to 10-kHz range. It also defines which signal source is directed to the output of the overall QSSG; from 1 mHz to 100 Hz, the subsampling block signal is output, and for 100 Hz to 10 kHz, the RCDAC generator signal is output.

Because M and N are integers, the possible output frequency values are discrete and cannot cover every point in the frequency range. However, in practice, continuous coverage is not necessary, provided the signal generator can maintain sufficient coverage density. The frequency step size at each frequency point is plotted in Fig. 7 and shows that at least ten points are produced per decade, which is more than enough for impedance measurement applications.
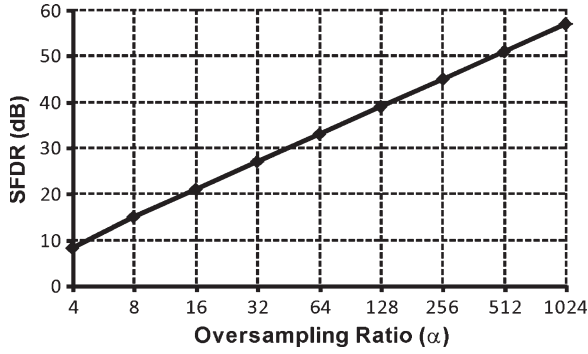
Fig. 8. Plot of the SFDR versus the OSR.

Fig. 9. Schematic of the RCDAC.

Fig. 10. T/H circuit for the subsampling QSSG.

III. VLSI REALIZATON

A. RCDAC for the High-Frequency QSSG

The RCDAC QSSG generates quadrature sinusoid signals of 100 Hz and above. The most important parameter of the RCDAC, as functionally described in Fig. 4(b), is the number of taps along the resistor chain, which determines the OSR of the output sinusoid waveform. Although increasing the number of taps improves linearity, it increases switch control logic complexity and requires more silicon areas for the switches and routing metals.

To determine an optimal OSR, the output linearity of the DAC has been analyzed in terms of the spurious-free dynamic range (SFDR). The waveform of the RCDAC output is a sample-and-hold sine wave. Its typical spectrum includes the fundamental signal and sampling replicas at multiples of the sampling frequency, which are enveloped by a sinc function [14]. Only the first replica will be considered because it dominates the spurs. Thus, the SFDR is defined as

$$\text{SFDR} = 20 \log \left(\frac{A_0}{A_1} \right) \qquad (6)$$

where A_0 and A_1 are the strengths of the fundamental signal and the first replica, respectively. Assuming the amplitude of the sample-and-hold sine wave to be 1

$$A_0 = \left| \frac{\alpha}{\pi} \sin \left(\frac{\pi}{\alpha} \right) \right| \qquad (7)$$

$$A_1 = \sqrt{\left(\frac{\alpha}{\pi(\alpha-1)} \sin \left(\pi \frac{\alpha-1}{\alpha} \right) \right)^2 + \left(\frac{\alpha}{\pi(\alpha+1)} \sin \left(\pi \frac{\alpha+1}{\alpha} \right) \right)^2} \qquad (8)$$

where α is the OSR at the DAC output. Based on (6)–(8), the relationship between SFDR and α can be plotted, as shown in Fig. 8. Because the replica strength is inversely proportional to the OSR, Fig. 8 shows that the SFDR is higher as the OSR increases.

Fig. 8 indicates that, when the OSR is greater than 512, a linearity (SFDR) of more than 50 dB is achieved without replica suppression. However, this would require 256 or more taps on the DAC and is undesirable because of the required circuit complexity and chip area. Each tap needs a dedicated control signal; therefore, as the number of taps increases, so
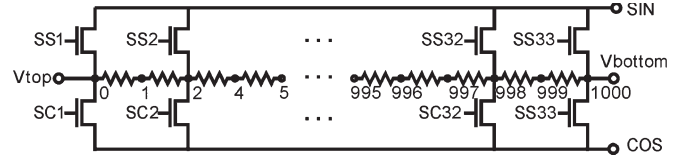
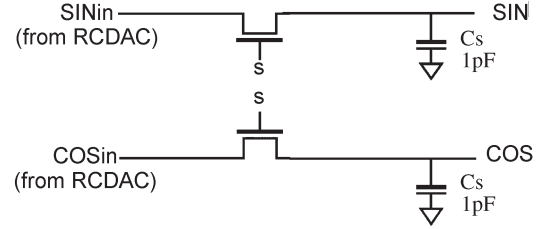does the required routing area. A preferable alternative is to lower the OSR and employ an LPF to further improve the SFDR by suppressing the replicas. However, the OSR cannot be too low because it determines the distance between the fundamental signal and its replicas, adding undesirable complexity to filter design. After analyzing this tradeoff to minimize the DAC and filter circuit complexity/area, the OSR was set to 64×, requiring only 33 DAC taps. For a 64× OSR, (6)–(8) give an SFDR of 33 dB; thus, the proceeding LPF needs to provide at least 17-dB suppression of the replicas to achieve a 50-dB SFDR. Compared with the alternative of using 256 taps and no filter, the routing area is decreased by 87%. Because a simple compact second-order LPF is sufficient to provide 17-dB replica suppression, the chosen approach provides a significant overall area savings.

The schematic of the 64× OSR RCDAC is shown in Fig. 9. For a high linearity, matching of DAC resistors is very important. In this sinusoidal tapped DAC, the resistances between taps are not equal, as they would be in a linear DAC. Because matching can best be achieved with same-size resistors, a resistor chain composed of 1000 same-size resistors was utilized, and the 33 tap points were sinusoidally mapped across the 1000 elements. At each tap point, a separate switch for sine and cosine taps was included. NMOS transistor switches were used instead of complimentary CMOS switches to simplify control logic and save chip area.

B. T/H Circuit for the Subsampling QSSG

To sample and hold the sinusoid outputs of the RCDAC QSSG, the track-and-hold (T/H) circuit shown in Fig. 10 was realized. Minimum-sized NMOS transistors were employed for the switches for two reasons: First, charge injection of the switch is a potential problem for the simple T/H circuit in Fig. 10. Having a small channel capacitance compared with the sampling capacitor (Cs), they minimize the charge injection effect. Second, they minimize the transistor source/drain leakage current to prevent a significant charge loss on the sampling capacitor, even at the lowest sampling frequency, ~100 Hz. Notice that, in this application, the sampling clock frequency is very close to the input reference sinusoid frequency, and therefore, the voltage change between two consecutive tracking
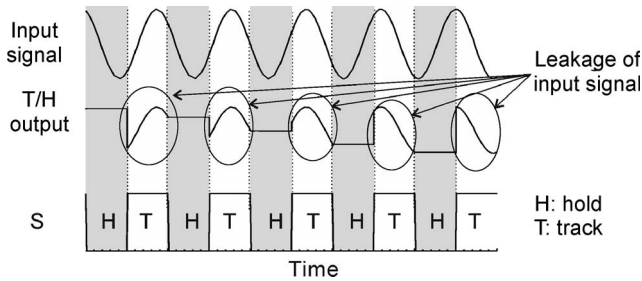
Fig. 11.   Waveform of signals for the T/H system.

Fig. 12.   Schematic of the g_m-C biquadratic filter.

TABLE II
OUTPUT FREQUENCY AND SIGNAL GENERATOR SETTINGS

	Gm	C1	C2	Cutoff Frequency
Fixed filter	9n	7.5p	3.7p	250
Tunable filter	60n	5p	2.5p	2k
	600n	5p	2.5p	20k
	600n	0.5p	0.25p	200k

operations is very small. Therefore, even with a minimum-sized NMOS sampling switch, the signal will still quickly settle.

Another potential concern for the subsampling T/H system is pollution of the output signal during the tracking phase. The T/H system, as shown in Fig. 10, periodically switches between the T/H modes based on the value of S, which is the switch control signal in Fig. 10. The desired low-frequency sinusoid output is composed of the sequence of hold values. However, in the track mode, the input and output are shorted, and therefore, the high-frequency input shows at the output. Thus, as shown in Fig. 11, the T/H system presents two time-multiplexed signals at its output, namely, the desired hold-mode output and the track-mode leakage. The duty cycle of S determines the relative strength of these two signals. To achieve a high SFDR, the track-mode duration is set very narrow, around 100 ns, much less than the 10-μs or greater hold-mode duration, so that the track-mode leakage appears as glitches that are easily removed with a simple filter. An alternative solution to the track-mode leakage is to establish two paths, where, at any given time, one is in tracking mode and the other is in holding mode, and include an analog multiplexer that always connects the path in tracking mode to the output. However, this would double the number of switches connected to the sampling capacitor, increasing the source/drain leakage to potentially significant levels at the lowest sampling frequency ($\sim$100 Hz).

C. Filter Design

To smooth the output and provide good replica suppression, the RCDAC QSSG requires an LPF. To cover its entire frequency range, a filter with selectable cutoff frequencies was determined to be most effective. The filter's cutoff frequency was set to 2 kHz for output frequencies of 100 Hz to 1 kHz and to 20 kHz for 1–10 kHz. Note that, if coverage density were not critical, the RCDAC QSSG is capable of generating frequencies greater than 10 kHz by setting the division factor M to less than 16. To support this extended range, a filter cutoff frequency of 200 kHz was also implemented.

At each of the three tunable settings, the least replica suppression occurs when the input is at the low end of the frequency range, where the replicas are the closest to the filter cutoff frequency. For example, when the cutoff frequency is 2 kHz, replicas are least suppressed when the output signal is at 100 Hz. The worst-case replica suppression for the RCDAC tunable filter was designed to be 21 dB, which is more than the 17 dB required to achieve the target 50-dB SFDR with a 64-tap RCDAC.
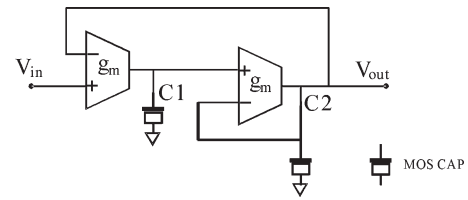
For the subsampling QSSG, notice that the sampling clock is very close to the RCDAC output frequency. Thus, the OSR is approximately the ratio between the RCDAC output frequency and the subsampling QSSG output frequency. Based on Table I, the OSR for outputs between 1 mHz and 1 Hz is 1000 and above, which supports an SFDR of more than 50 dB (Fig. 8). Here, the filter is not required to provide replica suppression but will smooth the output of high-frequency switching glitches. Alternatively, for the 1- to 100-Hz outputs, the OSR could be as low as 100, and additional 13-dB replica suppression is needed based on Fig. 8. The subsampling QSSG has a relatively constant sampling frequency because the output frequency is tuned by controlling the small frequency difference between the sampling and input reference frequencies. Thus, for output frequencies within 1–100 Hz, the second-order replicas only appear at either 1 kHz or 10 kHz, easing filter design requirements. An LPF with a fixed cutoff frequency of 250 Hz was determined to provide the necessary replica suppression.

For both the RCDAC and subsampling QSSG, a second-order Butterworth filter was implemented to provide maximum passband flatness. The g_m-C biquadratic circuit, as shown in Fig. 12 [15], was chosen to realize both the tunable and fixed cutoff frequency filters. To achieve Butterworth performance, the ratio of $C1$ to $C2$ was set to 2 so that Q is fixed at 0.707, which provides maximum flatness on the passband. The g_m and C values chosen for each of the filter configurations and settings are listed in Table II. Rather than using metal–insulator–metal capacitors, NMOS gate capacitances were used to minimize the chip area.

For the tunable filter, g_m and the two capacitors each have been implemented with two selectable values, appropriately chosen to provide the three different cutoff frequencies shown in Table II. Both capacitors are implemented using two elements in parallel that can be switched on/off to set the correct value. For the fixed filter, with the capacitors set to reasonable on-chip values, a very small g_m value (9 nS) was needed to achieve the 250-Hz cutoff frequency.

To generate g_m for the filters, an operational transconductance amplifier (OTA) was used. The transconductance of the OTA should be small to match the small capacitances available on chip. There are several ways to design an OTA with a small g_m, including an OTA with current division [16] and/or source
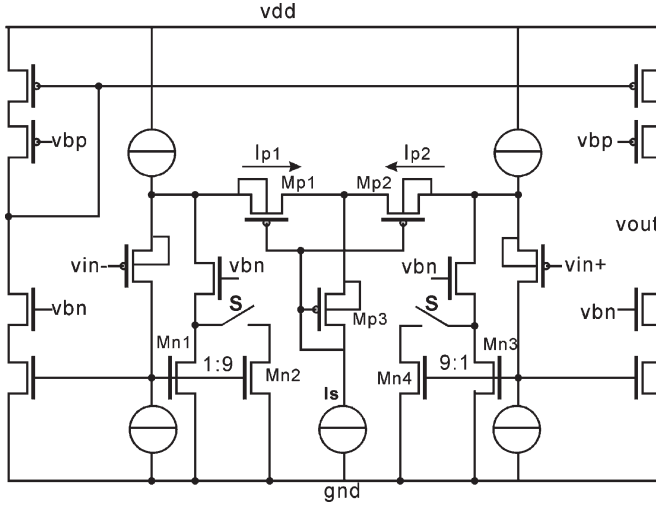
Fig. 13.   Simplified schematic of the OTA.

degeneration [17], a floating-gate OTA [18], and a bulk-driven OTA [19]. Because an OTA with current division and source degeneration consumes less power and has an easily tunable g_m value [20], this approach was selected for the QSSG filters. Fig. 13 shows the OTA that was designed to combine these two techniques in a new way. The input PMOS transistors are sized to 12 μm/1.2 μm. Current division was realized with the mirror structures Mn1 and Mn2, and Mn3 and Mn4. Internal feedback loops involving each of the input pair transistors control the gate of the current mirror transistors Mn1 and Mn3. With the current of the input transistors fixed, this structure gives good linearity performance. PMOS transistors (Mp1 and Mp2) working in a triode region were used as the source degeneration resistors, i.e., MOS-R. The g_m of this OTA is

$$g_M = K \frac{g_{O1,2}}{2} \tag{9}$$

$$g_{O1,2} = \sqrt{2\mu C_{OX} \frac{W_{Mp1,2}}{L_{Mp1,2}} I_s} \tag{10}$$

where I_S is the bias current for the source degeneration MOS-R (Mp1 and Mp2), and K is the ratio of current division, which is controlled by S in Fig. 13. Thus, the transconductance g_m can be tuned by the size of the MOS-R and its bias current.

For the filter with variable cutoff frequencies, the W/L ratios of Mp1 and Mp2 were set to 1.5 μm/24 μm, and the bias current I_S was set to 300 nA. With switch S turned on or off, it can provide transconductances of 60 and 600 nS, respectively. For the filter with a fixed 250-Hz cutoff frequency, the W/L ratios of Mp1 and Mp2 were set to 1.5 μm/150 μm, and I_S was set to 50 nA. With the switches S always closed, a transconductance of 9 nS was achieved.

IV. EXPERIMENTAL RESULTS

The complete QSSG was implemented in a 0.5-μm CMOS process and occupies 1 mm × 1 mm, as shown in Fig. 14. With a 3-V supply, the entire circuit draws only 60 μA. Test results demonstrate that it can generate the desired quadrature sinusoid signals from 1 mHz and 10 kHz with good matching and linearity. For the prototype circuit, external clock dividers were
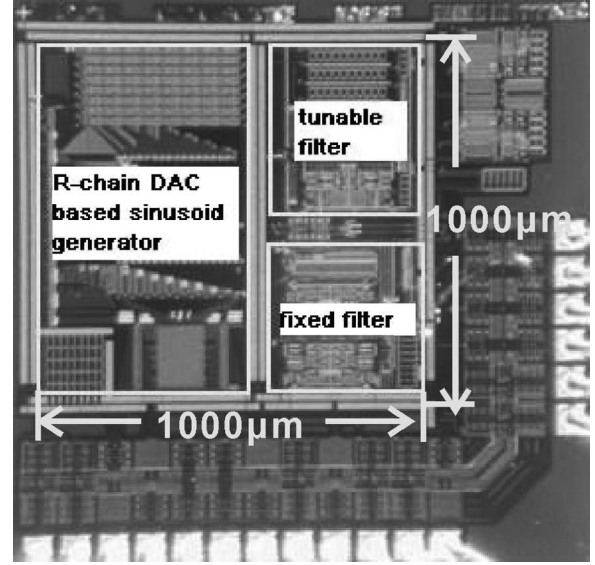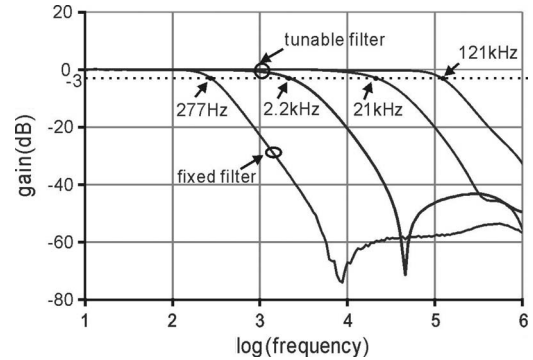

Fig. 14.   Die photo of the new QSSG.

Fig. 15.   Measured frequency response of the filters with −3-dB bandwidths labeled for each plot.

employed to generate the proper updating clock for the RCDAC and subsampling signal generator, as shown in Fig. 3. An integrated version of this divide-by-N function could readily be achieved with digital counters or modular dividers [21].

A. Analog Filter Characterization

Because the performance of the analog filters is critical to the overall signal generator, they were independently tested. Experiments were performed to check the frequency transfer function and large signal linearity for the two second-order filters (one with three tunable cutoff frequencies, and the other with a fixed cutoff). Fig. 15 shows the transfer function of the filters combined into one plot for easy comparison. The measured cutoff frequencies are slightly shifted from design values, but they can still provide sufficient suppression of the replicas. To demonstrate the achieved filter linearity, Fig. 16 shows the output signal frequency spectrum for both the tunable and fixed filters. Only one plot is given for the tunable filter because the main nonlinearity contributors, namely, Mp1 and Mp2 in Fig. 13, are the same for all three cutoff frequencies. These plots show that both filters can provide more than 50-dB linearity with up to a 500-mVpp sinusoid input.
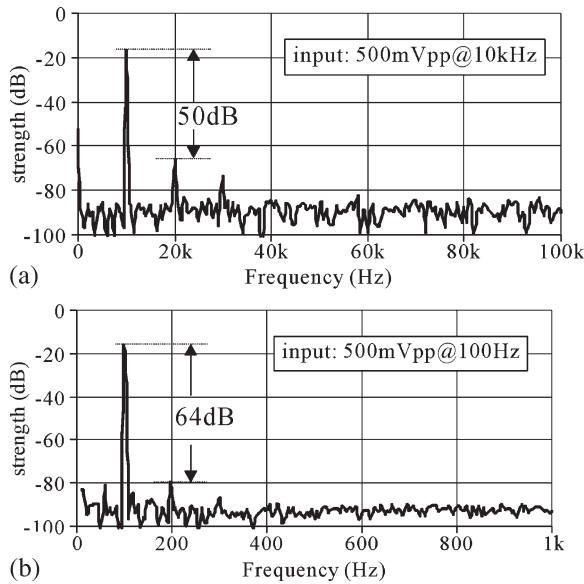
Fig. 16. Filter frequency spectrum demonstrating linearity. (a) Output of the tunable filter with 500 mVpp at a 10-kHz sinusoid input. (b) Output of the fixed filter with 500 mVpp at a 100-Hz sinusoid input.
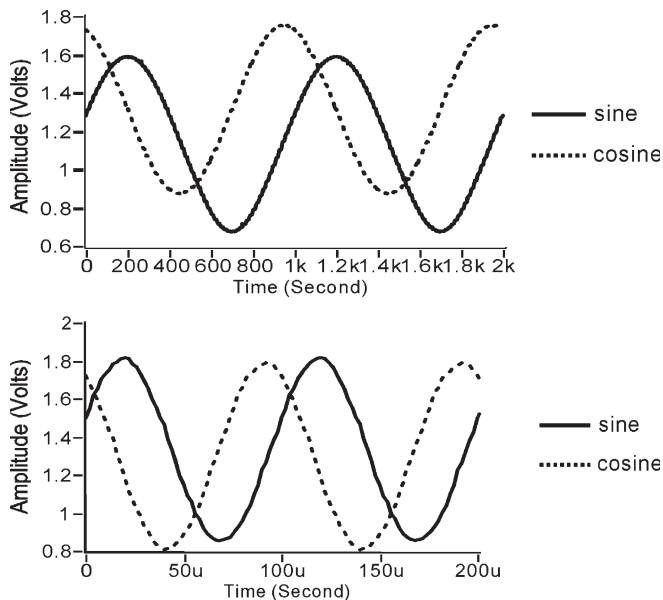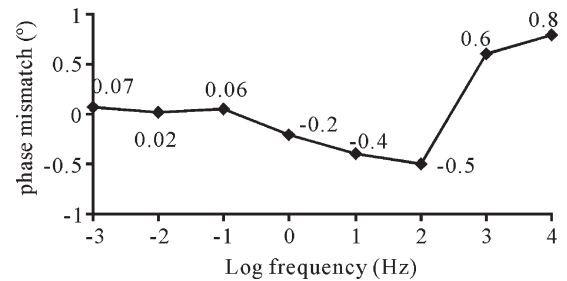

Fig. 18. Phase mismatch of the output quadrature signals over frequency.
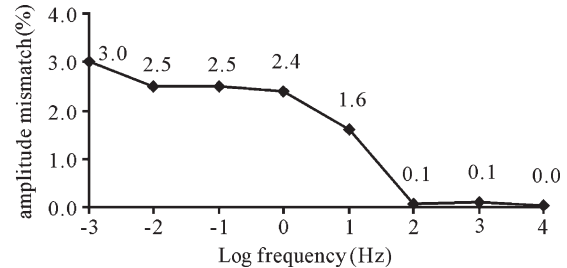

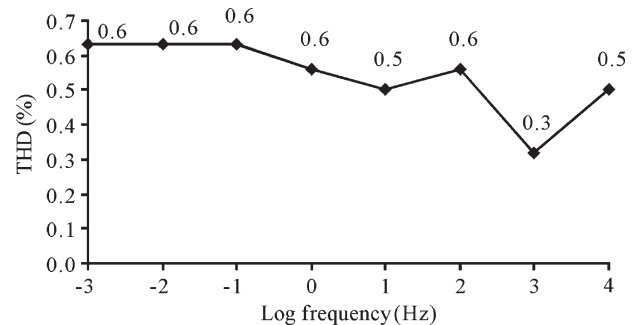Fig. 19. Amplitude mismatch of the output quadrature signals over frequency.

Fig. 20. THD of the output quadrature signals.

Fig. 17. Waveforms of quadrature sinusoid outputs at two frequencies: (top) 1 mHz and (bottom) 10 kHz.

TABLE III
PERFORMANCE SUMMARY OF THE QSSG

Technology	$0.5\mu m$ CMOS
Die area	$1mm^2$
Power consumption	$60\mu A$ at 3V
Frequency range	1m Hz – 10kHz
Phase mismatch	$< 0.8°$
Amplitude mismatching	$< 3\%$
THD	$< 0.6\%$

B. Quadrature Sinusoid Output

Several output frequency test points, ranging from 1 mHz to 10 kHz, were generated and observed to be correct. The waveforms of two extreme output frequencies are plotted in Fig. 17. Fig. 17 shows a direct-current offset between 1-mHz sine and cosine outputs. This is partially due to the offset in the fixed filters and is constant over frequency for all subsampling circuit (1 mHz to 100 Hz) outputs, allowing it to be precalibrated.

To quantify how well the sine and cosine results match expectations, the phase mismatch (variation from 90° between sinusoid and cosine outputs), amplitude mismatch, and total harmonic distortion (THD) were measured across the entire frequency range. These results, which are plotted in Figs. 18–20,

respectively, show that the new QSSG design can provide high-quality quadrature sinusoid outputs with good phase ($< 0.8°$) and amplitude matching ($< 3\%$) between sine and cosine outputs. Frequency accuracy is inherently guaranteed by digital control of the clock frequencies. The measured THD is smaller than 0.6% over the entire seven-order frequency range. Performance is summarized in Table III.

V. CONCLUSION

An on-chip QSSG with a seven-order frequency span (1 mHz to 10 kHz) suitable for miniaturized impedance measurement instruments has been presented and described. To our knowledge, this signal generator achieves the widest frequency range reported to date. Utilizing a hybrid architecture that employs the

subsampling technique in an original manner, the overall QSSG provides excellent phase ($0.8°$) and amplitude (3%) matching between quadrature sinusoid signals and less than 0.6% THD over its entire 1-mHz to 10-kHz span. It inherently guarantees frequency-tuning accuracy with purely digital control. The new QSSG circuit was implemented in a 0.5-μm CMOS process, where it occupies only 1 mm^2 and consumes only 60 μA at 3 V. Measurement results confirm that the design meets the frequency range and performance requirement for on-chip sensor impedance instrumentation.

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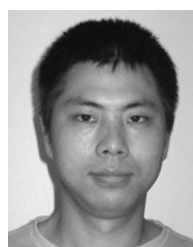
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