A High-Voltage Test Bed for the Evaluation of High-Voltage Dividers for Pulsed Applications

Miguel Cerqueira Bastos, Maria Hammarquist, and Anders Bergman

***Abstract*—The design, evaluation, and commissioning of a high-voltage reference test bed for pulsed applications to be used in the precision testing of high-voltage dividers is described. The test bed is composed of a pulsed power supply, a reference divider based on compressed-gas capacitor technology, and an acquisition system that makes use of the fast measurement capabilities of the HP3458 digital voltmeter. The results of the evaluation of the reference system are presented.**

***Index Terms*—Capacitance measurement, high-voltage techniques, linear particle accelerator, large Hadron Collider, measurement uncertainty, pulse measurement, pulsed power supplies, voltage measurement.**

I. Introduction

IN ORDER to increase the luminosity of the proton beams injected into the Large Hadron Collider at the European Organization for Nuclear Research (CERN), the new linear accelerator Linac4 [1] is being built to replace the old injector Linac2. Operation is foreseen to start in 2014.

Radio-frequency (RF) power requirements for the new accelerator translate into new requirements for the high-voltage measurements at the level of the klystron power supplies: Cathode and anode voltages will be pulsed at −110 and −50 kV, respectively, with a repetition rate of 1.1 Hz. Voltage rise and fall times are in the range of 150 μs, and pulsewidth is approximately 1.7 ms. The measurement of the flat-top voltage must be performed with an uncertainty value better than 0.5%.

These requirements pose a new measurement challenge as commercial high-voltage dividers are not characterized in the time domain, and the indicated uncertainty values at given frequency ranges are usually not better than 1%. To overcome these difficulties and characterize the dividers' performance for the aforementioned pulses, CERN is building a high-voltage pulsed reference test bed, which includes a reference system supplied by SP Technical Research Institute of Sweden. The reference system is based on a system described in [2].

Manuscript received June 20, 2010; revised September 29, 2010; accepted November 27, 2010. Date of publication January 10, 2011; date of current version June 8, 2011. The Associate Editor coordinating the review process for this paper was Dr. Wan-Seop Kim.

M. C. Bastos is with the European Organization for Nuclear Research (CERN), 1211 Geneva, Switzerland (e-mail: miguel.cerqueira.bastos@cern.ch).

M. Hammarquist and A. Bergman are with the SP Technical Research Institute of Sweden, 501 15 Boras, Sweden (e-mail: maria.hammarquist@sp.se; anders.bergman@sp.se).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIM.2010.2099950

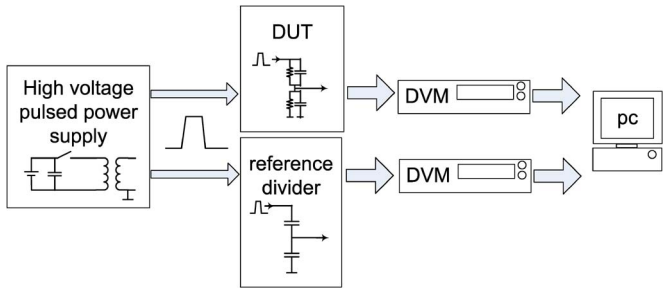

Fig. 1. Block diagram of the test bed.

This paper describes the different elements of the reference test bed. The results of the evaluation and commissioning of the reference system are presented. The analysis and results presented here are an extension of the work described in [3].

II. High-Voltage Test Bed

The high-voltage test bed consists of a CERN-built high-voltage pulsed power supply, which generates the −110 kV/1.7 ms test pulses, a dedicated oil tank where the dividers under test are installed (in the final application, the dividers will be installed in oil), a reference divider, and an acquisition system composed of two HP3458 digital voltmeters (DVMs), which are triggered simultaneously at the pulse start. A block diagram is shown in Fig. 1.

The power supply consists of a bank of capacitors, which are switched into a pulse transformer to generate the test pulses. No droop compensation is foreseen; therefore, the bank of capacitors was dimensioned so that the droop remains below 0.5% for a 1.7-ms pulse. A test pulse with good flat-top stability is desirable although not essential since the measurement is relative to the reference divider, i.e., the error of the device under test (DUT) is calculated by subtracting the value of the reference measurement from the value of the DUT measurement for the flat top of the pulse. Uncertainty is given by the combination of reference divider, DVM, and measurement process uncertainty values.

III. Reference System Requirements

To be able to relate the power supply performance to the RF system's performance, it is convenient to speak in terms of flat-top stability, flat-top noise, pulse-to-pulse repeatability, and long-term drift. Fig. 2 illustrates the meaning of some of these parameters.

For convenience, the reference system used to characterize the power supply's voltage divider must be specified in the same terms. The reference system's requirements are presented

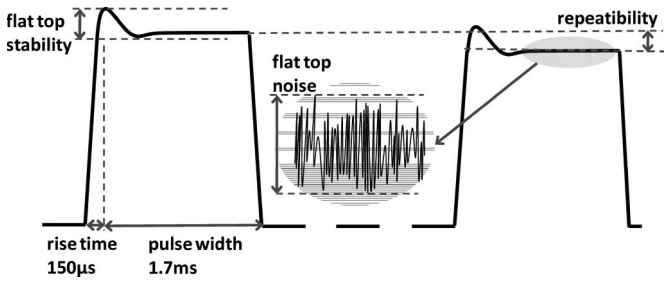

Fig. 2. Pulse characteristics and meaning of main performance parameters.

TABLE I
REFERENCE SYSTEM REQUIREMENTS

Flat top stability (Max allowed flat top level variation)	0.1%
Repeatability (Pulse to pulse, short term stability)	0.1%
1 year stability	0.1%
Flat top noise (>>kHz ripple)	0.1%
Linearity	better than 0.1%

in Table I. The stated requirements are given as percentage of value, except linearity, which is given as percentage of full scale.

In the final application, nominal performance is only required for the last 1.2 ms of the flat top, which corresponds to the moment when the beam is passing through the accelerating cavities. Hence, the reference system requirements presented in Table I refer only to the flat top of the pulse. What happens during rise and fall times is of no interest for this application. Anticipating future needs, the reference-divider nominal voltage was specified to be 150 kV. In the Linac4 test bed, the system will be used to characterize dividers with nominal voltages ranging from 50 to 110 kV; therefore, linearity is an essential requirement.

IV. REFERENCE MEASURING SYSTEM

A. Reference Divider

The reference divider consists of a 100-pF high-voltage gas-insulated capacitor and a 1.5-μF low-voltage capacitor of proprietary design based on high-quality ceramic capacitors. The system is primarily characterized by capacitance measurements. The linearity of the system was investigated by measuring the capacitance of the compressed-gas capacitor over its whole voltage range. The linearity was investigated at power frequency since theoretical considerations of the gas capacitor indicate no correlation between frequency and voltage dependence. In the test, the capacitance changed by an amount of less than 20 ppm from 20 to 150 kV. A 300-kV capacitor, with a voltage coefficient of less than 1 ppm from low voltage to 300 kV, was used as a reference. This reference capacitor was characterized according to the methods described in [4]–[6]. These measurements ensure traceability over the system's entire working range. The voltage coefficient of the low-voltage capacitor was also measured and found negligible.

B. Acquisition System

The acquisition system uses two HP3458 DVMs connected to a personal computer (PC) via a general-purpose interface bus. The DVMs are used in direct-current voltage (DCV) mode at a 50-kS/s sampling rate and a 10-μs aperture. The DCV signal conditioning path has typical bandwidths ranging from 50 to 150 kHz and a settling time inferior to 50 μs (0.01% of the final value) in the lower ranges [7]. Specified external trigger latency is less than 175 ns.

In the high-voltage test bed, the DVMs are controlled by an application running on the control PC. When a measurement is launched, the DVMs are initialized and set to wait for a trigger signal, which is sent by the power supply at the beginning of each pulse. In addition, the reference-divider DVM requires a pretrigger signal. The reason for this is because a measurement of the baseline voltage is required before the pulse start: As the high-voltage divider is capacitive, a residual charge will always be present, and it will cause an offset. This offset needs to be measured and subtracted from the measurement results. This is done by the software upon reception of the pretrigger signal from the power supply.

V. VERIFICATION OF THE REFERENCE SYSTEM

The particular time-domain requirements of this application present a new challenge in the field of high-voltage measurement. The verification of the reference system is in itself a challenge. As there are no better references available to test the reference system against, direct measurements at full scale are of limited interest.

For this reason, a different validation method is proposed in this paper. The proposed approach is to fully characterize the reference system at low voltage and to measure the factors that can affect its performance at higher voltages. By including those factors in the uncertainty analysis, conclusions about the performance of the system at high voltage can be drawn from its low-voltage performance. For this, it is assumed that no coupling exists between error sources.

In the following section, the verification of the system over its entire range of voltage is presented, according to the aforementioned approach.

The scale factor of the divider was established from calibration data for the two capacitors and other contributing factors, such as cable capacitance and DVM input capacitance.

The calibration was done in two steps. The first calibration was performed by SP in Sweden using a current-comparator capacitance bridge, a phase-sensitive null detector, and characterized capacitance standards. The measurement equipment was then brought to CERN, and the final characterization was made after installation of the system to avoid errors due to the different environment, in particular proximity effects.

The scale factor of the system has also been measured directly. This was done by using a test pulse with the aforementioned characteristics and an amplitude of 1 kV (the voltage coefficient is negligible, as discussed in Section IV-A). Both the applied voltage and the output signal from the low-voltage arm were measured using two HP3458 DVMs in the 1-kV and

TABLE II
SCALE FACTOR OF THE SYSTEM, AS CALCULATED BOTH FROM CAPACITANCE AND DIRECT MEASUREMENTS AT SP AND CERN, RESPECTIVELY

Scale factor	
SP, capacitive	15085.21 ± 0.04 %
SP, from 1kV pulse test	15076.6, Std dev=0.005% (five measurements)
CERN, capacitive	15085.20 ± 0.04 %
CERN, from 1kV pulse test	15080.8 ± 0.05 %

100-mV ranges, respectively. From this test, an experimental scale factor can be obtained by dividing the input signal with the output signal as read by the DVMs. The comparison of this value and the value obtained by capacitance measurements can serve as verification of the capacitively determined scale factor. Measurement results are given in Table II.

The difference between the scale factors obtained at SP from capacitive measurements and from the pulse test is 0.06%. The lower value was obtained when the capacitor was in a "free space" (about 4 m to the nearest metallic object). The measurements of the capacitor's proximity effect show that the capacitance value is approximately 0.05% higher in the free space than in its metallic enclosure. Taking this into account, the two results agree well, within respective uncertainty values.

The difference in the scale-factor values determined through capacitance measurements at SP and CERN is negligible. This is the value that will be used for the scale factor in the final test bed since the value resulting from the 1-kV pulse test, although providing a good indication of the scale factor, might have an error due to the droop (see Section VI-B).

VI. UNCERTAINTY ANALYSIS

A. Uncertainty Calculations

The expanded uncertainty of measurement is stated as the standard uncertainty of measurement multiplied by the coverage factor $k = 2$, which, for a normal distribution, corresponds to a coverage probability of approximately 95%. The standard uncertainty has been determined in accordance with the Guide to the Expression of Uncertainty in Measurement [9]. A summarized uncertainty analysis is given in Table III.

TABLE III
SUMMARY OF THE UNCERTAINTY ANALYSIS. THE SENSITIVITY COEFFICIENT IS 1, AND THE DEGREES OF FREEDOM ARE ≥ 50. THE REFERENCE TEMPERATURE IS 23 °C

Uncertainty of high voltage arm			
Contribution	Value	Std uncertainty	Uncertainty contribution
Calibration of HV capacitor	97,4497 pF	0,0007 pF	0,0007 pF
Voltage dependency (20 to 125 kV)	0	0,0012 pF	0,0012 pF
Proximity effect (±50 mm off center)	0	0,0008 pF	0,0008 pF
Long-term drift of HV capacitor	0	0,0011 pF	0,0011 pF
Result	**97,4497 pF**		**0,0019 pF**
Uncertainty of low voltage arm			
Calibration of LV capacitor	1467644 pF	49 pF	49 pF
Voltage dependency	0	3 pF	3 pF
Frequency dependency	0	269 pF	269 pF
Long-term drift of LV cap	0	7 pF	7 pF
Capacitance of HV cable	267 pF	1 pF	1 pF
Capacitance of LV cable	960 pF	5 pF	5 pF
Input capacitance of HP 3458A	280 pF	16 pF	16 pF
Parasitic capacitance of HV capacitor	800 pF	40 pF	40 pF
Result	**1469951 pF**		**277 pF**
Relative uncertainty of measuring system			
Ratio of divider	15085,2	0,000 189 pu	0,000 189 pu
Flat top stability	1	0,000 069 pu	0,000 069 pu
Temperature dependency of HV divider (± 5 K)	1	0,000 014 pu	0,000 069 pu
DVM gain error at short aperture	1	0,000 050 pu	0,000 050 pu
DVM quantisation at 50 kSamples/s and DINT	1	0,000 046 pu	0,000 046 pu
Validation of software used to evaluate trapezoidal voltage	1	0,000 100 pu	0,000 100 pu
Total	**15085,2**	**ratio**	**0,000 245 pu**
Expanded uncertainty	**0,049%**		

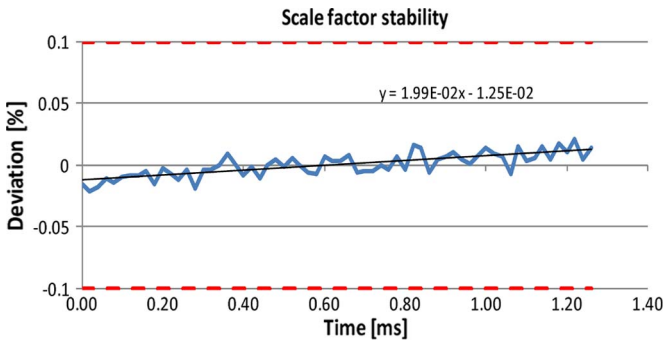

Fig. 3. Stability of the scale factor over the last 1.2 ms of the pulse. The slope of the curve corresponds to the droop.

B. Comments on Selected Uncertainty Contributions

Flat-Top Stability: The flat-top level variation for the reference divider is dominated by a droop. To understand this, the scale factor was determined per sample for one pulse measurement, and the result is depicted in Fig. 3. Both the applied voltage and the output signal from the low-voltage arm were measured using two HP3458 DVMs run by two separate computers. The test voltage was approximately 980 V. The change in scale factor over the last 1.2 ms of the pulse can be used as a measure of the stability of the flat top. The deviation of an instantaneous scale factor from the average scale factor over the last 1.2 ms of the pulse flat top (i.e., the change of the linear curve fit over the measured time span) is approximately 0.024%.

The possible causes of the droop are the leakage current and the frequency dependence of the capacitance of the low-voltage capacitor.

The leakage current of the system is caused by either resistive loading of the capacitor, or leakage and bias currents in the DVM input circuits. The input resistance of the instrument at dc in the 10-V range was measured by applying a known voltage over a known standard resistor in series with HP3458 and by measuring the voltage with the DVM. The input resistance for the instrument is specified to > 10 GΩ [8]. The result for two different measurements was 36 GΩ ± 3% and 60 GΩ ± 9%. Using the mean value of these two measurements, the effect of input leakage current was calculated and found to cause a droop over the 1.5-μF capacitor of less than 1 ppm.

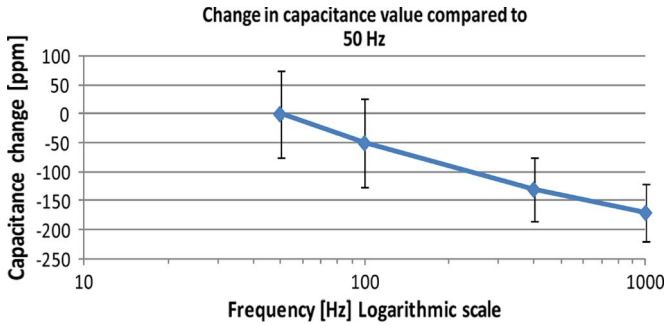

Fig. 4. Frequency dependence of a 10-μF capacitor with a similar design as the one used in the reference divider.

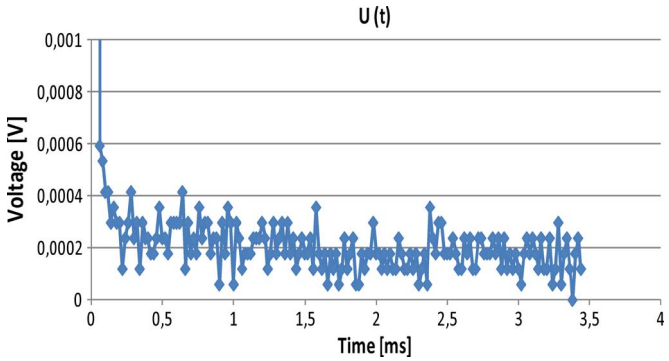

Fig. 5. DVM step response.

As for the frequency dependence of the low-voltage capacitor, a capacitor of a similar design and identical capacitors but with a value of 10 μF have been measured in the frequency span ranging from 50 Hz to 1 kHz. The change between 50 Hz and 1 kHz was measured to be -170 ppm with an estimated uncertainty value of 50 ppm (see Fig. 4).

From the aforementioned results, the frequency dependence of the low-voltage arm would seem to be a plausible cause of the observed droop. In order to correct for this effect, more measurements are needed. For now, an uncertainty contribution is added.

DVM Step Response: The step response of the DVM 10-V range was measured using a DCV source switched by an Hg relay, giving a rise time in the range of 2 ns. A zoom of the step (from 8 to 0 V) is shown in Fig. 5.

The step-response time of the DVM, to a level of within 0.005% of its final value, was found to be within 0.1 ms.

DVM Bias Error: Since the DVM bias error (gain and offset) is not specified for a 10-μs aperture, a test campaign was necessary to characterize the dependence of the DVM error as a function of sampling speed. Several DVMs were measured on the 10-V range at different speeds using a 10-V standard reference voltage. Fig. 6 shows the results for the DVM unit that was chosen for the reference system.

The continuous curve (left-axis scale) shows the bias error in ppm of range. The dotted curve (right-axis scale) shows the peak-to-peak noise for four different measurements. It can be seen that there is a "knee" above which a bias error shows up. This happens at around 5 kS/s, and this error reaches 20 ppm (of range) at 50 kS/s. This value has a negligible impact in the scale factor calculated in the uncertainty analysis; therefore, no

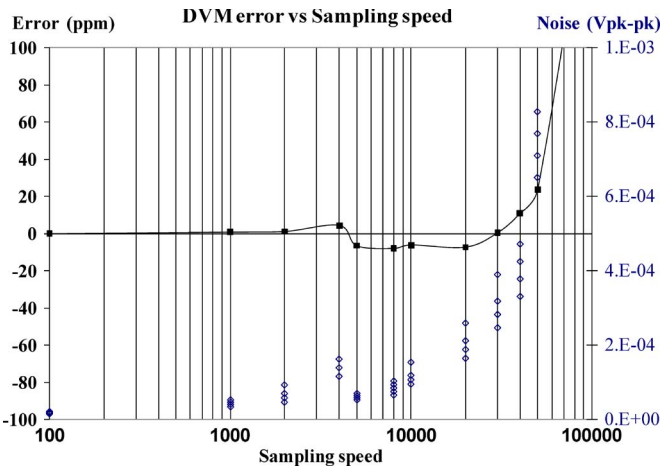

Fig. 6. DVM bias error and peak-to-peak noise versus sampling speed.

correction was included for this. The spread in the amplitude of the error above the "knee" sampling speed for different DVMs is not shown here, but a value on the order of 100 ppm was observed. Therefore, if another DVM is used, a scale factor correction might be necessary.

As for the noise, it increases as expected with decreasing aperture time reaching about 30-ppm root mean square at 50 kS/s. A value of 50 ppm was used for the uncertainty calculations.

Short-Term Stability: Repeated measurements with the capacitance bridge show that short-term stability of capacitance values is excellent, which is less than a few ppm. Heating effects, which are a known source of short-term stability degradation in high-voltage measuring systems, are negligible for a compressed-gas capacitor.

Other effects can conceivably influence the short-term stability of the system, and therefore, evaluation has also been performed through direct measurements at about 1 kV. The scale factor was calculated from the voltage applied to the high-voltage arm divided by the voltage over the low-voltage arm. These voltages were measured by two DVMs triggered simultaneously. For the five measurements taken (pulses $P_1, P_2, \ldots$), the scale factors for each sample of each pulse $(P_1 n_1, P_1 n_2, \ldots)$ were calculated. The average difference between the scale factor of each corresponding sample in the five measurements (e.g., $P_1 n_1$, $P_2 n_1$, $P_3 n_1$, $P_4 n_1$, and $P_5 n_1$) was found to be less than 0.04%. Additionally, all measured points for the five pulses are within 0.08%. In Fig. 7, the deviation of the scale factor (for each sample) from the mean value of the first five samples is shown for the five pulses measured.

Proximity Effects: During the characterization of the compressed-gas capacitor, it was found that this individual has an uncommonly large proximity effect. Capacitance was measured in SP's laboratory with the capacitor placed in a quadratic metallic cage, for different positions in the cage and with varying side length. Moving the capacitor 0.1 m off the center in a cage with a 1.8-m side length caused a change in the capacitance value by about 16 ppm.

At CERN, the compressed-gas capacitor is permanently installed in a metallic cage, which means that the surroundings are fixed, and therefore, proximity errors can be eliminated by

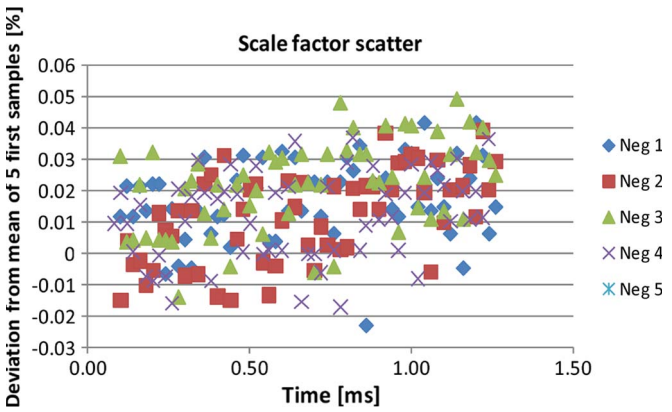

Fig. 7. Deviation of the instantaneous scale-factor value from the average of the first five values in five different pulses.

in situ calibration of the divider. During commissioning of the reference system, care was taken to fix the capacitor well in its final position in the test bed to avoid modification in the distances to surrounding objects.

Temperature Effects: The capacitors were put in a climatic chamber, and the variation of capacitance with temperature was measured. The low-voltage capacitor was measured between ca. 20 °C and 40 °C. Its temperature coefficient was less than 4 ppm/°C.

The high-voltage capacitor was measured at ca. 20 °C and ca. 30 °C, which are both at steady state. The capacitance was furthermore recorded at different times during the warm-up process. The settling time to within 5% of the step value was estimated to approximately 6 h. A temperature coefficient of 20 ppm/°C was obtained. In the uncertainty analysis, an uncertainty contribution for the whole system corresponding to a temperature change of ±5 °C was added.

VII. Test Bed: Experimental Results

The characterization of the reference system, as described in the previous sections, showed that it performs within the specified requirements for this application. The results presented in this section illustrate the operation of the complete test bed when used in the evaluation of commercial voltage dividers at −110 kV. These dividers are to be used in the klystron modulator power supplies. The main requirements for the dividers are the following: 0.5% initial calibration uncertainty, flat-top stability better than 0.25%, and pulse-to-pulse repeatability better than 0.25% (see Fig. 2 for definition details).

The tests were performed with a prototype of the klystron modulator power supply [10] as the test-bed power supply was not available. The prototype power supply generates −110 kV and 50/1000 μs pulses although with a 10% droop. The droop does not affect the measurements as they are always performed with respect to the reference system. The power supply was pulsed at −110 kV, and the pulses were measured by the reference divider in parallel with the commercial divider under test, which, in this case, is a compensated resistive divider (VD110B) from North Star High Voltage. The outputs of both the reference divider and VD110B were measured using two

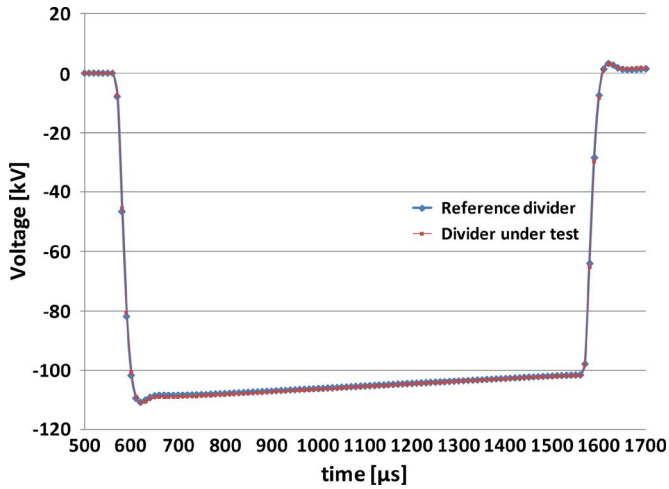

Fig. 8. Reference divider versus VD110B-1: −110-kV complete pulse.

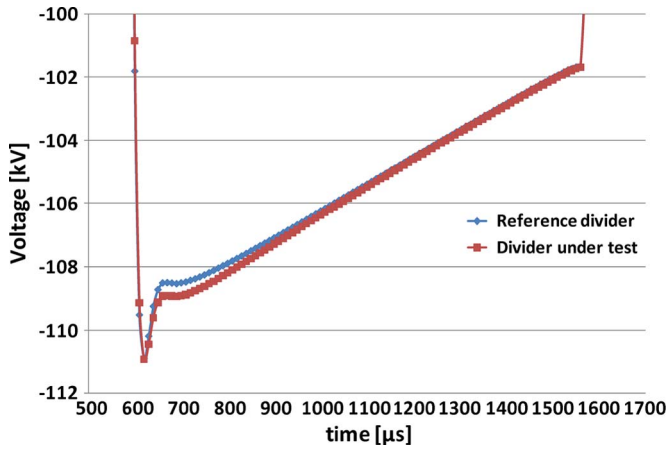

Fig. 9. Reference divider versus VD110B-1: zoom of the −110-kV pulse flat top.

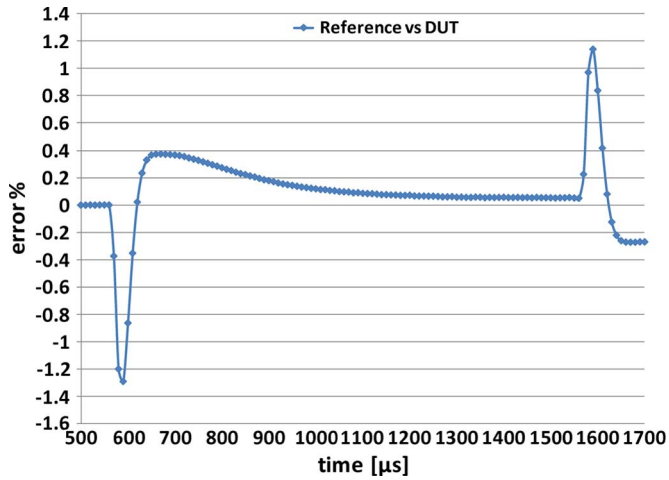

Fig. 10. VD110B-1 error during the −110-kV pulse.

DVMs at a 50-kS/s sampling rate and a 10-μs aperture. The results are presented in Figs. 8–12.

Fig. 8 shows the complete −110-kV pulse, as measured by the two dividers. Fig. 9 shows a zoom of the flat top of the same pulse, and Fig. 10 shows the VD110B error in relation to the reference system, in percentage of full scale.

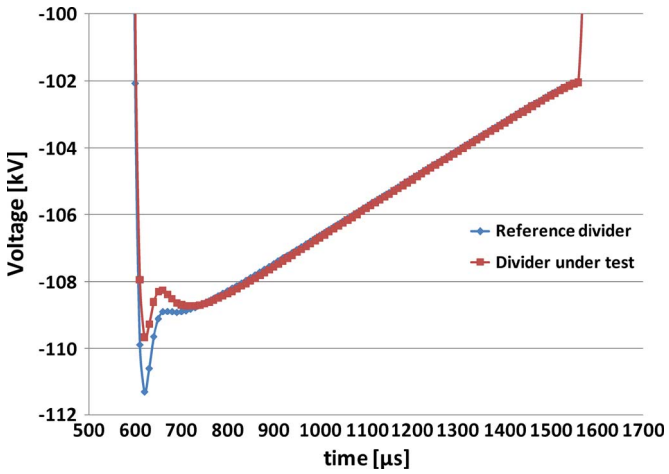

Fig. 11. Reference divider versus VD110B-2: zoom of the −110-kV-pulse flat top.

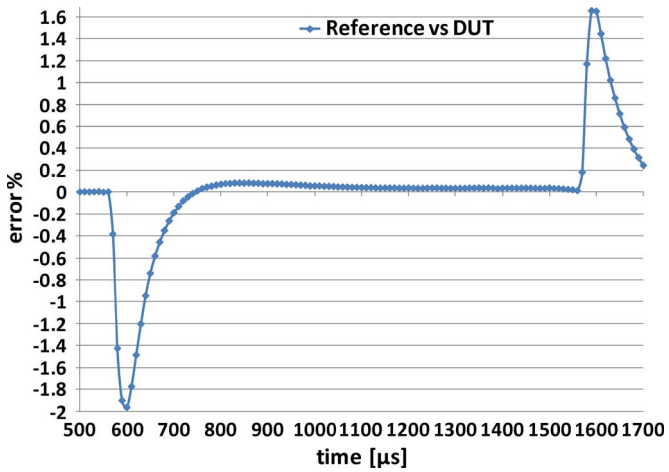

Fig. 12. VD110B-2 error during the −110-kV pulse.

The same test was performed with a different unit of VD110B. The results are depicted in Figs. 11 and 12.

The results show that the test bed performs as expected at high voltage, providing an easy method for evaluating the performance of voltage dividers for the described application. A simple analysis of the results allows an easy comparison of the response of the two VD110B probes: VD110B-1 shows a faster response albeit with a higher overshoot, whereas VD110B-2 shows less overshoot at the expense of a longer settling time. The difference in their dynamic behavior is most likely related to the adjustment of the capacitive compensation. These results could be used to adjust the capacitive compensation in order to obtain a better dynamic response. Initial calibration (ratio) errors on both VD110B units are below 0.1%, hence within specification. Again, it should be recalled that only the flat-top measurement performance is relevant for this application.

The acquisition system performs as expected. A trigger provided by the power supply 1 ms before the pulse is used for the zero calibration, and then, a second trigger at the start of the pulse is used to trigger the two DVMs simultaneously. The number of points obtained during the flat top is enough for the evaluation of the system's performance according to the specifications presented in Table I. However, if a higher sampling rate is required, the system allows for a maximum sampling speed of 100 kS/s albeit with an aperture of 1.4 μs and the limitations already presented in Fig. 6.

VIII. Conclusion

A high-voltage reference test bed for the evaluation of high-voltage dividers for pulsed applications was built at CERN. A reference system has been developed, produced, and evaluated by SP. The results show that the reference measuring system fulfills or exceeds the requirements for the application, having an uncertainty value of 0.049% at $k = 2$. The test bed provides a valuable tool for the evaluation of commercial voltage dividers for pulsed applications.

References

[1] R. Garoby, F. Gerigk, K. Hanke, A. M. Lombardi, M. Pasini, C. Rossi, E. Sargsyan, and M. Vretenar, "Linac4, a new injector for the CERN PS booster," in *Proc. EPAC*, Edinburgh, U.K., 2006.

[2] H. Tang and A. Bergman, "Development and evaluation of a high resolution measuring system for a switching impulse measurement," in *Proc. CPEM*, Sydney, Australia, May 14–19, 2000, pp. 355–356.

[3] M. C. Bastos, M. Hammarquist, and A. Bergman, "A high-voltage reference testbed for the evaluation of high-voltage dividers for pulsed applications," in *Proc. CPEM*, 2010, pp. 667–668.

[4] W. A. Nash, *Theory and Problems of Strength of Materials*, 2nd ed. Birmingham, U.K.: McGraw-Hill, 1987.

[5] L. Hans-Georg, "Über den Einfluss von Spannung und Frequenz aud die Kapazität von Hochspannungs-Druckgaskondensatoren," Von der Fakultät für Maschinenbau und Elektrotechnik der Technischen Universität Carola-Wilhelmina zu Braunschweig, 1989.

[6] L. Hans-Georg, "Voltage-induced capacitance variation in high-voltage compressed gas capacitors due to electrode flexibility," Physikalisch-Technische Bundesanstalt, Braunschweig, Germany, Aug. 1990.

[7] D. A. Czenkusch, "High-resolution digitizing techniques with an integrating digital multimeter," *Hewlett-Packard J.*, vol. 40, no. 2, pp. 39–49, Apr. 1989.

[8] *Agilent Technologies 3458A Multimeter Calibration Manual*, Edition 3, Manual Part Number: 03458-90017.

[9] *Evaluation of Measurement Data—Guide to the Expression of Uncertainty in Measurement*, JCGM 100:2008 (GUM 1995 with minor corrections).

[10] C. A. Martins, F. Bordry, and G. Simonet, "A solid state 100 kV long pulse generator for klystrons power supply," in *Proc. 13th Eur. Conf. Power Electron. Appl., EPE*, Barcelona, Spain, Sep. 8–10, 2009, pp. 1–10.

Miguel Cerqueira Bastos was born in Porto, Portugal, in 1975. He received the University degree in electrical and computer engineering from the University of Porto, Porto, Portugal, in 1999.

After initially working as a Project Engineer on traffic information systems with EFACEC, Matosinhos, Portugal, he joined the European Organization for Nuclear Research (CERN), Geneva, Switzerland, in 2002 as a Project Engineer in analog electronics, with particular emphasis on precision current measurement and analog-to-digital conversion. From 2002 to 2008, he participated in the development and characterization of high-accuracy calibration instruments and current transducers for the power converters of the Large Hadron Collider (LHC) at CERN. Since December 2008, he has been the Section Leader of the High-Precision Measurements Section, Electrical Power Converters Group, CERN. As such, he is responsible for all the high-precision aspects of CERN's power converters and, in particular, the operation of the LHC calibration system and the electrical standards laboratory. More recently, he has been working in the precision measurement of high voltage and current pulses for linear accelerator applications.

Maria Hammarquist was born in Stockholm, Sweden, in 1975. She received the M.Sc. degree in engineering physics from Chalmers University of Technology, Göteborg, Sweden, in 2000.

In 2000, she joined SP Technical Research Institute of Sweden, Boras, Sweden, working with the primary standards and high-precision direct-current/low-frequency electrical measurements and calibration. Since 2009, she has been with the Electrical Power Group, SP, working with high-voltage and high-current calibration and measurements.

Anders Bergman was born in Överluleå, Sweden in 1948. He received the B.Sc. degree in physics and the Ph.D. degree from Uppsala University, Uppsala, Sweden, in 1971 and 1994, respectively. His Ph.D. thesis, which is entitled "In situ calibration of voltage transformers on the Swedish National Grid," is based on the results of a project to calibrate the total complement of voltage transformers on the Swedish 220- and 400-kV grids.

After being involved in the design and construction of a 100-MeV cyclotron with Scanditronix, Uppsala, he moved to the high-voltage laboratory of Allmänna Svenska Elektriska Aktiebolaget (ASEA), Stockholm, Sweden, in 1977, where he was engaged in the metrological aspects of high-voltage testing, with main emphasis on impulse voltage and partial discharges. Since 1988, he has been with SP Technical Research Institute of Sweden, Boras, Sweden, where he is responsible for calibration activities for high voltage and current. He is primarily engaged in calibration activities in fields of high-voltage engineering, which are needed by industry, and he has developed several major reference systems that are used for on-site calibration of high-voltage measurement systems. He is involved in international standardization, mainly within the International Electrotechnical Commission Technical Committee 42, high-voltage test techniques, as a Convenor of Working Group 20, and instruments and software used for measurements in high-voltage and -current tests. Since September 2010, he has been coordinating a three-year research project for metrology for high-voltage direct current, with participation from eight other European bodies. The project is funded by the European Commission.