Assessment of non-linearities for precision DACs

J.L. Blanco-Murillo, *Member, IEEE*, V.Yagüe-Jiménez and F.J. Casajús-Quirós

Abstract

One may identify two independent sources of non-linearities in digital-to-analog converters: (i) deviations at input sources and switches, (ii) non-idealities in the posterior summation circuit. The first are described by specific figures of merit, mainly INL and DNL; the second, in terms of standard amplifier performance (e.g., THD, etc.). Performance is assessed without considering prior separation of the two, resulting in misleading characterization. We address cross-influence of (i) and (ii), and propose a novel figure of merit for band-pass response that separately addresses nonlinear deviations and memory effects attending to DACs inner structure.

Index Terms

Digital-to-Analog converter, linearity, performance evaluation, system testing, generalized Hammerstein systems

I. Introduction

Digital-to-Analog converters (DACs) are at the crossroad between the digital and analog worlds. Throughout the years, different layouts have been proposed for such devices; but performance has always been characterized using the same figures of merit, while focusing on the expected, overall linear behavior.

Linearity can only be achieved by overcoming all possible random and systematic deviations [1], [2]; arising both during manufacturing and operation. In the past, technologies' matching properties received most of the attention; whereas performance assessment must cover all affecting variables and their interactions, requiring an informed model for the system. Early contributions focused on the calibration of digital-to-analog converters, assuming an underlying static, linear model. In [3] offset and gain parameters were discussed, in relation to spurious deviations in bit-currents (i.e., one source per bit). With this idea in mind, in [4] a low rate, supposedly linear DAC was proposed, based on a single bit (single source), to mitigate the aforementioned influence of matching properties. Contrarily, reported results evidenced that a spurious, non-linear effect was still present.

In [5] authors proposed a purely nonlinear, static model that was used for calibration in [6]; and further extended for high-resolution DACs in [7]. These contributions, along with many others promoted the extensive use of the integral non-linearity (INL; followed, or not, by its counterpart the differential non-linearity, DNL) as in [8], [9]

The authors are with the Signal Processing Applications Group, Univ. Politécnica de Madrid, Spain. Dr. Yagüe-Jiménez is also with the Instituto de Tecnologías Físicas y de la Información (ITEFI), Spanish National Research Council, Spain.

Work supported under grant TEC2012-38402-C04-1 from the Spanish Ministry of Economy and Competitivity.

and [10]. These figures describe the static (time-independent) differences between quantization levels, evaluated at DACs' respective outputs.

Work has been reported on the characterization of INL; particularly with regard to its statistics, and specifically to its variance [11]. Results evidenced that through the assessment of INL statistics the relevance of intermodulation errors can be assessed. The impact of these deviations on the generated waveforms was extensively addressed in [12]. There, clock modulation was also addressed, in addition to the vertical deviations still being modelled by means of INL.

Interestingly, INL is not inmediate to evaluate, and its statistics are likely to be biased by the selected peak detection process. This was suggested in [13], where authors addressed the variance assessment via the root-mean square value of sinusoidal signals. This is certainly a more robust approach, but focuses on low-frequency (up to audio ranges according to the authors), monofrequency sinusoids. Contrarily, one may prefer to look at power distribution (i.e., variance or RMS values) for the individual order-dependent, intermodulation products; while addressing a wide range of frequencies.

The aim of this contribution is to rework the figures of merit describing DACs' nonlinearities. Taking into consideration the internal structure and the electronic components that are most typically embedded inside a DAC, we propose an informed, cascade model; extending that in [5]. This is intended to provide a closer description of the system and explain the nature of the deviations observed.

The rest of the paper is organized as follows. In Section II we describe the general structure and ideal performance of a DAC component, following the standard simplifications described in the literature. While reviewing these in Section III, we identified several limitations of this model. There we derive an alternative, informed linear model (III-A); revisit the figures of merit described in the literature for distortion assessment when applied on the postulated system model (III-B), and propose a suitable procedure that matches the latter (III-C). In Section IV we describe the assessment of two DAC commercial components, while conclusions and future work are included in Section V.

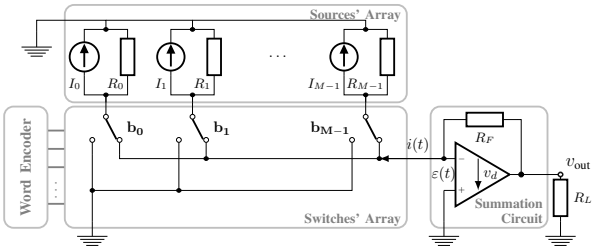

Fig. 1. Equivalent circuit model describing the general structure of a DAC.

II. General structure and ideal performance

Generally speaking, the electronics of an N-bit DAC is formed from the cascade of two blocks as depicted in Fig. 1: (i) a set of individual currents (voltages) sources, followed by a switching array, and (ii) a summation step. The structure of module (i) depends on the design of the DAC. Two of the most frequent structures are thermometer

decoded and ladders; which otherwise may appear in combination. Their goal is to produce individual sources of fixed value(s). Subsequently, module (ii) allows sources' summation, depending on the preceding arrays, impedances $\{R_k\}$ and reference R_F.

Regardless of the inner structure of module (i), let us consider a set of M sources [1]. To these we refer by their outgoing currents, $\{I_k\}_{k=0,\dots,M-1}$, as for a current steering DAC or their Norton equivalents. For steady state analysis around the differential voltage input (V_d) and output (V_{out}) of the amplifier in Fig. 1, one would have from Kirchhoff's current/voltage laws that

$$\begin{aligned} V_d = &\quad V_+ - V_- = -V_- \\ V_{\text{out}} = &\quad -a_0 + a_1 \cdot V_d \qquad \text{[linear, no delay]} \\ V_{\text{out}} - V_- = &\quad R_F \cdot I \end{aligned} \tag{1}$$

with some typical (a_0, a_1), resulting in the well-known virtual ground principle (VGP)

$$\begin{aligned} V_- = &\quad -\left[I \cdot R_{\text{F}} + a_0\right] / [a_1 + 1] \to 0, \quad \text{with } a_1 \to \infty \\ V_{\text{out}} \to &\quad R_F \cdot I = R_F \cdot \left[\sum_{k=0}^{M-1} b_k^{(n} \cdot I_k\right] = R_F \cdot [\mathbf{w}_n^{\intercal} \cdot \mathbf{I}] \end{aligned} \tag{2}$$

where binary coefficient $b_k^{(n}$ governs the k-th gate (0 close, 1 open) between $(n-1)T_{\text{clk}} < t \leq nT_{\text{clk}}$, and is encoded at the k-th position of n-th digital word, $\mathbf{w}_n$. The latter, results from the digital signal generation process:

$$x(t) \mapsto x(nT_{\text{clk}}) \mapsto x[n] \mapsto \mathbf{Q}(x[n]) \mapsto \mathbf{w}_n \tag{3}$$

Digital word $\mathbf{w}_n$ (binary as for Fig. 1 or not) is produced by $\mathbf{Q}(\cdot)$, a M'-levels, uniform quantizer applied on the discrete-time sequence $x[n]$.

Let us focus on the signals connecting the blocks $(i, \varepsilon)(t)$ in Fig. 1. These represent, respectively, the time-varying current produced by the source's array and traversing the summation loop, and the voltage at the inverting input V_-. In other words, the inputs of the summation circuit. In steady state: $i(nT_{\text{clk}}) \to \mathbf{w}_n^{\intercal} \cdot \mathbf{I}$ and $\varepsilon(nT_{\text{clk}}) \to 0$; whereas time evolution under 1^{st}-order intersymbol interference assumption produces,

$$i(t) = \textstyle\sum_{k=0}^{M-1} I_k \cdot p_k(t|b_k^{(n} - b_k^{(n-1)}), \quad \begin{matrix} \mathbf{w}_{n-1} \to \mathbf{w}_n \\ (n-1)T_{\text{clk}} < t \leq nT_{\text{clk}} \end{matrix} \tag{4}$$

with $p_k(t|b_k^{(n} - b_k^{(n-1)})$ the pulse describing k-th gate's time evolution due to its immediately prior ($b_k^{(n-1)}$) and current ($b_k^{(n}$) status, and such that $p_k(t = nT_{\text{clk}}|b_k^{(n} - b_k^{(n-1)}) = b_k^{(n}$ so it produces ideal reconstruction for synchronized clocks [18],[19],[20].

In spite of the ideal, linear model for the DAC, in this contribution we hypothesize that:

1) a nonlinear (NL) model is needed to describe summation circuit behaviour, instead of $v_{\text{out}}(t)/R_F \propto i(t)$;
2) spurious voltages are to be expected due to dynamic evolution, despite VGP simplification ($\varepsilon \to 0$);

3) sensible deviations affect sources (currents, $\{I_k\}$, and impedances, $\{R_k\}$) producing $\{\tilde{I}_k\}$ and $\{\tilde{R}_k\}$, respectively [1].

Based on these and the seemingly independent deviations affecting modules (i) and (ii); we must establish a suitable and informed, nonlinear model that is specific of the D/A conversion process, incorporates the nonidealities previously described, is easy to evaluate and interpret.

III. DAC SYSTEM MODEL

Hereafter we describe the proposed nonlinear model. First we enunciate the model itself, which is derived from the prior hypotheses. Then, attending to the resulting structure, we review several figures of merit for DACs' performance assessment described in the literature and included in most datasheets. Finally, we derive a novel procedure based on the proposed structure.

A. Informed nonlinear model

In light of the three previous hypotheses, let us consider the non-ideal current, flowing between blocks (i) and (ii),

$$\hat{\tilde{i}}(t) = \sum_{k=0}^{M-1} \Big[\underbrace{\tilde{I}_k}_{\text{source}} \cdot \underbrace{p_k(t|b_k^{(n} - b_k^{(n-1)})}_{\text{switch response}} - \underbrace{\varepsilon(t)/\tilde{R}_k}_{\text{summation loop}} \Big] \tag{5}$$

for $\mathbf{w}_{n-1} \rightarrow \mathbf{w}_n$, $(n-1)T_{\text{clk}} < t \leq nT_{\text{clk}}$, and with $\varepsilon(t)$ the actual voltage at the inverting input (V_-) of the amplifier. The latter expression addresses contributions from the sources' and switches' arrays, which may deviate from the ideal static behavior based on hypothesis 2) and 3); as well as from the summation module, involving a negative feedback loop and the ideal summation of currents. This is unavoidably affected by sources' impedances, $\{\tilde{R}_k\}$, displays characteristic dynamic evolution and NL behavior (hypotheses 1 and 2).

The aggregated effect encapsulated in (5) may be formulated in terms of a nonlinear, cascade system as the one depicted in Fig.2. The output of this may be written as

$$\tilde{\tilde{i}}(t) = \sum_{k=0}^{M-1} \tilde{I}_k \cdot p_k(t|b_k^{(n} - b_k^{(n-1)}) \tag{6}$$

$$v_{\text{out}}(t) = h_0 + \sum_{r=1}^{Q} h_r(t) * \left(R_F \cdot \tilde{\tilde{i}}(t)\right)^r \quad \text{[NL, mem.]} \tag{7}$$

where (6) incorporates deviations at sources and switches, as well as quantization noise whenever a digitized signal is considered (block i), and (7) deviations referring to the summation circuit (block ii). These include a static nonlinearity, in the same way as [5], but extends this by introducing a spurious memory effect.

This particular structure originates from the assumption of low prior memory effect found in amplifiers [15], [16]. Additionally, due to the relatively rapid responses (low memory) at the switching gates, here we assume that the overall system behavior (incorporating effects due to sources, switches and summation) may be described by a single generalized, Hammerstein network, only considering diagonal, order-dependent kernels' ($h_r(t)$) up to order Q [17]. Such structure considers:

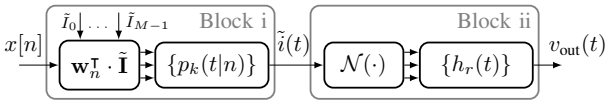

Fig. 2. Block diagram describing the nonlinear model for a DAC.

1) a nonlinear connection $\mathcal{N}(\cdot)$ between the traversing current and the output voltage, up to a given order, $1 \leq r \leq Q$;
2) time- and input-dependent evolution, depending on the order of the nonlinearity, $\{h_r(t)\}$;
3) deviations at the input sources, $\tilde{I}_k$, and gates' responses, $p_k(t|b_k^{(n} - b_k^{(n-1)})$, conditioning the summated current;

ultimately incorporating all nonidealities previously listed. This model may be fully validated through system identification, provided that one could access the traversing current, $\tilde{i}(t)$. Meanwhile, the methodology that we propose for linearity assessment, and the resulting figure of merit, already evidence the adequateness of the model. This is discussed in Sections III-C and V. We shall now evaluate how figures of merit from the literature perform on this.

B. Distortion assessment

In assessing DAC's performance [2] one will frequently find several figures of merit focusing on different distortion effects. Among these are INL (Γ_k) and DNL (γ_k):

$$\Gamma_k = (\tilde{I}_k - \tilde{I}_0)/\tilde{I}_{\text{LSB}} - k \qquad \gamma_k = (\tilde{I}_{k+1} - \tilde{I}_k)/\tilde{I}_{\text{LSB}} - 1 \tag{8}$$

with $0 \leq k \leq M-1$ sources, $\tilde{I}_k$ the actual current produced by the k-th source, and $\tilde{I}_{\text{LSB}} = (\tilde{I}_{M-1} - \tilde{I}_0)/M$. These are related to static deviations from the ideal, linear transfer characteristic, and therefore should be close to zero.

Assuming $\tilde{I}_k = I_k(1+\alpha_k)$, $\{I_k\}$ the expected currents and $\{\alpha_k\}$ the respective tolerances, these may be used to write

$$\tilde{I}_{k+1} = \quad \tilde{I}_0 + \tilde{I}_{\text{LSB}} \cdot [\Gamma_k + \gamma_k + (k+1)] \tag{9}$$

$$\alpha_{k+1} = \quad [\Gamma_k + \gamma_k] \,/\, \left(k + 1 + \tilde{I}_0/\tilde{I}_{\text{LSB}}\right) \tag{10}$$

so at sampling instant, the current in (6) takes value

$$\tilde{i}(nT_{\text{clk}}) = \mathbf{w}_n^\intercal \mathbf{I} + \mathbf{w}_n^\intercal(\bar{\alpha} \circ \mathbf{I}) \tag{11}$$

where $\circ$ stands for the element-wise, Hadamard product. For the sake of simplicity, we consider $\tilde{I}_0 \approx 0$, and consequently $\bar{\alpha} \circ \bar{k} \approx \bar{\Gamma} + \bar{\gamma}$. Hence, for $(n-1)T_{\text{clk}} < t \leq nT_{\text{clk}}$,

$$\tilde{i}(t) = \overbrace{x[n] \cdot \textstyle\sum_{k=0}^{M-1} p_k(t|n)}^{\hat{x}(t)\text{: Reconstructed signal}} + \overbrace{\textstyle\sum_{k=0}^{M-1} \alpha_k I_k p_k(t|n)}^{\xi(t)\text{: NL distortion - Block 1}} \tag{12}$$

with $p_k(t|n) = p_k\left(t|b_k^{(n} - b_k^{(n-1}\right)$ relating to the pulse describing the k-th gate's time evolution previously referred, and representing here the interpolation pulses that produce the reconstructed signal, $\hat{x}(t)$, from digital sequence $x[n]$.

Then, following from (7) and addressing quantization effect, $x(t) = \hat{x}(t) + q(t)$, system output may be written as:

$$\begin{aligned} v_{\text{out}}(t) = \; & [R_F h_1 * x](t) + h_0 + \overbrace{\textstyle\sum_{r=2}^{Q} \left[h_r * \left(R_F \tilde{i} \right)^r \right](t)}^{\text{NL distortion - Block 2}} \\ & + [R_F h_1 * (\xi + q)](t) \end{aligned} \tag{13}$$

First addends represent a linear transformation on $x(t)$; the others are noise and distortion terms due to the hypothesized effects and the proposed system model.

From (13), and considering some full-scale (F.S.) amplitude, low-frequency tone for INL and DNL computation as in [2],[21]: $x[n] = A_{\text{F.S.}} \sin(2\pi n f_0 / f_s)$, the subtraction of the expected and actual outputs produces:

$$\begin{aligned} & (v_{\text{out}} - R_F H_1(f_0) \cdot x)(t) \approx \\ & \quad \approx h_0 + R_F H_1(f_0) \left[\xi + q + \textstyle\sum_{r=2}^{Q} \frac{H_r(f_0)}{H_1(f_0)} R_F^{r-1} \tilde{i}^r \right](t) \end{aligned} \tag{14}$$

with $H_r(f_0)$ the frequency response to the excitation central frequency of the r-th nonlinearity order, memory term, $h_r(t)$. It is a frequency-, time- and NL-dependent distribution, unlike the INL and DNL figures. Thus, these figures may not be directly estimated from the system output.

Moreover, datasheets also include the total harmonic distortion (THD), a measurement of the harmonic distortion present, defined as the ratio of the sum of powers of all harmonic components ($m \geq 2$) to that of the fundamental ($m = 1$) of a monotone of frequency f.

Under the proposed system model, we find that

$$\text{THD}(f) \approx \sqrt{\textstyle\sum_{m=2}^{Q} [R_F^m |G_m(f)|]_m^2(f)} \Big/ [R_F |G_1|(f)] \tag{15}$$

with $G_m(f) = \sum_{r=1} c_{rm} \cdot H_r(f)$, $\{c_{r,m}\}$ the coefficients from Chebyshev polynomials [14]. Thus, THD provides a monotone analysis of the nonlinear behavior of the system and is highly conditioned by memory effects. These are limiting factors when complex signals are involved.

Finally, one may also take into consideration other figures, such as the intermodulation distortion (IMD) describing the ratio between fundamental tones' (f_1, f_2) and order distortion products' (p_1, p_2) power. Once again, considering the proposed system model, we observe that for an input sequence

$$x[n] = A_{\text{F.S.}} \left[\sin(2\pi n f_1 / f_s) + \sin(2\pi n f_2 / f_s) \right]$$

one would expect for the r-order IMD product:

$$\text{IMD}_r(f_1, f_2) \approx A_{\text{F.S.}}^{r-1} \sqrt{\sum_{|p_1|+|p_2|=r} d_{p_1,p_2} \frac{H_r(p_1 f_1 + p_2 f_2)}{\sqrt{H_1(f_1) + H_1(f_2)}}} \tag{16}$$

This figure is still not descriptive for complex signals (beyond pairwise combination of monotones), and is still highly conditioned by memory effects, just as THD.

Thus, we conclude that none of these standard figures of merit could be directly estimated from the system output whenever the proposed nonlinear model matches the system overall behavior.

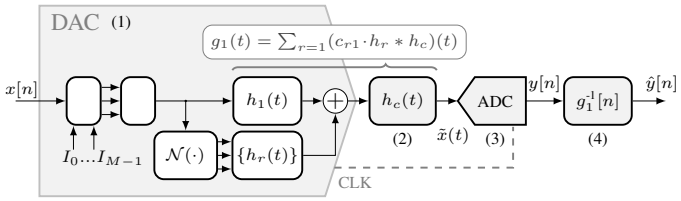

Fig. 3. Block diagram describing the evaluation setup.

We propose a novel procedure that separately addresses the aforementioned sources of non-ideal behavior, and satisfactorily describes the underlying system.

C. Proposed nonlinearity assessment procedure

From (12) and (13), let us consider the setup in Fig. 3. This involves: (1) the device under test (i.e., the DAC; the model for which is taken from Fig. 2), (2) a linear model for the connection of the DAC to (3) a calibrated analog-to-digital converter (ADC), including cable, connectors, etc.; and (4) a post-equalization step. The latter shall compensate colouring effects on the first order response, including high order contributions —$\sum_r c_{r1} \cdot h_r(t)$, see [14]— as well as connection's response —$h_c(t)$.

The signal obtained from the latter setup shall then equate

$$\begin{aligned} \hat{y}[n] &\approx \tilde{q}'[n] + g_1^{-1}[n] * [h_c * v_{\text{out}} + \eta](nT_{\text{ADC}}) \approx \\ &\approx \underbrace{x[n]}_{\text{Input}} + \Big(\underbrace{\xi' + q' + \tilde{q}' + \eta'}_{\text{L Block i + } \mathbf{Q}\text{'s + Noise}} + \underbrace{\textstyle\sum_{r=2}^{Q} g_1^{-1} * h_c * g_r * \left(R_F \tilde{i}\right)^r}_{\text{NL Block ii (NL Block i)}} \Big)[n] \end{aligned} \tag{17}$$

with $g_r[n] = \sum_{m=1} c_{mr} \cdot h_m[n]$, and only for synchronized DAC and ADC, while considering additive, white, gaussian, measuring noise (η), quantization noises $(q, \tilde{q})$ due to DAC and ADC, respectively; as well as a linear component of distortion (ξ) due to block (i). Primed terms result from the aforementioned post-equalization via $g_1^{-1}[n]$.

According to (6) and (17), and assuming negligible memory effect due to the switches' array [15], setup in Fig. 3 displays the structure of a generalized, Hammerstein network, including:

1) a prominent linear term associated to the input sequence,
2) additive, order-dependent, distortion terms,
3) an additive, filtered noise term.

In identifying generalized Hammerstein systems such as the hypothesized one, long, full-scale, exponential, sweep-sine, chirp pulses may be used [14]. This analog signal may be mathematically formulated as

$$\begin{aligned} e(t) &= A_{\text{F.S.}} \cdot \sin\left(\phi(t)\right) \\ \phi(t) &= 2\pi T f_0 \left((f_1/f_0)^{(t-t_0)/T} - 1 \right) / \log(f_1/f_0) + \phi_0 \end{aligned} \tag{18}$$

where $A_{\text{F.S.}}$ is the full-scale amplitude, $T \gg T_{\text{clk}}$ is the pulse duration, (ϕ_0, t_0) are some convenient phase and time initial values, f_0 and f_1 the prefixed, lower and upper frequency bounds, respectively. Here we use a digitalized version of the former, $e[n]$, and cover the following steps:

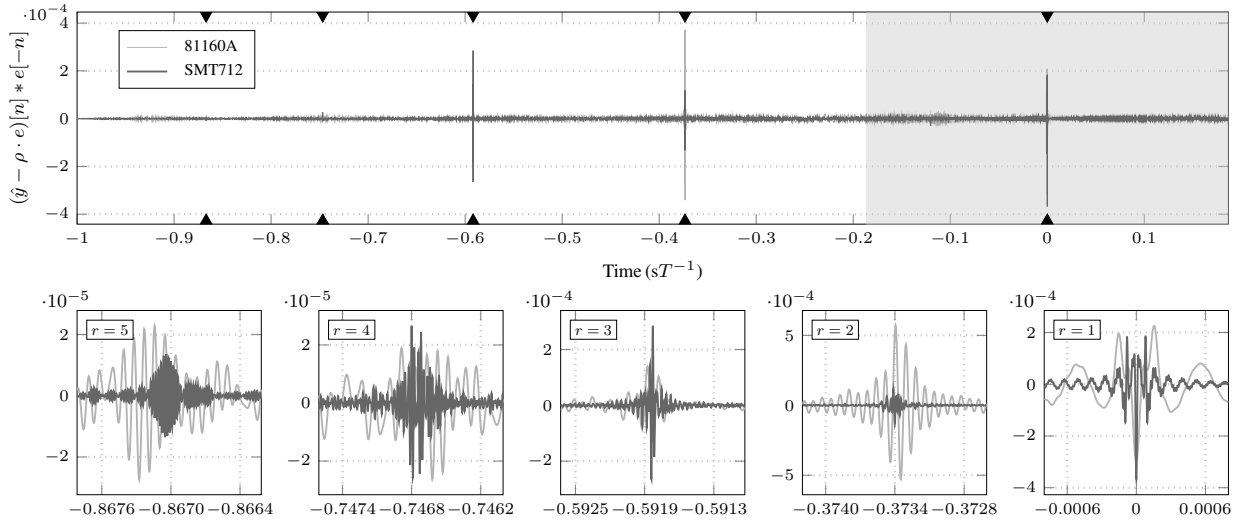

Fig. 4. Time-domain NL residue for Agilent's 81160A and Sundance's SMT712. Triangular markers located at $\log_k(r)\cdot T^{-1}$ determine the location of the order-dependent contributors, $1\leq r\leq 5$. Below, we zoom around each of these, where differences between the two commercial components become apparent. Particularly, as we compare their amplitudes we observe a larger second-order contributor for 81160A —see $r=2$.

Step 1: input the DAC and compute the linear part of the generalized Hammerstein model (see Fig. 3); then, estimate a reliable inverse response such as

$$g_1^{-1}[n]=\mathcal{F}^{-1}\left\{\frac{\mathcal{F}\{(e[-n]*e[n])[m]\}}{\mathcal{F}\{(e[-n]*y[n])[m]\}}(f)\right\},\qquad \begin{array}{l} f_0\leq f\leq f_1\\ |m|\leq\lfloor n_2/2\rfloor\end{array} \tag{19}$$

where $\mathcal{F}$ stands for the Fast Fourier Transform and $n_2=\lfloor\log_k 2\cdot f_s\rfloor$. Then compute $\hat{y}[n]$ and the system residue

$$\begin{aligned} s[n]=(\hat{y}-\rho e)[n]*e[-n]\approx\ & (\xi'+q'+\tilde{q}'+\eta')[n]*e[-n]+\\ & +\textstyle\sum_{r=2}^{Q}R_F^r\cdot\hat{g}_r[n+n_r]\end{aligned} \tag{20}$$

with $\rho=\|y[n]*e[-n]\|/\|e[n]*e[-n]\|$ the ratio between output's and ideal linear response's power, $n_r=\lfloor\log_k(r)\cdot f_s\rfloor$ for $2\leq r\leq Q$, f_s the ADC recording sampling rate and finally, $\hat{g}_r[n]=(g_1^{-1}*g_r)[n]$, the remaining, order-dependent memory effects.

Step 2: for any computed system residue $s[n]$, one may also

1) compute clusters $\{\hat{y}_i\}=\{\hat{y}[n]|\mathbf{w}^{(n}=\mathbf{w}_i\}$,
2) obtain $\eta_i'=\hat{y}_i-x_i$ with $x_i=\mathbf{Q}^{-1}(\mathbf{w}_i)$ –see (3),
3) compute statistics as per digital word.

The resulting curve describes $\mathcal{N}(\cdot)$ in our NL model, after the linear response has been subtracted.

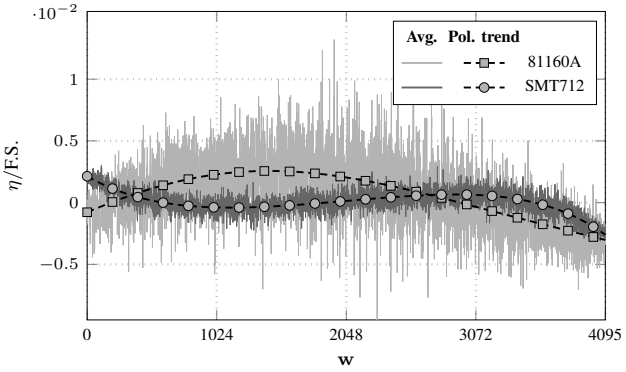

Fig. 5. Codeword NL average distortion and polynomial trends for commercial DACs Agilent's 81160A and Sundance's SMT712.

IV. Experiences

We evaluated two commercial, arbitrary signal generators: Agilent's 81160A and SMT712 from Sundance Multiprocessor Tech. Ltd., encapsulating Maxim's MAX19692 chip. We connected Agilent's DSO90254A Oscilloscope at 20 GSa/s (BW=2.5 GHz) according to the procedure in Section III-C to collect the corresponding outputs to full-scale, within respective operating frequency span's, with $f_1/f_0 \approx 32/5$ at the respective highest generation rates.

In Fig. 4 we include the results of Step 1 for the two generators evaluated: the respective system residues. We computed the standard average across 100 repetitions to mitigate measuring noise effect. By inspecting the curves on the top of the figure one may easily identify individual peaks, located around system-independent, input-dependent timestamps $\{n_r/f_s\}$, marked by triangles.

Peaks individually refer to the contributions of the $\{r = 1, \ldots, Q\}$ orders in the residue. The r-th peak is associated to contributor $\hat{g}_r[n]$ in (20); this is, the memory effect from the r-th order kernel. We include a zoom around each of these for $1 \leq r \leq 5$ on the lower part of Fig. 4. The responses for the different orders shall explain the distortion effect in a DAC component. When addressing the static, purely nonlinear model in [5], these shall reduce to frequency-bounded, delta-like impulses; or ideally, equate zero for a perfectly linear response. In summary, the proposed figure may well be introduced for a variety of nonlinear models that match the overall behaviour of digital-to-analog converters; and may be interpreted in terms of energy distribution: the more energy concentrated on one order, the higher its contribution to the nonlinearity.

According to our results, 81160A displays higher even orders (i.e., larger peaks for even values of r), whereas for SMT712 odd orders dominate. On (17) we related this to the compound effect of Blocks (i) and (ii) in Fig. 2. Furthermore, for this same equation and the response delivered by 81160A, the first order contribution (around $n_r = 0$) mostly related to Block (i) is significantly more relevant (wider) compared to SMT712.

In Fig. 5 we include the results for Step 2. For input sequence $e[n]$, on each unique codeword $\mathbf{w_i}$ governing the switches' array state, we computed the average of η_i'. Here, polynomial trends perfectly match the order-dependent contributions on the system residue, depicted in Fig. 4 —even and odd, respectively for 81160A and SMT712.

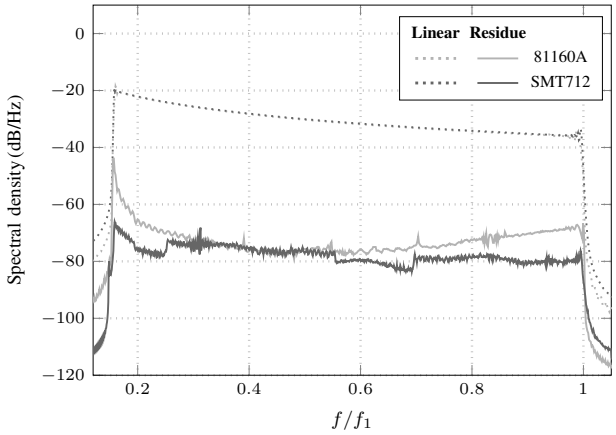

Fig. 6. Spectral density of the normalized linear terms and NL system residues for commercial DACs Agilent's 81160A and Sundance's SMT712.

Moreover, the spurious spikes that one may identify by simple inspection are mainly related to Block i —see (17).

Still, one should bare in mind that in computing the NL system residue (20), the linear response of the DAC was normalized and subtracted. In Fig. 6 we include frequency responses of the purely linear terms ($\rho e[n] * e[-n]$) and the NL system residues' ($s[n]$) for Agilent's and Sundance's components. Differences in power level between the linear term and NL distortion vary along frequency, in ranges ca. $(35, 45)$ dB/Hz and $(45, 55)$ dB/Hz for Agilent's and Sundance's commercial components, respectively.

V. Conclusions

Standard figures of merit in conventional specifications of DACs may be misleading considering the internal structure of a DAC component. Despite the benefits of steady state analysis, actual nonlinear behaviour demands a more complex approach. In this contribution we have reviewed non-ideal effects described in the literature for digital-to-analog converters, formulated an informed nonlinear model and revisited several standard figures attending to the proposed, cascade, nonlinear model for DAC behavior. According to the latter, a novel figure of merit, the system residue $s[n]$, is proposed for calibrated, high-precision DACs. Its computation requires a simple test to be performed on a full-scale, band-limited, exponential sweep.

Contrarily to the THD and IMD, the system nonlinear residue describes the device's full scale response along the full frequency span of the input, and for the different nonlinearity orders, not just harmonics' or intermodulation products' magnitude. Thus, it may well be used while considering complex signals, not just monotones' combinations. Furthermore, it differentiates between nonidealities affecting DACs' performance, separating the memory and nonlinearity static effects from the more dynamic ones; as one would like to have when computing INL and DNL figures.

By simple inspection one may compare performance for different devices. We compared two commercial, arbitrary signal generators, and observed systematic differences that may be decisive in high precision scenarios: (i)

1) deviations due to the input sources,

2) deviations due to a static nonlinearity.

Results for Steps 1 and 2 evidence the relevance of the system residue when describing the overall system behavior, instead of a direct analysis of the system output as it has been traditionally done when computing INL, DNL, THD or IMD products or intensive system identification. The proposed figure separates the contributions of the different blocks in the system in a way that is easy to interpret by simple inspection. DACs' behavior is intrinsically, but not purely, linear; while deviations match those that we derived from the postulated system model.

Future work shall extend the characterization of gates' time evolution in conjunction with the proposed model. This shall provide further insights on DACs behavior, considering the dynamic evolution of these nonlinear systems. Moreover, the proposed figure of merit ought to be tested for the characterization of other components that have a desired response and match a similar nonlinear model. Specifically, one may like to address amplifiers, mixers or systems involving processes such as modulation and demodulation; all having well-defined, ideal responses.

REFERENCES

[1] Y. Cong and R.L. Geiger, *Switching sequence optimization for gradient error compensation in thermometer-decoded DAC arrays*, *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, 2000, **7**, pp. 585-595.

[2] R.J. van de Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, *Springer Ser. Eng. Comp. Sci.*, 2003, **742**, pp. 51-105.

[3] T.B. Williams, *The calibration of a DAC using differential linearity measurements*, *IEEE Trans. Instrum. Meas.*, 1982, **31**(4), pp. 261-265.

[4] P.S. Wright and J.R. Pickering,*An AC voltage standard based on a PWM DAC*, *IEEE Trans. Instrum. Meas.*, 1999, **48**(2), pp. 475-461.

[5] B. Vargha and J. Schoukens and Y. Rolain, *Static nonlinearity testing of digital-to-analog converters*, *IEEE Trans. Instrum. Meas.*, 1999, **50**(5), pp. 1283-1288.

[6] B. Vargha and I. Zoltan, *Calibration algorithm for current-output R-2R ladders*, *IEEE Trans. Instrum. Meas.*, 2001, **50**(5), pp. 1216-1220.

[7] L. Angrisani and M. D'Apuzzo and M. D'Arco, *Fast Transformation for DAC Parameters Identification*, *IEEE Trans. Instrum. Meas.*, 2006, **55**(6), pp. 2007-2013.

[8] L. Jin and H. Haggag and R.L. Geiger and D. Chen, *Testing of Precision DAC Using Low-Resolution ADC With Wobbling*, *IEEE Trans. Instrum. Meas.*, 2008, **57**(5), pp. 940-946.

[9] Y. Yang and L. Huang and Z. Lu and W. Lu, *AC Voltage Reference Using the Fundamental of DAC Stepwise-Approximated Sine Waves*, *IEEE Trans. Instrum. Meas.*, 2014, **63**(2), pp. 473-478.

[10] L. Wang and Y. Fukatsu and K. Watanabe, *Characterization of current-mode CMOS R-2R ladder digital-to-analog converters*, *IEEE Trans. Instrum. Meas.*, 2001, **50**(6), pp. 1781-1786.

[11] M. D'Arco and A. Liccardo and N. Pasquino, *ANOVA-Based Approach for DAC Diagnostics*, *IEEE Trans. Instrum. Meas.*, 2012, **61**(7), pp. 1874-1882.

[12] M. D'Apuzzo and M. D'Arco and A. Liccardo and M. Vadursi, *Modeling DAC Output Waveforms*, *IEEE Trans. Instrum. Meas.*, 2010, **59**(11), pp. 2854-2862.

[13] M. Kampik, *Analysis of the Effect of DAC Resolution on AC Voltage Generated by Digitally Synthesized Source*, *IEEE Trans. Instrum. Meas.*, 2014, **63**(5), pp. 1235-1243.

[14] A. Novák and L. Simon and F. Kadlec and P. Lotton, *Nonlinear System Identification Using Exponential Swept-Sine Signal*, *IEEE Trans. Instrum. Meas.*, 2010, **8**, pp. 2220-2229.

[15] R.J. Baker, *CMOS: Circuit Design, Layout, and Simulation*, *Wiley*, IEEE Press Series on Microelectronic Systems, 2011.

[16] M. Gustavsson and J.J. Wikner and N. Tan, *CMOS Data Converters for Communications*, *Springer US*, The Springer International Series in Engineering and Computer Science, 2000.

[17] M. Schetzen, *Nonlinear system modeling based on the Wiener theory*, *Proc. of the IEEE*, 1981, **69**(12), pp. 1557-1573.

[18] J.J. Wikner and N. Tan, *Modeling of CMOS Digital-to-Analog Converters for Telecommunication*, *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, 1999, **46**, pp. 489-499.

[19] E. Balestrieri, *DAC Time-Domain Specifications Toward Standardization*, *IEEE Trans. Instrum. Meas.*, 2008, **57**(7), pp. 1290-1297.

[20] L. Angrisani and M. D'Arco, *Modeling Timing Jitter Effects in Digital-to-Analog Converters*, *IEEE Trans. Instrum. Meas.*, 2009, **58**(2), pp. 330-336.

[21] F. Attivissimo and N. Giaquinto and I. Kale, *INL reconstruction of A/D converters via parametric spectral estimation*, *Proc. 20th IEEE Instrum. Tech. Conf.*, 2003, **2**, pp. 1166-1170.