Direct E-field Measurement and Imaging of Oscillations within Power Amplifiers

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***Abstract*—We present for the first time a measurement system that is capable of directly detecting and identifying the physical location of an oscillation within RF and microwave power amplifiers. The method uses a combined external electro-optic, non-linear vector network analyzer, and vector load-pull measurement system, which allows the measurement of cross-frequency phase-coherent multi-harmonic vector electric fields above the transistor with an 8 µm spatial resolution and 20 MHz – 40 GHz bandwidth. Raster scans above the amplifier allow the time-domain electric fields to be animated and superimposed on top of the amplifier image enabling immediate identification of any oscillations by direct inspection. The method is first demonstrated on a low power amplifier composed of two parallel 0.1-W pHEMT transistors that is intentionally designed to have an odd-mode oscillation. The applicability of the method is further demonstrated by measuring and animating in-package parametric odd-mode oscillations within a 260-W laterally diffused metal-oxide-semiconductor (LDMOS) transistor operating at 2.2 GHz under pulsed RF conditions with 10 µs pulses and 10% duty cycle. The measurement and identification technique is applicable to all semiconductor devices as the external electric field is non-invasively measured above the amplifier.**

***Index Terms*—Bifurcation detection, device characterization, electro-optic sampling, laterally diffused metal-oxide-semiconductor (LDMOS) transistor, near-field measurement, oscillation, stability**

I. Introduction

PACKAGED radio frequency (RF) and microwave transistors achieve high output powers through the parallel connection of many individual transistors within a single die. Further increases in output powers are achieved through the parallel assembly of many dies within a transistor package as shown in Fig. 1, where a 260-W, 2.1–2.2 GHz packaged laterally diffused metal-oxide-semiconductor (LDMOS) power transistor is shown with its ceramic lid removed revealing the semiconductor dies and the internal matching networks. The matching networks are composed of arrays of parallel bonding wires, metal-oxide-semiconductor (MOS) capacitors, and the package, and are designed to increase the input and output impedances of the parallel transistor assembly so that matching can be readily performed on printed circuit boards (PCB). While the specific matching network is shown for a packaged LDMOS transistor, similar assembly, packaging, and matching network configurations are used for gallium nitride (GaN) and gallium arsenide (GaAs) packaged transistors. One of the main drawbacks of these highly parallelized networks, referred to as cluster matching, is that their construction forms many closed loops within the package and these matching topologies have been shown to suffer from detrimental loop oscillations [1], [2].

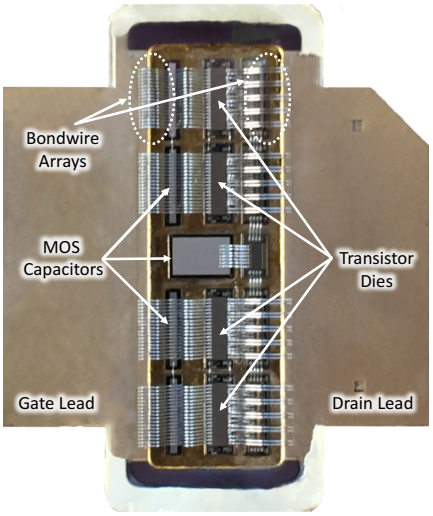

Fig. 1. A 260-W packaged LDMOS transistor with its protective ceramic lid removed. The transistor circuitry is comprised of 4 transistor dies connected in parallel that are individually input and output matched using bondwire arrays and MOS capacitors.

The stability analysis of transistors has long been studied as power amplifiers (PAs) often exhibit instabilities in the form of spurious oscillations at incommensurate or sub-harmonic frequencies [3]–[5]. Parametric oscillations are a function of the input power, frequency, and other circuit or biasing parameters, and are only observable at a certain gain compression point [5]–[7]. This is of particular importance for power amplifiers that are driven by modulated signals with high peak-to-average power ratios, as the peak of the signal often enters the gain compression region. Moreover, if digital pre-distortion is used, it will fail to compensate for the sudden gain compression or expansion if the parametric oscillation is induced in the device. Due to the non-linear nature of the problem, traditional linear stability analysis methods employing μ- and k-factors are invalid [8]–[10]. Time-domain simulations are often impractical due to the majority of components defined in frequency domain, so harmonic balance (HB) simulators are frequently used. During circuit design, a detailed large-signal stability analysis and bifurcation detection on HB is

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required due to its potential converge to an often coexisting unstable solution. Typically the analysis employs either a pole-zero technique, or a switching-parameter algorithm with an auxiliary generator yielding an admittance function Y_{AG}, which is calculated using the conversion-matrix approach [4], [10]–[12]. By setting Y_{AG} = 0, bifurcation loci are obtained. This is sufficient to determine the parameter-dependent stability limits of the amplifier, however, to identify the mode of the oscillation further analysis is needed.

Power amplifier circuits can oscillate in even- and odd-modes. During even-mode oscillations signals are flowing in and out of the circuit ports under consideration, while during odd-mode oscillations, characterized by a 180° phase difference between signals in parallel devices, internal current loops are generated that do not leave the circuit, thus port-based analysis techniques are not suited for odd-mode oscillation detection [13], [14]. To overcome this, various analysis methods have been proposed. Devices exhibiting layout symmetry are frequently analysed using the eigenvalue analysis [14] and by splitting the circuit and enforcing a ground connection at the power combining port [15]. More general approaches that are not constrained to symmetrical circuits are the normalized determinant function (NDF) [16], [17] and Ohtomo test [18], [19]. The main limitation of the aforementioned odd-mode stability analysis techniques is their inapplicability to devices operating in the non-linear regime, with the fundamental limitation arising from the derivation of the linear stability analysis techniques, which is based on the linearisation of the device around its DC operating point. This, however, is only defined for small perturbations around the linearisation point, which precludes the large signal drive conditions [20]. Thus, they cannot be used to detect the parametric odd-mode oscillations, which are typically found through a pole-zero analysis [21].

A very common and thoroughly studied case of parametric odd-mode oscillations is at sub-harmonic divide-by-two ($f_0/2$) frequencies [6], [12], [20], [22], but odd-mode oscillations at the fundamental operating frequency (f_0) have also been reported [23]. They are observed as a sharp decrease in the output power, P_{out}, with respect to the input power, P_{in}, on a drive-up curve, and a sudden gain expansion or compression in the gain curve.

One of the main problems associated with the large-signal non-linear stability analysis is its reliance on very accurate device models. This poses a problem if the device is still a prototype and the device models are yet to be generated. In this case there is no quick and convenient way of analysing the device stability and directly identifying the origin of oscillations. In a circuit with *N* active devices connected in parallel there might be *N-1* independent odd-mode oscillations [12], thus tests that are capable of visualizing oscillations *in situ* are needed to identify the origin of closed loops.

Until now, the AM/AM drive-ups obtained through load-pull measurements and the power spectrum analysis were the only measurement-based techniques to identify parametric oscillations within microwave power transistors. However, they provided no information about the location of the oscillations, particularly the closed loops between multiple devices in the case of a parametric odd-mode oscillation. In this paper, a new electro-optic (EO) E-field measurement-based technique for the direct detection, localization, and imaging of these types of oscillations is presented. We demonstrate how to visualize parametric odd-mode oscillations enabling the load-impedance dependence characterization of odd-mode instabilities and detection of their origin at fundamental and harmonic frequencies. The proposed method is demonstrated on a PA operating as a free-running oscillator and the 260-W LDMOS power transistor shown in Fig. 1. Section II of the paper describes the devices used during the measurement and the measurement set-up. Section III presents both port-based and distributed E-field measurement results, and Section IV concludes the the paper.

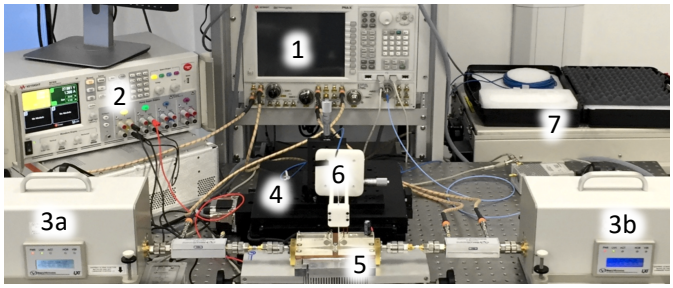


Fig. 2. Measurement set-up used to detect unstable oscillations within power amplifiers, combining a PNA-X working in an NVNA mode (1), a DC power supply (2), source (3a) and load (3b) impedance tuners, a 2-D translation stage (4), a DUT in a load-pull test fixture (5), all dielectric EO probe holder (6) and a NeoScan optical mainframe (7).

II. Measurement Set-up and Test-Amplifiers

Electro-optic measurements have long been used to interrogate vector E-fields above the device under test (DUT) [24]–[26]. In this paper, the measurement setup to detect and understand the physical origins of oscillations uses a commercially available NeoScan™ electro-optic (EO) measurement system from EMAG Technologies Inc., which employs external $Bi_{12}SiO_{20}$ (BSO) probes to measure vector electric-field (E-field) with amplitudes of 1 V/m – 2 MV/m, and 20 MHz – 40 GHz bandwidth [27]. To enable multi-harmonic phase-coherent electric field measurements the system is connected to a Keysight Technologies N5247A PNA-X 67 GHz non-linear vector network analyzer (NVNA) that uses a comb generator as a phase reference [28], [29]. Two Maury MT982BL01 impedance tuners are used to present various source and load impedances to the DUT [30], [31]. The measurement set-up, as shown in Fig. 2, is controlled by custom measurement software implemented using National Instruments™ LabVIEW.

The measured phase-coherent multi-harmonic E-fields can be used to reconstruct time-domain E-fields above the DUT or extract waveforms at different locations above the circuit. This is achieved through a pixel-by-pixel time-domain summation of all harmonics of the distributed E-fields measured above the DUT [27]. As the E-field and light polarization change relationship inside the EO crystal is scalar and linear, the relative distributed E-field measurement results presented in this paper are normalized to their own maximum. Thus the E-field measurement plots are within the normalised range of -1

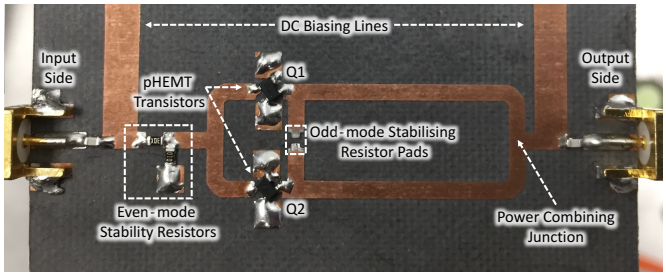


Fig. 3. Image of the low-power PA, highlighting the key components and the power combining junction where a virtual ground is formed during an odd-mode oscillation.

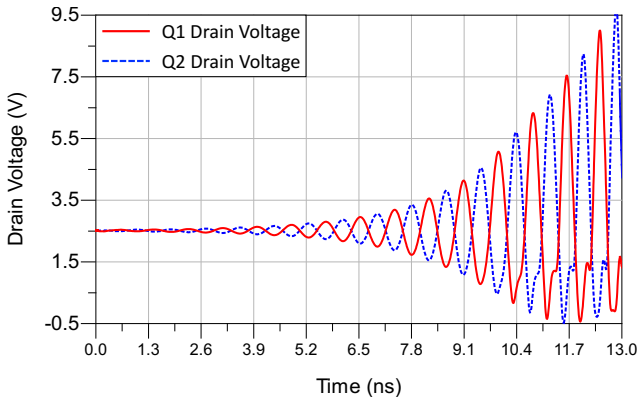


Fig. 4. Simulated odd-mode voltage at the Q1 and Q2 drain terminals of the low-power GaAs pHEMT PA shown in Fig. 3. The odd-mode behavior is characterized by a 180° phase difference between the two drain voltages.

to 1 and indicate the peak positive amplitude of the measured E-field with a dark red, and the peak negative amplitude with dark blue colors in the picture overlays.

A. Low-Power GaAs pHEMT PA

To demonstrate the potential of the new measurement technique, a power amplifier exhibiting odd-mode oscillations was designed. The power amplifier design was based on [32] and was fabricated using a 20-mil thick Rogers RT5880 substrate with two parallel Avago Technologies ATF-54143 pseudomorphic high electron mobility transistors (pHEMTs) connected in parallel by two symmetrical gate and drain feeds. A photograph of the circuit is shown in Fig. 3 with included pads for an odd-mode oscillation suppression resistor.

To check if odd-mode oscillations could be excited within the PA, a model of the amplifier was developed in ADS and an external current impulse source acting as a perturbation signal was connected to the drain terminal of one of the pHEMT transistors [14]. In the case of a stable power amplifier, the resulting perturbation is dampened until it decays. In the case of the amplifier being unstable, the odd-mode oscillation is exited, a closed current loop is formed, and the oscillation builds up. This indeed is the case if the inter-drain stabilizing resistor is not connected between the two pads as shown in Fig. 3. The simulated build-up of the odd-mode voltage on the two drain outputs is shown in Fig. 4, where it can be seen that the voltage at the drain lead of each GaAs transistor has a 180° phase difference. The instability is further confirmed by

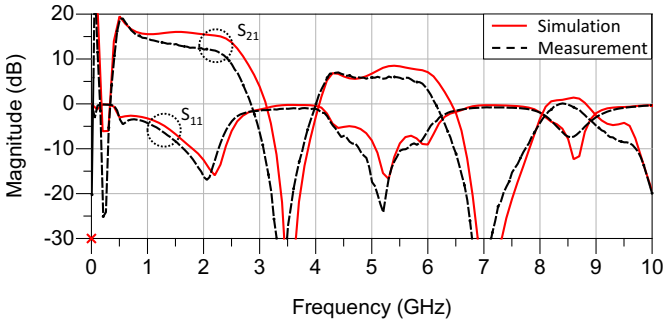


Fig. 5. Simulated and measured S-parameters of a low-power GaAs pHEMT PA showing a good agreement of the results. The slight mismatches are attributed to the transistor model and no co-simulation with layout components.

eigenvalue analysis and simulating the reflection coefficient of each amplifier branch separately with a ground placed at the power combining junction. This is done to emulate a virtual ground created by the odd-mode oscillation.

To ensure stable device operation, a 180-Ω stabilizing resistor was placed between the two drain feed branches suppressing potential odd-mode oscillations. In this configuration the circuit was biased at V_d = 3 V and V_g = 0.62 V resulting in a stable device operation. Comparison between measured and simulated S-parameters of the stable PA is shown in Fig. 5 indicating a good agreement of the results.

Before measuring E-fields of the PA, the odd-mode stabilizing resistor was removed. This resulted in the PA operating as a free-running oscillator with the autonomous fundamental frequency of 1.4 GHz. The circuit was terminated using a 50-Ω load. During the E-field measurements, the system has been configured to measure normal E-field component (perpendicular to the surface of the PA circuit) with 4 harmonics of a 1.4 GHz fundamental.

B. Packaged High-Power LDMOS Transistor

The 260-W large-periphery LDMOS transistor, as shown in Fig. 1, has 4 transistor dies connected in parallel and exhibits a layout symmetry, making it prone to parametric odd-mode oscillations. The transistor is packaged in an air-ceramic cavity package and the protective lid was removed for the E-field measurements. The transistor was measured inside a load-pull test-fixture with a tapered impedance transformer [27]. The maximum measured output power at the 3-dB gain compression point (P_{3dB}) was 54.6 dBm at 2.11 GHz. The measurement reference planes were at the ends of 3.5 mm connectors of the load-pull test-fixture. A short-open-load-through (SOLT) calibration was performed at the connector ends. The transistor was biased at V_{ds} = 28 V, I_{ds}= 1.46 A, V_{gs} = 2.55 V.

In order to obtain load-pull contours and drive-up curves that reveal the parametric odd-mode instabilities, pulsed NVNA load-pull (PLP) measurements were first performed on a large periphery 4-die 260-W LDMOS transistor. The NVNA was configured to measure 3 harmonics of a 2.11, 2.14, 2.17 and 2.2 GHz fundamental with 10 µs RF signal pulse width and 10% duty cycle. The noise bandwidth of the NVNA during the measurement was set to 500 Hz, the

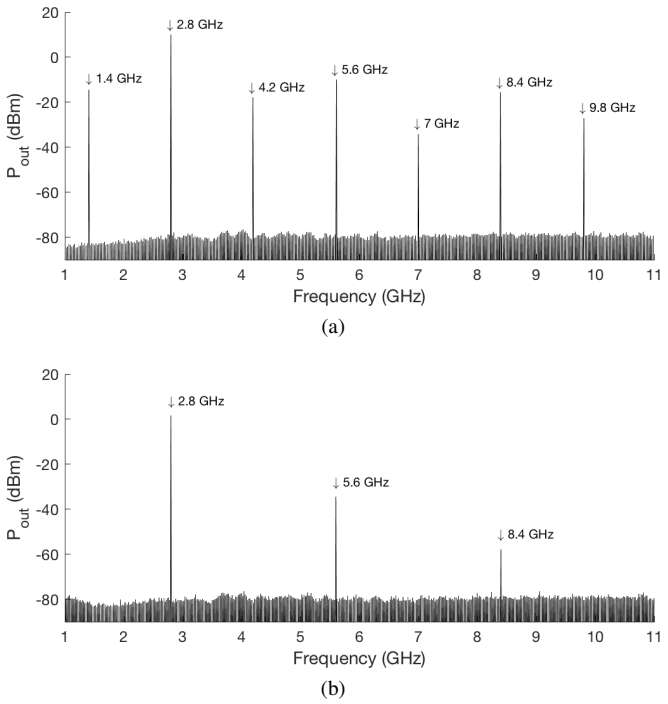


Fig. 6. Measured spectrum of the low-power GaAs pHEMT PA operating as a free-running oscillator (a), and a stabilised PA spectrum with an externally injected 2.8 GHz 0 dBm signal (b). The 1.4 GHz odd-mode signal in Fig. 6(a) is significantly smaller than the 2.8 GHz even-mode signal, due to the cancellation of the waves and the virtual ground being formed at the drain combining junction.

IF bandwidth used during the calibration was 10 Hz, and measurement averaging was set to 5.

III. Results

A. Low-Power GaAs pHEMT PA Measurements

The PA was biased as indicated in Section II. Due to the unstable operation of the PA, each drain-side power combining branch exhibits a 180° phase difference at 1.4 GHz, which produces a very strong 2.8 GHz even-mode mixing product on the output, as shown in the measured spectrum of the PA in Fig. 6(a), where the 2.8 GHz even-mode signal is 20 dB higher than the 1.4 GHz odd-mode signal. As expected, this is due to the partial cancellation of the waves at the power combining junction that forms a virtual ground inside the circuit. In an ideal linear circuit the odd-mode signals would cancel out entirely, resulting in no spectral component at 1.4 GHz. This is the reason why external port-based stability analysis methods have difficulties in predicting odd-mode oscillations.

If the transistor is stabilized by including an inter-drain resistor, the autonomous oscillation at 1.4 GHz and its corresponding harmonics disappear, and no output signal is observed. For comparison Fig. 6(b) shows the spectral output of the stabilised PA, when a 2.8 GHz 0 dBm external signal is injected into the PA. The output spectrum shows only the signal at the frequency of interest (2.8 GHz) and its second and third harmonic. To measure the E-fields of the unstable power amplifier, the stabilising resistor was removed from the circuit, which resulted in the PA operating as a free-running oscillator with an autonomous frequency of 1.4 GHz.

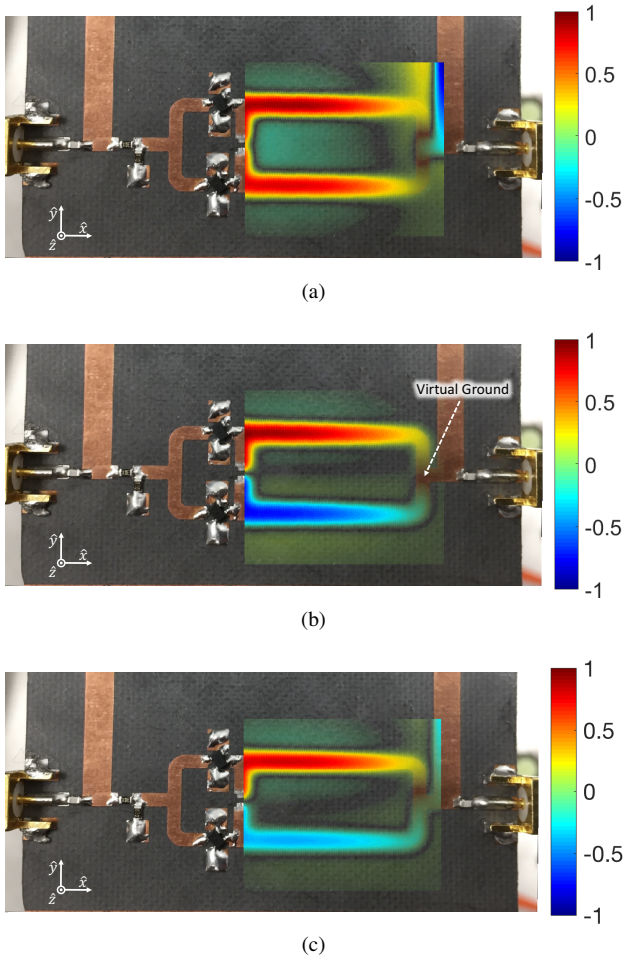


Fig. 7. Measurement overlay of a 2.8 GHz even-mode (a), 1.4 GHz odd-mode (b), and time-domain (c), reconstructed using 4 harmonics, oscillations on the low-power GaAs pHEMT PA image. The 180° phase difference on the two amplifier drain microstrips forms a virtual ground at the drain power combining junction as shown in (b). The peak positive and negative amplitudes of the normalised measured E-field are represented by the dark red, and dark blue colors respectively. Animations are provided for all configurations showing the time varying fields in movies Fig_6a-c.mov.

The output of the PA was scanned at four harmonics between 1.4 GHz and 5.6 GHz, with the scan area of 23 x 20 mm, and a 100 µm step size on both x and y axes. The EO probe was positioned 300 µm above the printed circuit board (PCB) of the PA. The normal E-field vector component (E_z) was measured. The total scan time was 6 hours during which the measurement stability was ensured by monitoring the total and received laser beam powers in the optical mainframe of the EO system. Thermal stability of the polarizers was ensured by an integrated thermoelectric circuit (TEC).

The normalized E_z field measurement results are shown in Fig. 7, where they are superimposed on a photograph of the PA. Measurement results agree well with theory and show the device operating in even-mode at 2.8 GHz, as shown in Fig. 7(a), and in odd-mode at 1.4 GHz, as shown in Fig. 7(b). The virtual ground is seen at the drain-side power combining junction leading to minimum power being delivered to the load. The measurement results reveal that every odd harmonic of the 1.4 GHz signal results in an odd-mode device behavior.

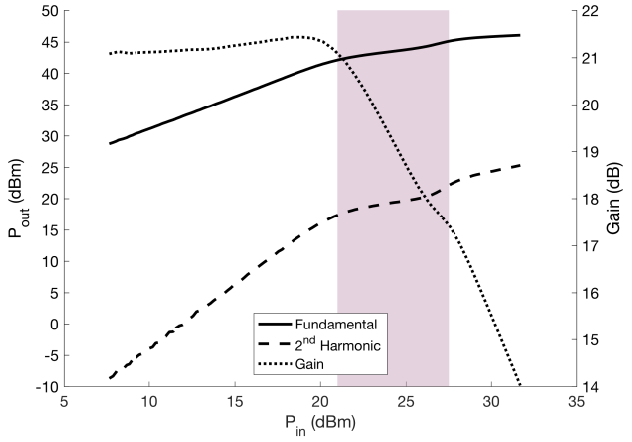


Fig. 8. The P_{out} and gain curves vs. P_{in} of an LDMOS transistor at a load where parametric odd-mode oscillation is observed. The shaded area indicates the region with a parametric oscillation.

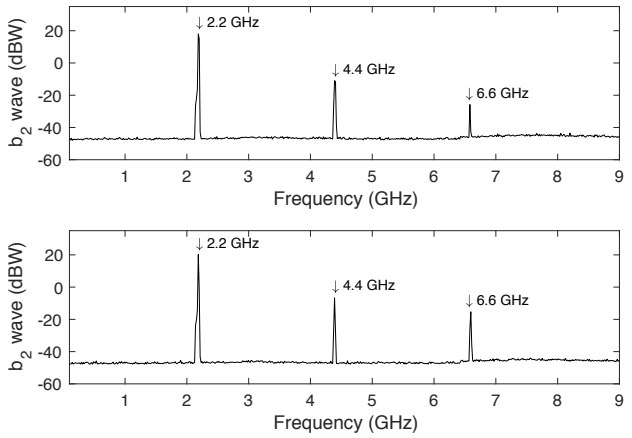


Fig. 9. Spectrum of a 260-W LDMOS transistor at a load where parametric odd-mode oscillation is observed operating at 2.2 GHz fundamental with P_{in} = 25.1 dBm, showing no sub-harmonic oscillation (top), and at P_{6dB} gain compression point outside of the drive-up curve region with parametric oscillations (bottom).

The E-field plot in Fig. 7(c) shows, for the first time, a reconstructed time-domain odd-mode electric field with all 4 measured harmonics (1.4 GHz – 5.6 GHz). In the case of the stable PA operation with a 2.8 GHz injected signal, the E-field distribution would be exactly the same as the one shown in Fig. 7(a) as the device, in both cases, is working in even-mode. Measurements on this amplifier demonstrate the measurement system's ability to detect and animate odd-mode oscillations and its applicability to measure parametric instabilities.

B. Packaged High-Power LDMOS Transistor Measurements

The measured drive-up curves at some impedance points at a 2.2 GHz fundamental had a decrease in the P_{in} vs. P_{out} curve, which is a characteristic of a parametric oscillation, occurring only at a certain gain compression point [5]. For example at Γ_{load} = 0.85, -38° the transistor exhibits a decrease in the P_{out} at both fundamental and 2nd harmonics, as shown in Fig. 8. A change in the slope of the gain can also be seen, further denoting the presence of a parametric oscillation. No spurious spectral lines are observed in the measured spectrum

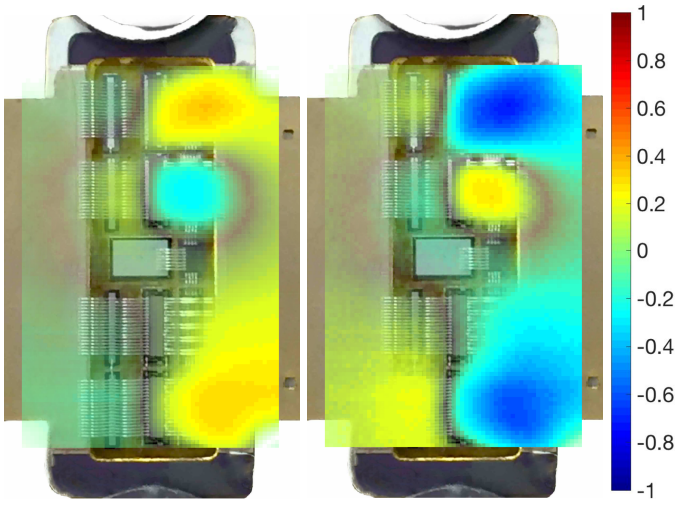


Fig. 10. Normalized E_z-field measurement overlaid on a 4-die LDMOS transistor picture highlighting the locations of closed loops and dies oscillating in odd-mode. The measurement results are shown for a 2.2 GHz fundamental (a) and 2nd harmonic (b) with Γ_{load} = 0.85, -38°. In both (a) and (b) only the top pair of transistor dies are oscillating in odd-mode resulting in an asymmetrical device operation. The peak positive and negative amplitudes of the normalised measured E-field are represented by the dark red, and dark blue colors respectively. Animated versions are available by opening movies Fig_9a-b.mov.

of the b_2 power wave emitted from the output of the amplifier as shown in Fig. 9, suggesting that the closed loops formed at both fundamental, and 2nd harmonics support odd-mode oscillations that lead to direct cancellation of waves inside the transistor. The odd-mode oscillation at the 2nd harmonic, in this transistor, is the cause for an odd-mode oscillation in the fundamental. The odd-mode oscillation generated at the 2nd harmonic couples back to the input, and mixes with an even-mode fundamental signal on the gate. The resulting mixing products are an odd-mode oscillation at the fundamental frequency, 2nd harmonic and the 3rd harmonic as confirmed by the measurements. This demonstrates the importance of performing harmonic PLP measurements, as the bifurcation might occur outside of the transistor operating frequency band, but still have an impact on the device behavior at the fundamental frequencies.

After the load-pull measurements were obtained and load impedance points at which the device exhibits parametric oscillations were identified, the E-field measurement system was configured to measure the normal E-field component, E_z, perpendicular to the LDMOS transistor surface. During the E-field measurement of the LDMOS transistor the source impedance tuner was set to the complex conjugate of the DUT input impedance to maximise the input power. The load impedance was varied to present specific impedance points where the oscillation is present. The E-field measurements were performed using the NVNA mode of the PNA-X, which preserved the cross-frequency phase coherence of the measured signals and their harmonics [27].

During the E_z field measurements, the external EO probe was positioned 300 µm above the tallest bondwires of the packaged transistor. The measurement area was 18 x 12 mm,

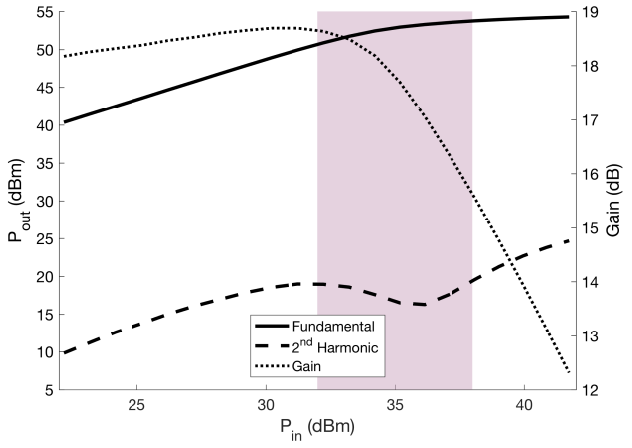
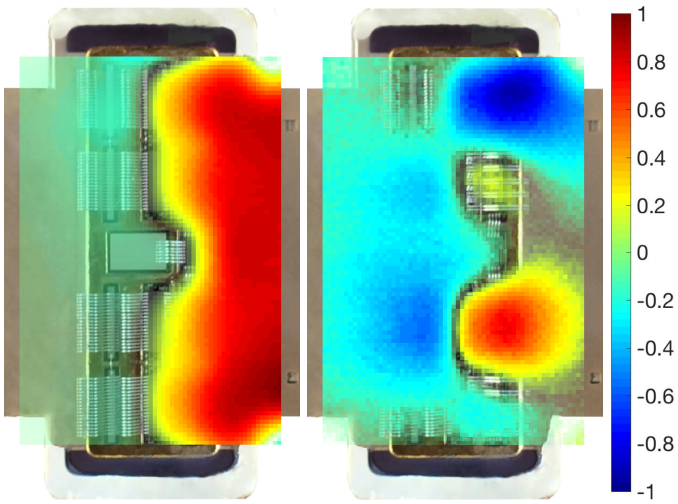


Fig. 11. The drive-up curves of a 260-W LDMOS transistor at Γ_{load} = 0.7, 10.5° operating at 2.2 GHz. The drop in the output power of the 2nd harmonic (bottom) indicates an parametric oscillation, which has no effect on device operation at the fundamental frequency (top). The shaded area in the bottom curve indicates the region with a parametric odd-mode oscillation which can be observed in both fundamental, and the 2nd harmonic.



(a) (b)

Fig. 12. Normalized E_z-field measurement overlaid on a 4-die LDMOS transistor picture with odd-mode suppressing drain wires operating at 2.2 GHz fundamental (a) and 2nd harmonic (b) with the load reflection coefficient set to Γ_{load} = 0.7, 10.5°. In (b) both pairs of the transistor dies are oscillating in odd-mode forming two closed loops. The peak positive and negative amplitudes of the normalised measured E-field are represented by the dark red, and dark blue colors respectively. Animated versions are available by opening movies Fig_11a-b.mov.

with the translation stage step size set to 200 µm on both *x* and *y* axes. The duration of the scan was 4 hours to measure 3 harmonics of a 2.2 GHz fundamental signal. The transistor was biased as indicated in Section II and the input power was 25.1 dBm with the load reflection coefficient set to Γ_{load} = 0.85, -38°.

The normalized E-field measurement results shown in Fig. 10 reveal the bottom two dies operating in even-mode and the top two dies operating in odd-mode at both fundamental (Fig. 10(a)) and 2nd harmonic (Fig. 10(b)). This is seen by the out-of-phase normalized E_z-field values on top of the output matching networks. As the magnitude and phase of the measured E-field is measured at multiple harmonics for each pixel, Fourier series are computed and show the time-dependent E-field above the devices [27]. These surfaces are animated and provided with this paper. They reveal complex and dynamic device behavior of the oscillation and provide significantly more insight than the static images.

C. Oscillation Suppression

A common technique to suppress odd-mode oscillations is to introduce a resistor between the drain/gate leads of the two transistors, as was used to stabilise the low-power GaAs pHEMT PA in Section II-A. A resistor will be able to stabilise the circuit only if there are no quasi-cancellations of the unstable right hand plane (RHP) poles by the RHP zeros in the circuit transfer function [33]. The use of resistors can also increase the losses in the circuit by conducting the current in even-mode if the voltage distribution across the transistor is non-uniform.

To dampen the oscillations either on the gate or the drain side, a reactive element, such as a capacitor or a bondwire, can also be used if the impedance of the element is carefully selected. By changing the length and the loop height of the bondwire interconnecting the drains of the 4 transistor dies, an impedance presented at different frequencies by these inter-drain bondwires can be changed. Additionally, a capacitor connected in series to the bondwire forms a frequency-dependent resonant circuit. By connecting this LC circuit to the damping resistor, an effective frequency selective oscillation suppression RLC circuit is formed. This fix was implemented to the LDMOS transistor presented in the previous section.

To evaluate the effectiveness of the oscillation suppression technique, the LDMOS transistor with the RLC circuits between transistor dies was measured. The drive-up curves at 208 load impedance points had no indication of bifurcations at the fundamental frequencies, however, some of the drive-up curves with a 2.2 GHz fundamental had a decrease in P_{out} at the 2nd harmonic. One of such points is Γ_{load} = 0.7, 10.5°, which has its drive-up curves plotted in Fig. 11. The output frequency spectrum showed no spurious spectral components. As the inter-drain RLC circuits are able to effectively dampen out the odd-mode oscillations at the drain of the transistor, the oscillations at the 2.2 GHz fundamental frequency are successfully prevented.

The EO measurement system settings used were the same as noted in Section III-B. The load reflection coefficient presented to the transistor was set to Γ_{load} = 0.7, 10.5° and the input power was set to 36 dBm. The normalized E-field measurement results showing relative E_z field component distribution above the DUT are shown in Fig. 12. From the drive-up curves at Γ_{load} = 0.7, 10.5°, as shown in Fig. 11, it is seen that the device is operating in an even-mode at the fundamental frequency and in odd-mode at the 2nd harmonic. This is confirmed by the measured E-field shown in Fig. 12, where both pairs, top and bottom, of the transistor dies exhibit odd-mode oscillations.

While the measurement time needed to scan the entire

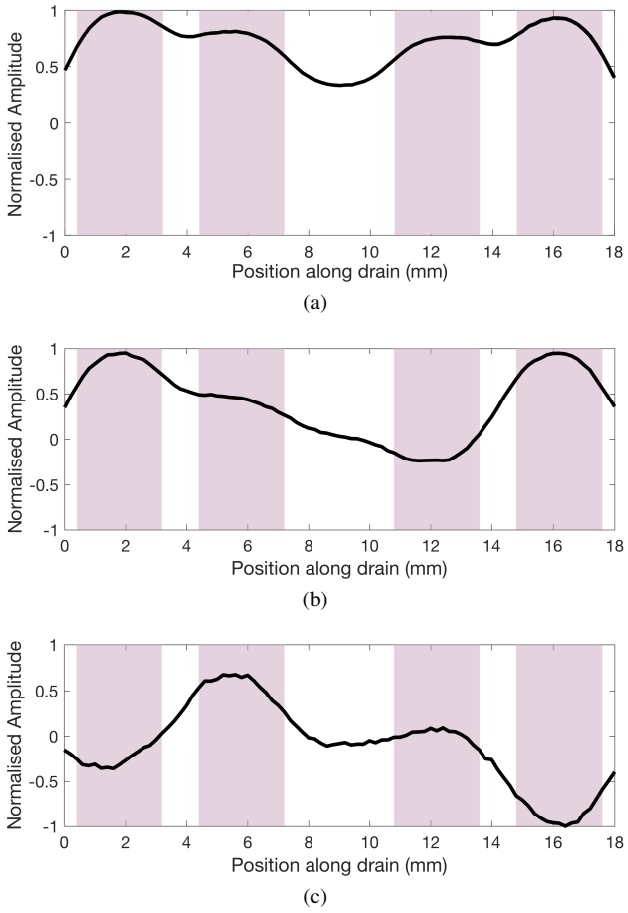


Fig. 13. Normalized E_z field cut-lines over the LDMOS transistor drain bondwire arrays showing the even-mode oscillation at 2.2 GHz (a) and the odd-mode oscillation at the 2nd harmonic (c) of the transistor with the inter-drain bondwires. In (b) an odd-mode oscillation at 2.2 GHz fundamental of the transistor without the the inter-drain bondwires can be seen with top two dies oscillating out of phase. Animated versions are available by opening movies Fig_12a-c.mov.

packaged transistor can be quite long, the measurement of a single cut-line across the packaged transistor drain bondwire arrays with a 200 µm spatial resolution, as shown in Fig. 13, only takes 4 minutes and reveals the 180° phase difference between the transistor dies oscillating in odd-mode. The cut-line measurements enable a fast and efficient way to identify the oscillating dies and can be a valuable aid in the design and optimization of microwave power amplifiers.

IV. Conclusion

A new E-field measurement-based oscillation identification and imaging method within power amplifiers is described. The effectiveness of the method was demonstrated by measuring, for the first time, odd-mode E-field oscillations in an unstable low-power PA behaving as a free-running oscillator, and by further extending it to the measurements of the parametric odd-mode oscillations in a 260-W packaged LDMOS transistor operating under pulsed conditions. The proposed method can be applied to measure any kind of instabilities in multi-die microwave transistors and other complex circuits, allowing an in-depth analysis and imaging of the closed loops, undesired coupling, odd- and even-mode device behavior etc. at fundamental and harmonic frequencies, and under pulsed or CW excitation. All of the E-field measurement results presented in this paper are animated to showcase a time-domain behavior of the measured devices and are provided as additional multimedia files.

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