Ultra-Low-Power Synchronous Demodulation for Low-Level Sensor Signal Detection

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***Abstract*—The design and experimental characterization of a high-resolution analog lock-in amplifier (LIA)-based measurement system is presented in this paper. Different design strategies are used to attain a versatile solution which features programmable gain (72.6 – 82.6 dB) and operating frequency (5 – 115 kHz), preserving good recovery performance. The prototype, integrated in the UMC 0.18 µm CMOS process with a single supply voltage of 1.8 V, achieves a resolution of 200 nV and a high dynamic reserve of 43.5 dB, showing significantly lower power consumption (885 µW) than high-resolution state-of-the-art LIAs with minimum size (0.075 mm² silicon area). To validate the amplitude recovery performance of the proposed single-phase LIA, it was used to measure the equivalent value of a passive resistive sensor, exhibiting a maximum error of 1.9 % when R_S is varied from 100 Ω to 10 kΩ with an input signal in the order of hundreds of microvolts. Thus, it constitutes a highly suitable choice for portable and lab-on-a-chip sensing applications.**

***Index Terms*—Analog processing circuits, CMOS, lock-in amplifiers, low-voltage low-power, synchronous detection.**

I. Introduction

THE increasing interest in portable and wearable sensing devices demanded by innovative medical, scientific, industrial and environmental applications [1-6] requires from designers to develop novel integrated circuit solutions that fulfill key criteria in low-voltage energy-constrained scenarios. One critical problem encountered in battery-compatible integrated sensors is their low output signal level, which may even be outdone by noisy environments. As a result, the use of special amplification techniques addressed to increasing the signal to noise ratio (SNR) are becoming an essential part of the analog front-end electronic interface to reliably extract the signal information.

An interesting alternative with the capability to fulfill the conditions of low-cost portable systems is the use of lock-in amplifiers (LIAs), that operates under the principle of a technique known as phase sensitive detection (PSD) to recover the amplitude and phase of very low-level signals at a reference frequency f_0 even in noisy environments [7, 8]. A phase sensitive detector (mixer) carries out the multiplication between the sensor signal $s(t)=V_{in}\ sin\ (2\pi f_0 t)$ and the reference signal $r(t)= V_{ref}\ sin\ (2\pi f_0 t + \theta)$, where V_{in} is the input amplitude to be recovered, f_0 is the operating frequency, and θ is the phase shift between the input and the reference signal. The multiplication of both signals results in a DC level, which contains information of V_{in} and θ, and a harmonic component at twice the operating frequency, which is filtered by a LPF. If a square signal is used as reference instead, additional harmonic components result from the multiplication, but they are filtered and only a DC level is retrieved at the output, which again contains information of V_{in} and θ. In particular, the output dc level when using a square reference signal is given by [8]:

$$V_{out\_DC} = \frac{2V_{in}V_{ref}}{\pi}\cos\theta \qquad (1)$$

The output DC level is therefore directly proportional to the input amplitude, and for $\theta = 0$, i.e. for in-phase condition, the maximum output DC level at a given V_{in} is obtained. This principle of operation is also suitable to detect the signal information from the new generation of CMOS integrated impedance or resonant sensors [9-13], when quadrature synchronous demodulation is combined with in-phase demodulation (i.e., when dual phase synchronous detection is used).

For the implementation of the PSD operation, digital LIAs offer more flexibility, robustness and higher dynamic reserve, but their complexity is too high for them to be used in low-cost sensor applications [13-20]. In contrast, an analog implementation, with proper design techniques, can result in a simpler design with low voltage and low power consumption, as well as high dynamic reserve can be reach when input filtering stage is added [21, 22].

Although LIAs are widely used as laboratory equipment, very few versatile integrated implementations can be found in the literature for portable instruments. Some of them work in dual supply mode, not being battery-compatible [23, 24]. Others can operate with a single supply [25-27], but their power consumption lies in the order of milliwatts, which makes them unsuitable for battery-operated portable systems.

In the attempt to attain a high-performance truly portable

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LIA, the current-mode approach arises as a promising alternative: the proposals in [21, 22, 28] render good dynamic reserve figures (48 dB) with a reduction in area (0.045 mm^2) and power consumption (below 930 µW) compared to voltage-mode implementations. However, the moderate gain, in the order of 40 dB, and the diminished output range (550 mV for 1.8 V supply) of these previous current-mode LIAs limit their resolution to tens of microvolts, thus narrowing their application range.

In this work, we focus on employing the benefits from the current-mode rectification approach to develop a high resolution and high dynamic range lock-in amplifier while preserving compactness and low power operation, necessary for portable sensing applications. This integrated circuit (IC) custom proposal is validated by measuring a resistance sensor, showing good correlation with theoretical results. The paper is organized as follows: Section II describes the proposed LIA and the design of its building blocks. Section III presents the experimental characterization of the integrated prototype. Finally, conclusions are drawn in Section IV.

II. Lock-in Amplifier Architecture

The block diagram of the proposed LIA is shown in Figure 1. To increase resolution, the input stage is a high-gain fully-differential low noise preamplifier (LNP). It is followed by a voltage-to-current converter which operates with square reference signal to perform a synchronous rectification function embedded in the output current paths to reduce the area and power consumption of the entire system. The coupling between the LNP and the transconductor is done through a high pass filter (HPF) that removes the low frequency flicker noise. Next, a transimpedance amplifier based on a two-stage amplifier and a feedback resistor is used to convert the signal back to the voltage domain with high output dynamic range and linearity. Finally, an external low-pass filter (LPF) provides information of the amplitude of the input signal, assuming that the input and reference signals are synchronized and there is no phase difference between them.

In order to design a high-performance architecture, suitable for versatile autonomous portable applications, the following requirements were established: An overall gain higher than 80 dB, with an input referred-noise below 20 $nV/Hz^{1/2}$ within the operating frequency range, so as to achieve a resolution in the order of hundreds of *nV* and a dynamic reserve above 40 dB; programmable gain and programmable low (f_{HP}) and high (f_{BW}) cut-off frequencies, in the range 1–100 kHz, relevant to most microelectromechanical (MEM) resonant sensors, so that these parameters can be adjusted according to the final application; and finally, low power consumption (below 1mW) and minimal integration area are also critical design constraints. The gain allocation and the main specifications for each stage are shown in Figure 1. The design of each building block is next described.

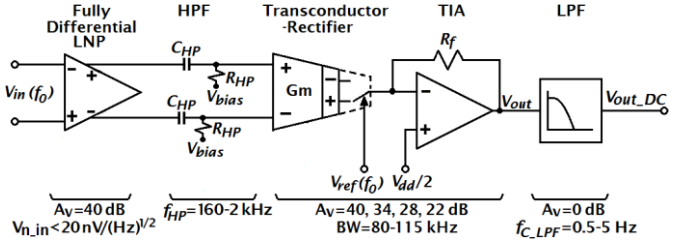
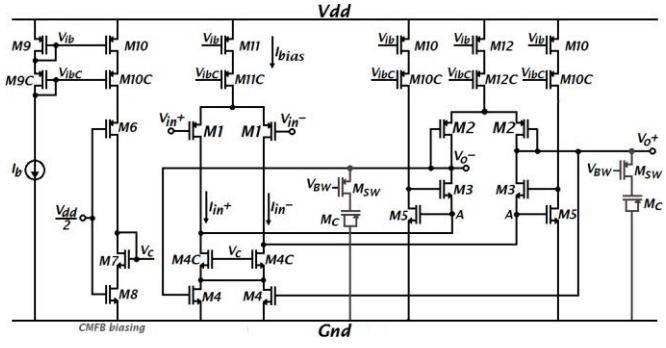


Fig. 1. Block diagram of the proposed Lock-in Amplifier.

A. Low Noise Preamplifier

A Low-Noise Preamplifier is an essential block in analog processing front-ends, since it usually determines the entire system noise floor. Its design becomes a challenge especially when further specifications such as high gain and high linearity are required with low power and area consumption. In our particular case, such a high gain LNP constitutes the LIA input stage to amplify the weak input signal while preserving low noise floor to enhance resolution. A fully differential stage was selected to increase noise immunity. The LNP gain is set to 40dB; this ensures that the noise of the entire system is determined by this stage, and renders a maximum gain of 80dB for the whole LIA. Besides, the intrinsic input-referred noise must remain below 20 $nV/Hz^{1/2}$ within the operating frequency range, to detect signals in the order of hundreds of *nV*, which was the target specification. Finally, to prevent saturation at the LIA output, it is necessary to match the output range of the LNP with the input range of the subsequent transconductor with the purpose of avoiding the saturation of the signal. Thus, the LNP is required to drive a maximum input range from units to tens of microvolts, depending on the gain setting of the transconductor.

A LNP based on a degenerated differential pair with resistive loads was first considered [22], but it did not reach the target noise figure over the 1–100 kHz range and was thus discarded. As shown in Figure 2, our final LNP consists of a transconductance input stage and a transimpedance amplifier in a folded cascode configuration [29]. The gain is given by the ratio of transconductances, $A_V = -g_{m1}/g_{m2}$, where g_{m1} is the transconductance of the input pair M1, and g_{m2} is the transconductance of the load output pair M2 of the



Transistor	M1	M2	M3	M4	M4C	M5	M6 M10 M10C
(W/L) µm/ µm	720/5	9/10	30/4	40/8	158/5	60/1	27/1

Transistor	M7 M8	M9 M9C	M11 M11C	M12 M12C	MSW	MC
(W/L) µm/ µm	20/8.5	18/1	288/1	18/6	4.5/1.3	60.4/20.7

Fig. 2. Low Noise Preamplifier.

transimpedance stage. The input signal $V_{in} = (V_{in}^{+} - V_{in}^{-})$ is converted into a differential current signal $I_{in} = (I_{in}^{+} - I_{in}^{-})$ by the input transistors M1. In order to ensure a low impedance path for I_{in}, the regulated cascode current mirror formed by transistors M3 and M5 is added. Transistors M3 are biased in weak inversion to increase their transconductance. Besides, this implementation keeps node A stable by means of the negative feedback loop, thus achieving a high output impedance [30, 31]. Common-mode feedback is performed by M4 working in the linear region as resistors controlled by the output common-mode voltage, which adjust the current to balance the operating point on the output branches.

A bias current I_b = 10 µA is used to supply the whole system and it is amplified to obtain I_{bias} = 160 µA as well as large dimensions were used for input transistors in order to increase the input transconductance (g_{m1} = 967.2 µA/V) and reduce the intrinsic noise of LNP. The output transconductance is 100 times lower, g_{m2} = 9.7 µA/V, to achieve the target gain. To adjust the LNP bandwidth, MOS capacitors M_C in series with PMOS switches M_{SW} were added to the output nodes. In this way, the contribution of noise can be minimized by limiting the system bandwidth according to the frequency of the input signal. The LNP in Figure 2 exhibits a 40.2 dB gain, with an intrinsic bandwidth of 174 kHz (when M_{SW} is off), which can be reduced down to 51 kHz when M_{SW} is turned on.

Figure 3 shows the simulated input noise spectral density of the entire lock-in amplifier acting as an amplifier, without demodulation operation, compared to that of the LNP. It can be seen how the HPF effectively limits the low-frequency noise, while for frequencies above f_{HP} the LIA noise matches the LNP noise, achieving a value below 20 nV/Hz$^{1/2}$ starting from 1 kHz. A linear output signal swing of ± 205 mV is obtained with an input signal swing of ± 2 mV. A CMRR of 95.6 dB at 100 kHz provides a high rejection to the common-mode. Its power consumption is 383 µW.

B. *High-Pass Filter*

The LNP output signal is coupled to the transconductor input through a HPF composed of a passive capacitor C_{HP}, and a high value active resistor R_{HP}, as shown in Figure 1. This simple approach eliminates the LNP offset and low frequency noise contributions before the rectification of the signal is carried out.

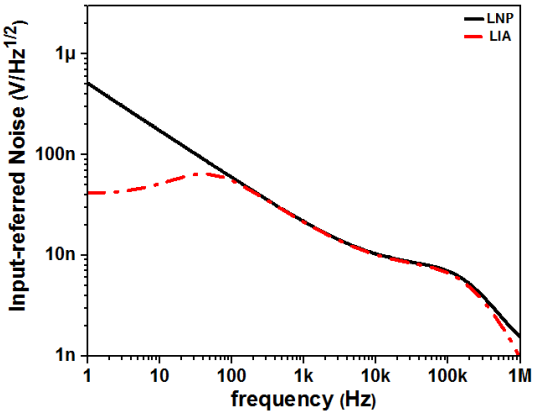
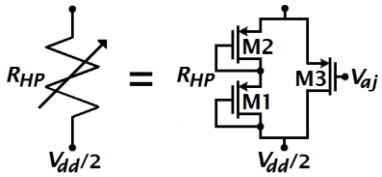


Fig. 3. Input-referred noise of the LNP and the whole LIA.

The low cut-off frequency $f_{HP} = 1/(2\pi R_{HP} C_{HP})$ is set to 450Hz to preserve a wide range of operation frequencies. A capacitance C_{HP} = 2 pF, which is high enough to neglect the effect of the input capacitance of the transconductor, was chosen to attain a hardware effective solution. Accordingly, the resistance R_{HP} must have a value of 177 MΩ. This large value discards its implementation by a passive resistor, since it would enormously increase the area of integration; besides it would not be possible to tune the resistor value to adjust the cut-off frequency over process variations. Thus, to attain a large resistance with minimum area penalty, R_{HP} was implemented with MOS transistors.

We focused on active structures commonly used in the area of biomedical instrumentation under the name of pseudo-resistors, which lead to very high resistive values [32-37]. In particular, an approach using diode PMOS transistors M1 and M2 connected in series, as shown in Figure 4, was adopted. A PMOS transistor M3 in parallel working in the cutoff region was added to adjust through its gate voltage V_{aj} the overall equivalent resistance R_{HF} in a 1:9 range. Long channel transistors were used to attain the desired high resistance values: $W_{1,2}/L_{1,2}$ = 2.5 µm/18 µm and W_3/L_3 = 2 µm/21 µm.

Figure 5 shows the frequency response of the high-pass filter under corner analysis. For a typical-typical process (*tt*) and an external voltage V_{aj} = 0.9 V the circuit has a cutoff frequency f_{HP} = 450 Hz. The frequency shifts in the fast-fast (*ff*) and slow-slow (*ss*) corners can be corrected by adjusting the voltage V_{aj},



V_{aj}	R_{HP}
0.8 V	45 MΩ
0.9 V	177 MΩ
1.2 V	280 MΩ
1.5 V	352 MΩ
1.8 V	411 MΩ

Fig. 4. R_{HP} implementation.

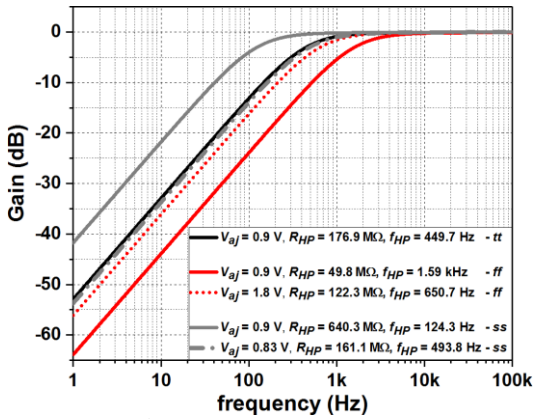


Fig. 5. R_{HP} response in frequency domain under corner variations.

TABLE I
FREQUENCY RESPONSE OF HPF UNDER CORNER ANALYSIS

Process	V_{aj} (V)	f_{HP} (Hz)
tt	0.90	450
ff	0.90	1590
ff	1.80	651
ss	0.90	124
ss	0.83	494

as highlighted in Table I, thus providing a reliable tunable resistor implementation. Note that a careful layout of this high-pass section will be required to ensure that the use of uncoupled filters do not degrade the low-frequency CMRR of the circuit due to mismatch between components.

C. Programmable transconductance/rectification stage

The design of the transconductor must comply with specific requirements, such as providing complementary outputs to straightforwardly perform the rectification of the signal and a programmable transconductance to adjust the gain of the entire LIA depending on the amplitude of the input signal, at low power consumption to preserve a power efficient system.

The topology of the combined transconductance/ rectification stage is shown in Figure 6 (a). In order to achieve a good trade-off between linearity and power consumption, a negative feedback g_m-boosted N-type differential pair with source-degeneration (M1-M2) is used. The input transistors act as enhanced voltage followers – named flipped voltage followers (FVF) [38] – and the differential input voltage $V_{in} = (V_{in}^{+} - V_{in}^{-})$ is buffered to the degeneration resistor R_{deg}. The linearized differential current signal, inversely proportional to R_{deg}, is copied out by loading nodes A with transistors M3 and M5 matched to M2. The complementary output is generated with two additional current mirroring branches (M7 and M9). The direction of the output current flow is controlled by the cascode transistors in the output branches, which also work as switches through their gate voltage V_{ref}. Thus, a phase-sensitive rectification is performed if a square signal with the same frequency as the input signal is used as V_{ref}. The mirror transistors M3, M5, M7 and M9 have a gain of 2 with respect to M2 in order to increase the transconductance.

Transconductance programmability is achieved by means of a variable degeneration resistor. To preserve linearity, reduced area consumption and, at the same time, facilitate digital gain control, the degeneration resistor consists of an arrangement of transistors connected in parallel and simultaneously acting as resistors and switches. To give more symmetry to the layout each branch in the array consists of two transistors in series, which work in the triode region when they are on. With the 3-bit array shown in Figure 6 (b), the output current is controlled by the digital word $D = \{d_2, d_1, d_0\}$ as follows:

$$I_{out} = \frac{(-1)^{Vref} \cdot M \cdot V_{in}}{R_{deg}} \left\{ \frac{1}{2^n} \left[1 + \sum_{j=0}^{n-1} \left(3^j - d_j 3^j \right) \right] \right\} \; with \; n = 3 \qquad (2)$$

Where R_{deg} are the degeneration resistors and M is the gain of the current mirror M3 and M5. The circuit, biased with I_b = 10 µA, has a programmable transconductance ranging from 90 µA/V at $D = \{111\}$ to 1.19 mA/V at $D = \{000\}$, with a constant bandwidth of 7 MHz. The total harmonic distortion (THD) remains below –66 dB up to 18 μA_{pp} output signal at 10kHz. Finally, the fact that this stage combines several functions not only minimizes its power consumption (389 µW) and integration area (0.016 mm^2) but also those of the entire system, since the number of building blocks is reduced compared with previous implementations [21].

D. Transimpedance Amplifier

The transimpedance amplifier, shown in Figure 7, converts the rectified current delivered by the transconductor into voltage. To increase the output dynamic range and maintain the linearity attained by the previous stages, it consists of a conventional two-stage amplifier and a polysilicon feedback resistor R_f = 100 kΩ, which sets the gain (100 dBΩ). The frequency compensation circuit consists of R_z = 4 kΩ, C_C = 4 pF and C_{C2} = 1.1 pF. The input signal swing is 15 μA_{pp} and the output signal swing is 1.54 V_{pp}. The power consumption is 113 µW.

Considering the cascade connection of the blocks presented so far, the total gain of the system as a function of the digital word is given by the following expression:

$$A_{VT} = \frac{(-1)^{Vref} \cdot M \cdot R_f \cdot g_{m1}}{R_{deg} \cdot g_{m2}} \left\{ \frac{1}{2^n} \left[1 + \sum_{j=0}^{n-1} \left(3^j - d_j 3^j \right) \right] \right\} \; with \; n = 3 \quad (3)$$

E. Low Pass Filter

The output LPF consists of an external second order RC passive network. The cut-off frequency was set at two different values during the LIA characterization: f_{C_LPF} = 5 Hz with 300

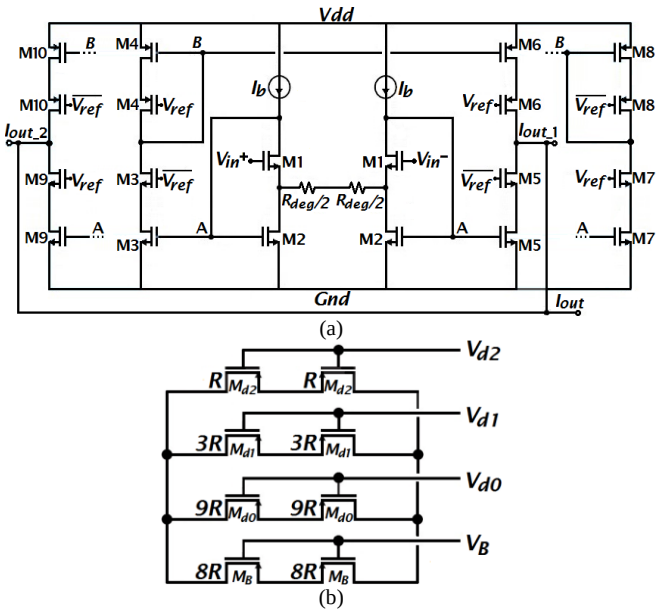


Fig. 6. (a) Transconductor/rectifier schematic; (b) Digitally programmable degeneration resistance.

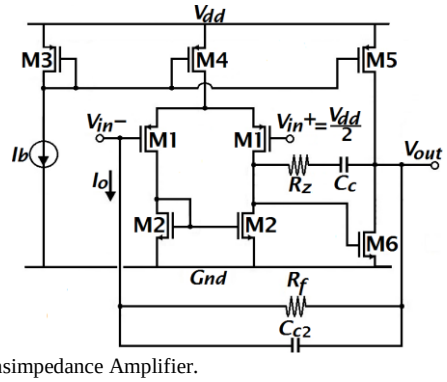


Fig. 7. Transimpedance Amplifier.

nF capacitors, and f_{C_LPF} = 0.5 Hz with 3 µF capacitors. In both cases 40 kΩ resistors were used.

III. Experimental Characterization

A. Lock-in Performance

The proposed LIA was designed in a UMC 0.18 µm CMOS process with 1.8 V single supply voltage. A photograph of the prototype, with an area of 262 µm ×280 µm, is shown in Figure 8.

Figure 9 shows the measured transfer function at each digital word when V_{ref} = 0 V, i.e., without rectification. The gain at midrange frequencies and for each digital setting is reported in Table II. It can be adjusted in a 10-dB range, from 72.6 dB to 82.6 dB, according to the input amplitude range imposed by the application.

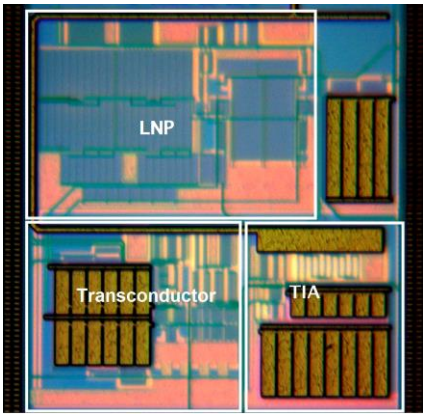


Fig. 8. Photograph of the Lock-in Amplifier prototype.

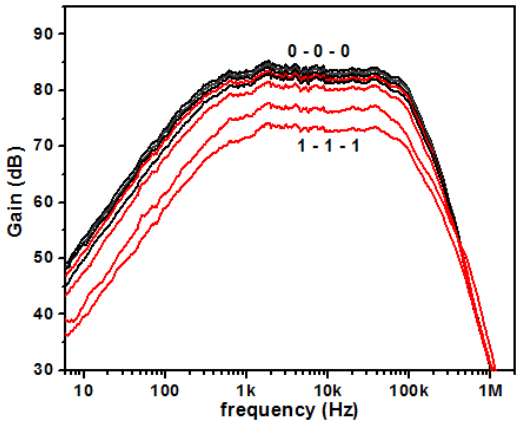


Fig. 9. Gain Programmability.

TABLE II
GAIN FOR EACH DIGITAL WORD

d_2-d_1-d_0	A_{exp} (dB)
0-0-0	82.6
0-0-1	82.2
0-1-0	81.9
0-1-1	81.2
1-0-0	80.8
1-0-1	80.3
1-1-0	75.9
1-1-1	72.6

As explained in Section II A, a 1-bit programmable on-chip capacitor was included to adjust the higher cutoff frequency (f_{BW}) of the system and limit the high frequency noise at the LNP stage. Figure 10 (a) shows this feature: f_{BW} can be set to 115 kHz (V_{BW} = V_{dd}) or 80 kHz (V_{BW} = G_{nd}). Furthermore, the tunable resistor R_{HP} of the HPF makes it possible to adjust the high-pass cutoff frequency as shown in Figure 10 (b), achieving an approximately linear variation of the resistance within the range of voltage ranging from 0.8 to 1.1 V. The band-pass response of the system results in a range of frequencies where the LIA can be used independently of the gain setting.

To test the capability of the LIA to recover signals submerged in noise, a square reference signal V_{ref} at the same frequency as the signal V_{in} to be detected is required. In the laboratory, a Source Meter SMU (Keithley 2336B) set to 1.8 V was used to introduce V_{dd} and simultaneously measure the supplied current to compute the total power consumption of the circuit. Note that a single-phase approach is not the most appropriate choice for phase recovery, that is why the characterization was carried out by a function generator ArbStudio 1104 to generate V_S and V_{ref} in-phase to determine the amplitude of the input signal. Amplifiers A1 and A2 were added to modify the amplitude of V_S by means of a linear configuration and obtain the desired differential input amplitude for V_{in}. The rectified output signal was observed with the Tektronix TDS210 oscilloscope and the DC voltage at the

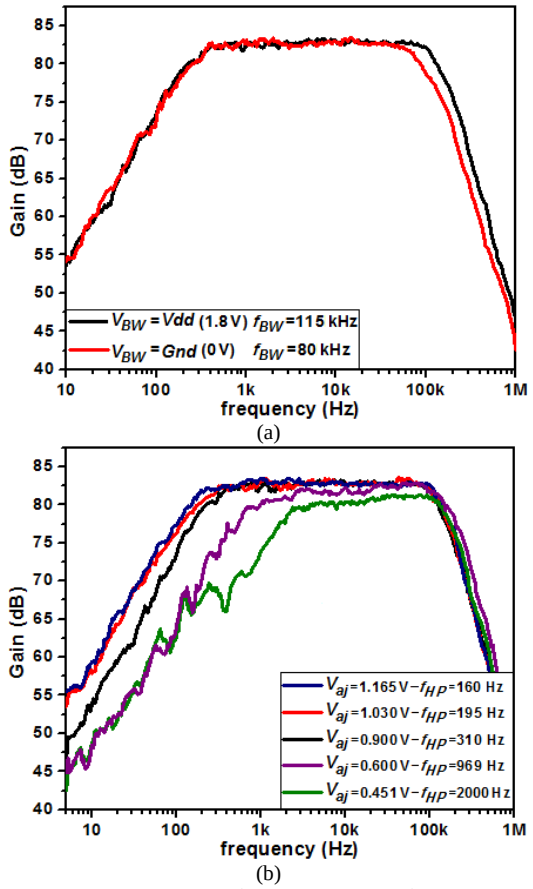


Fig. 10. Experimental response in frequency domain of the LIA: (a) Adjustment of f_{BW} by V_{BW}; (b) Adjustment of f_{HP} by V_{aj}.

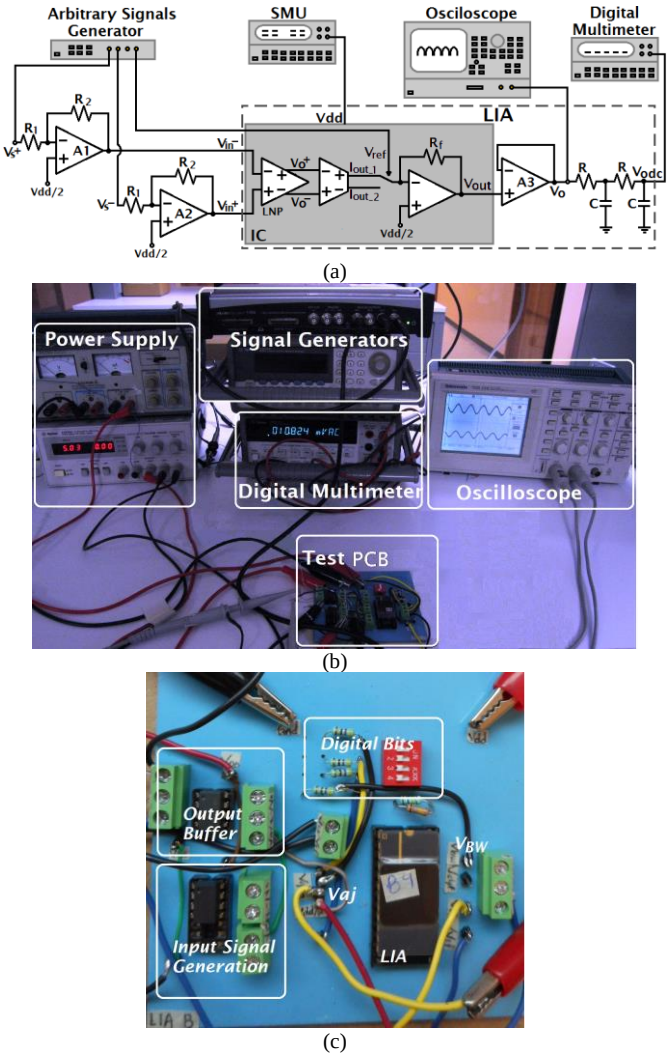


Fig. 11. Experimental Setup: (a) Block diagram; (b) Setup photograph; (c) test PCB photograph.

LPF output was measured with the Agilent 34410A 6 ½ digit digital multimeter, an output buffer A3 was added to the measurement setup for appropriate impedance coupling with the LPF as shown in Figure 11 (a) and (b). Figure 11 (c) shows a photograph of the test PCB.

The performance of the prototype was evaluated as follows. First, proper operation of the LIA was tested when processing a noise-free sine signal operating at 10 kHz with different amplitudes. The LIA was set to operate with f_{HP} = 310 Hz and f_{BW} = 115 kHz. The ideal DC output V_{out_DC} voltage is given by:

$$V_{out\_DC} = \frac{2A_V T V_{in}}{\pi} \quad (4)$$

Figure 12 shows both V_{out_DC} and the measured DC output $V_{out\_DC\_Meas}$ versus input signal at maximum and minimum gain. Since the measured signal presents offset, a calibration was necessary: an offset of 55 mV was subtracted from the experimental data. A relative error $\varepsilon_r \leq \pm 1.45\,\%$ for input signals ranging from 0.2 µV to 40 µV was obtained after calibration. The resolution of the system is 200 nV for maximum gain and 800 nV for minimum gain; and the

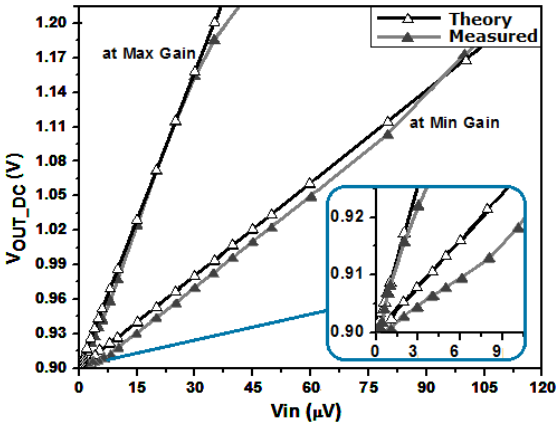


Fig. 12. DC voltage vs AC input signal at maximum gain (82.6 dB) and minimum gain (72.6 dB).

sensitivity is 7.6 mV/µV for maximum gain and 1.85 mV/µV for minimum gain.

Next, the capability of the LIA to recover information from signals buried in noise was evaluated. Note that the most important parameter of a LIA is the dynamic reserve DR, which indicates the maximum full-scale noise that can be tolerated; it can also be defined as the inverse of the worst SNR that can be tolerated at the input to obtain a full-scale output signal without saturation [7]. Noise signals were generated with a function generator Agilent 33120A. A 200 nV amplitude sine input signal at 10 kHz was immersed in 21.2 μV_{rms} white Gaussian noise with 10 MHz bandwidth. The rms value of the noise was chosen based on the maximum output amplitude that the LIA can handle before saturating. Table III summarizes the experimental data. The resulting dynamic reserve is 43.5 dB. When the cut-off frequency of the LPF is set at f_{C_LPF} = 5 Hz, the amplitude of the input signal can be determined with a relative error of 4.8 %, whereas the error is reduced to 3.5 %

TABLE III
DYNAMIC RESERVE OF LIA IN THE RECOVERY OF A SIGNAL SUBMERGED IN WHITE GAUSSIAN NOISE

V_{in} (nV)	V_n (μV_{rms})	DR (dB)	f_{C_LPF} (Hz)	V_{out_DC} (V)	$V_{out\_DC\_Meas}$ (V)	ε_r (%)
200	21.2	43.5	5.0	0.902	0.944	4.7
200	21.2	43.5	0.5	0.902	0.933	3.4

when f_{C_LPF} = 0.5 Hz, at the cost of increasing the measurement time from 0.3 s to 1.5 s. Note that these are the relative errors in the case when minimum input signal and maximum allowable input noise are considered.

For a noise-free input signal at 10kHz in quadrature with the reference signal, it was found that the output voltage of the LIA is $V_{dd}/2$, with an error lower than 0.08% both for minimum and maximum gain settings, and for the maximum allowable input amplitudes. Therefore, a high quadrature rejection would be expected if the proposed topology was modified to design a dual phase LIA for impedance measurements.

Finally, note that in equation (4) we are assuming that the sensor signal and the reference signal are in-phase, which is true for resistive sensors. However, to completely ensure this

condition, the inclusion of a phase alignment circuit would be convenient. Besides, a phase shift can be introduced by the LIA itself, if operated at low (next to the high-pass filter cutoff frequency) or high frequencies (next to the system bandwidth). This will result in a gain error, that should be calibrated for the corresponding operating frequency.

It has been shown in this Section that the proposed LIA is a highly versatile structure, as it can be adjusted to different applications with different input amplitude ranges and different operating frequencies, such as the detection of low gas concentrations [24, 26, 39] or low magnetic fields [40]. For applications that require DC rejection, the input could be done directly at the Gm-TIA stage through capacitors CHP, as proposed in [28]. This choice would allow direct coupling with lower adjustable gains, still providing adjustable cut-off frequency of the HPF and adjustable bandwidth, while reducing consumption by 42 % by eliminating the LNP. However, in order to fully profit from all the advantages of the proposed LIA, such as high gain settings, high resolution, and low input-referred noise, a capacitive coupling at the input of the proposed LIA should be used if needed [23, 39, 41].

B. Resistive Sensor Measurements

In present-day a wide diversity of resistive sensors such as piezo-resistive [42, 43], magneto-resistive sensors [44, 45] or resistive gas sensors [46-48], to mention a few, can be found in different and versatile applications. Those sensors can be characterized by a simple resistive model replicating their behavior in a simple manner [49-51]. Thus, to demonstrate the functionality of the proposed single-phase LIA a resistive divider circuit was implemented in the laboratory with temperature and light controlled conditions to eliminate any variation due to these parameters, focusing only in the detection of resistive variations. This is widely used as a typical conditioning system, being a realistic practical case, as proved in [24, 26, 39].

The measurement setup system is shown in Figure 13. The resistive sensor R_S is placed into a voltage divider with a reference resistor of 1 kΩ and stimulated with a sinusoidal voltage V_{in} = 35 µV at 10 kHz. A decoupling capacitor C_{dec} followed by an analog adder was used to set the required DC level ($V_{dd}/2$) at the LIA's input. The response was measured with 6 ½ digit digital multimeters, without LIA ($V_{o\_divider}$) and with LIA (V_{out_DC} rename as V_{odc_LIA}), for minimum and maximum gain, varying the resistance from 100 Ω to 10 kΩ, typical from piezo-resistive sensors [41, 42] and other resistive sensors [48-50].

The equivalent resistance of the sensor estimated from:

$$R_{S\_MEAS} = R_{ref}\left(\frac{A_{VT}V_{in}}{\pi V_{odc\_LIA}} - 1\right) \qquad (5)$$

The real resistance value R_S and the equivalent resistance R_{S_MEAS} using the V_{odc_LIA} measured at maximum and the minimum gain of the LIA, are presented in Table IV. Figure 14 shows the output voltage of the divider and the LIA, where can

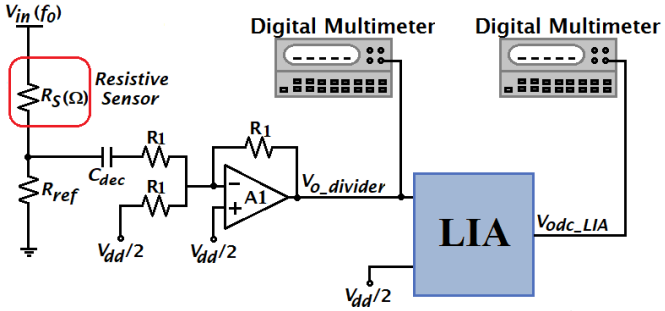


Fig. 13. Resistive Sensor measurement system with lock-in amplifier.

TABLE IV
RESISTANCE SENSOR ESTIMATED FROM LIA'S OUTPUT DC VOLTAGE

	LIA Minimum Gain		LIA Maximum Gain	
R_S (Ω)	R_{S_MEAS} (Ω)	εr (%)	R_{S_MEAS} (Ω)	εr (%)
100.8	100.7	0.1	101.7	-0.9
149.4	147.4	1.3	149.4	0.1
182.3	184.3	-1.1	184.3	-1.1
270.0	268.8	0.5	270.8	-0.3
464.2	455.5	1.9	461.1	0.7
555.1	547.4	1.4	552.7	0.4
682.6	685.2	-0.4	684.8	-0.3
818.6	814.1	0.6	820.0	-0.2
999.6	996.8	0.3	1001.4	-0.2
1200.5	1197.3	0.3	1204.4	-0.3
1500.1	1493.4	0.5	1506.5	-0.4
2201.3	2197.6	0.2	2205.4	-0.2
3303.7	3295.4	0.3	3313.2	-0.2
4998.1	4967.8	0.6	5007.0	-0.2
5605.6	5571.1	0.6	5628.1	-0.4
6807.1	6764.7	0.6	6827.3	-0.3
8204.7	8138.4	0.8	8224.6	-0.2
9997.5	9887.9	1.1	10016.0	-0.2

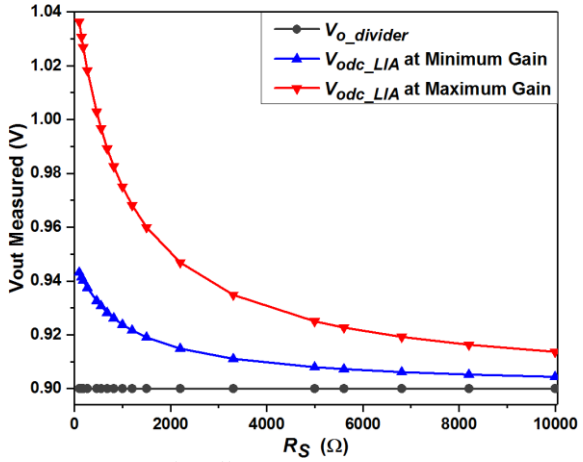


Fig. 14. Output Voltage for different R_S values using a voltage divider and the Lock-in amplifier.

TABLE V
PERFORMANCE COMPARISON OF INTEGRATED LIAS

Parameter	Proposed LIA[a, b]	[21][a]	[23]	[24][a, b]	[25]	[26]	[27][a]
CMOS Technology (µm)	0.18	0.18	0.7	0.35	0.18	0.35	0.18
Voltage Supply (V)	1.8	1.8	±2.5	±1.0	1.8	1.8	1.2
Gain (dB)	72.6-82.6	24.7-42	51-109	10-110	n.a.	106	0-40
BW (kHz)	115	125	50	n.a.	20000	0.025	700
CMRR (dB)	96@100kHz	78.3@DC	60@20kHz	n.a.	n.a.	n.a.	97
PSRR+ (dB)	85@100kHz	57.3@DC	n.a.	n.a.	n.a.	n.a.	n.a.
PSRR- (dB)	88@100kHz	50.6@DC	n.a.	n.a.	n.a.	n.a.	n.a.
Input Swing (mV_{pp})	0.24	17	0.35	0.01	n.a.	0.02	100
Output Swing (V_{pp})	1.04	1.0	1.1	1.4	1.08	n.a.	n.a.
Resolution (µV)	0.2	25	0.2	0.5	n.a.	0.012	1
Sensitivity (µV/Ω)	13.6-43	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.
Dynamic Reserve (dB)	43.5@ε_r=3.5%	35.5@ε_r=5.3%	50	n.a.	30	34	33@ε_r=2%
Input-referred noise ($nV/Hz^{1/2}$)	11.9@5kHz	n.a.	17@20kHz	34@77Hz	n.a.	n.a.	n.a.
Power Consumption (mW)	0.885	0.417	25	3	37	2	1.7
Area (mm^2)	0.075	0.013	6.5	5	5	n.a.	0.073
FOM (dB)	192	166	180	n.a.	n.a.	154	179

[a]External LPF, [b]Simulated Input-referred noise

be clearly observed that, in comparison with the voltage divider, which makes impossible the extraction of the sensor signal information, the LIA is capable to detect sensor variations with steps of tens or hundreds of Ohms, even though the input signal is in the order of hundreds of microvolts with relative error below 1.9 % over all the range.

Finally, in Table V the main characteristics of the integrated LIA are summarized and compared with other CMOS integrated implementations found in the literature. The proposed architecture shows high gain and low intrinsic-noise, which leads to a resolution in the order of hundreds of nanovolts, while it also has a wide and controllable range of operation frequencies which provides higher flexibility than other implementations to adapt the system to different applications. Only [25] and [27] can be used at higher frequencies, at the cost of power consumption. The dynamic reserve is 43.5 dB, only surpassed by [23], although the error in determining the amplitude of the input signal is not specified in that case.

For fair comparison between the topologies, a figure of merit (FOM) considering the main LIA performance parameters, previously presented in [21]:

$$FOM = DR(dB) + 10\log[BW(Hz)/[Resolution\ (\mu V)\cdot Power(W)]] \quad (6)$$

This FOM emphasizes the dynamic reserve, which is of most importance in lock-in amplifiers, as well as power efficiency for a given bandwidth BW and resolution. Therefore, a higher FOM denotes a better performance. The best FOM is achieved by the proposed LIA, which exhibits the best trade-off between DR, resolution, power consumption and BW, when compared to previous implementations found in the literature. This fact highlights that the proposed architecture is an adequate solution for low level signal detection in portable and lab-on-a-chip applications.

IV. CONCLUSION

A CMOS integrated lock-in amplifier has been presented. The prototype was designed to have high adjustable gain, bandwidth and low input noise, leading to a resolution of 200 nV and a high dynamic reserve of 43.5 dB with a relative error of 3.5 % in the signal recovery. The low power consumption of 885 µW and low integration area of 0.075 mm^2 make it highly suitable for portable devices. These obtained figures make also the proposed interface a promising solution to measure, through a dual phase LIA, electrical impedance from the new generation of CMOS integrated impedance sensors, thus empowering the outstanding challenge of implementing truly portable fully integrated measurement systems to support such sensors.

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