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An Enhanced Frequency-Adaptive Single-phase Grid Synchronization Technique

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***Abstract* — Second-order generalized integrator phase-locked loop (SOGIPLL) relies on the frequency feedback from the PLL estimation. The frequency is used to generate the equivalent in-phase and in-quadrature signals of the single-phase grid voltage. The phase-angle coupled frequency feedback makes the SOGIPLL structure vulnerable to various grid voltage transients such as voltage sag, phase-angle jumps (PAJs) and frequency variations. This paper proposes a PLL independent frequency estimation technique. It estimates the frequency using the simplified teager energy operation on the normalized in-phase voltage component output of the SOGI. The phase-angle is estimated using the third-order polynomial approximated arctangent function on the in-phase and in-quadrature outputs of the proposed frequency-adaptive SOGI. The grid synchronization technique presented in this work avoids the use of any trigonometric operations and PLL gain tuning issues. Additionally, the impact of steady-state grid disturbances, namely, harmonics and DC offset on the proposed synchronization technique is investigated. Finally, its performance robustness is compared with other techniques during both grid transients and steady-state disturbances using both simulation analysis and experimental validation.**

Keywords— arctangent, frequency variations, phase-angle jumps, single-phase converter, SOGI-PLL, synchronization, teager energy operator.

I. INTRODUCTION

The knowledge of fast and accurate grid voltage parameter estimation is essential for several applications in both the classical power systems and modern power electronics based power systems. The parameters include grid voltage amplitude, frequency and phase-angle. They are used for wide-area monitoring [1], [2], power quality (PQ) analysis [3], control and protection of grid-connected power electronic converters [4], and so on. Especially, the power converters require these parameters for grid synchronization during the integration of several renewable energy sources (RESs) such as solar and wind energy systems [5]. Additionally, robust grid synchronization of these converters is vital to provide fault ride-through as required by the modern grid codes [6]. Grid synchronization techniques are broadly classified as a) closed-loop techniques and b) open-loop techniques.

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Closed-loop grid synchronization using phase-locked loop (PLL) concept has been widely used by researchers both in academia and industries. It provides simple implementation and robust performance during normal grid operating conditions [7]-[9]. The converters use the frequency and phase-angle information estimated by PLL for their inner current control either in stationary or synchronous reference coordinates. For three-phase converter applications, phase-angle information is sufficient for control action. However, in single-phase systems, in addition to phase-angle, frequency information is also necessary to generate the equivalent in-phase and in-quadrature components of the grid voltage. Such a technique is called quadrature signal generation (QSG). The QSG unit combined with PLL, functions equivalently as a three-phase system. Several attempts have been made to implement the QSG over the years. In [10], a delay of 5 ms is provided to the original single-phase voltage signal to generate the quadrature component. These delay-based signal generations are not suitable during the occurrence of transients in the grid voltage. Generation of the quadrature signal using the differentiation of the original sinusoidal grid voltage signal is presented in [11]. However, implementation of differentiation operator in real time results in poor noise immunity. Similarly, Hilbert transform is proposed in [12] to generate the quadrature voltage component of the measured single-phase grid voltage. The use of Hilbert transform adds more computational complexity to the grid synchronization technique in real time.

QSG using second-order generalized integrator (SOGI) is developed in [13] and has gained much attention for real time application as it provides a good trade-off between accuracy and robustness during grid parameter estimation. The SOGI in combination with the synchronous reference frame phase-locked loop (SRFPLL) is called as SOGIPLL. It has been reported that SOGIPLL provides a good in-loop filtering to reject noise and harmonics in the grid voltage during synchronization [14]. SOGIPLL uses two feedback paths during grid synchronization. The first one is the estimated frequency which is fed to the SOGIQSG unit to generate the in-phase and in-quadrature components. The second one is the estimated phase which is used for frame transformation ($\alpha\beta/dq$). The presence of these two feedback paths create interdependency between the estimated frequency and phase by SOGIPLL. The interdependency functions well during normal grid operating conditions. However, during grid transients such as voltage sags, phase-angle jumps (PAJs), and frequency variations, SOGIPLL

exhibits poor dynamic performance. The reason for this is attributed to inaccurate tuning of PLL gain parameters as it maintains a design trade-off between fast (high bandwidth PLL) and robust (low bandwidth PLL and good harmonic rejection capability) grid synchronization. Hence, PLL becomes unsuitable during grid transients [15].

Apart from grid transients, steady-state grid voltage disturbances like the presence of DC offset and lower order harmonics, decrease the robustness of the SOGIPLL. Under such conditions, PLL requires extra pre- or in-loop filters to remove steady state distortions in the grid voltage [16], [17]. Various filters such as moving average filters (MAF) [18], delayed signal cancellation (DSC) block [19], and multi-harmonic decoupling cell (MHDC) [20], can be efficiently used in SOGIPLL to enhance its performance at the cost of extra delay. The PLL delay in SOGIPLL, has been suggested to be kept at more than two fundamental cycles (40 ms) in order to avoid the interaction with filtering stage [21] during grid distortions. Such large PLL delay has negative consequences during the fault ride-though operation of grid connected converters. For instance, at higher voltage sags or PAJs, converters will trip instead of providing voltage support to the grid, as the estimation of the grid voltage by SOGIPLL gets delayed longer.

In contrast to PLL based closed-loop grid synchronization, open-loop techniques have been recently proposed for single-phase grid synchronization [22]. It can alleviate the coupling issue that is present between frequency and phase in SOGIPLL. However, this technique requires a parallel frequency estimator to feed the QSG to generate the single-phase grid voltage equivalent of in-phase and quadrature signals. Under this principle, the spectral leakage information of a fixed window-based discrete Fourier transform (DFT) estimates the frequency for SOGIQSG [23]. This technique improves the synchronization dynamics during both grid transients and steady-state disturbances as compared to SOGIPLL at the cost of high computational burden. The computational burden can be relaxed by using the DFT recursively [24], [25]. With this concept, the combination of DFT and teager energy operator-based frequency estimation is proposed in [26]. However, the estimation of grid voltage amplitude and phase-angle is not included in the scope of the work. To estimate the amplitude and phase-angle, the DFT and teager energy operator-based frequency estimation is used by SOGI in a feedforward manner in our previous work [27]. The SOGI outputs are used for amplitude and phase-angle estimation. The combination of DFT, teager and SOGI provides faster grid synchronization dynamics and unsusceptible to DC offset and harmonics in the grid voltage. Nevertheless, it increases the overall computational complexity by adding another band pass filter.

A. Motivation

As discussed above, in comparison to PLL based closed-loop frequency estimation, open-loop techniques using advanced signal processing techniques such as DFT, or teager energy operator, or a combination of both as done in [27] can feed the frequency to the SOGI to provide faster amplitude and phase-angle estimations. It should be noted here that SOGI itself acts as a band-pass filter [13] and can be used to feed the normalized grid voltage signal to the teager energy operator to estimate the grid frequency. This can overcome the requirement of additional BPF as used in [27] and hence can reduce the computational burden further, which is the motivation for the research work in this paper.

B. Contributions:

To reduce the computational burden in comparison to [27] and at the same time achieve faster grid voltage parameter estimation in comparison to PLL based techniques, the contributions in this work are as follows:

- An enhanced frequency-fed SOGI is proposed for single-phase grid synchronization. The frequency is estimated based on the simplified teager energy operator using the SOGI band pass filtered (BPF) in-phase grid voltage component. The simplification relies on the three consecutive samples of the normalized grid voltage signal to provide frequency information.
- The normalization is done using in-phase and in-quadrature signal outputs of the enhanced frequency-adaptive SOGI without the addition of any extra BPF unlike [27].
- The phase-angle of the grid voltage is estimated using the arctangent function on the SOGI output. To reduce the computational complexity, the arctangent function is approximated using a third-order polynomial function with a phase unwrapping technique.
- Knowing the fact that the SOGI suffers due to the presence of DC offset in the grid voltage, the proposed technique uses a ½ fundamental period delayed signal cancellation (DSC) for the in-quadrature signal output of SOGI before it is used for grid voltage normalization. The DSC block is fed with the proposed frequency estimation to avoid any phase-angle offset during off-nominal grid frequency variations.
- The grid voltage parameter estimation robustness of the proposed synchronization technique is compared with other PLL techniques such as the SOGIPLL [13] and frequency-fixed SOGIPLL [28]. During the comparison, the impact of varying the gain of SOGI and PLL settling times are investigated by considering both grid transients and steady-state distortions. Additionally, the comparison is also made with the frequency feedforward technique detailed in [27]. The simulation analyses carried out for the above comparison study are validated with real time experiments.

C. Organization

To address the above salient features, the paper is organized as below: In Section II, single-phase grid synchronization technique using SOGIPLL is discussed. In Section III, grid synchronization using proposed frequency-adaptive SOGI based grid synchronization is explained. Section IV provides the simulation comparisons. Section V presents the experimental

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validations, and the research findings of the paper are concluded in Section VI.

II. Second-Order Generalized Integrator Phase-Locked Loop (SOGIPLL)

The single-phase grid voltage parameter estimation using SOGIPLL technique is shown in Fig. 1. In case of conventional SOGIPLL, initially the voltage signal is approximated to two orthogonally displaced signals referred as in-phase (V_α) and in-quadrature (V_β) components. The SOGI technique uses two integrators to estimate these components.

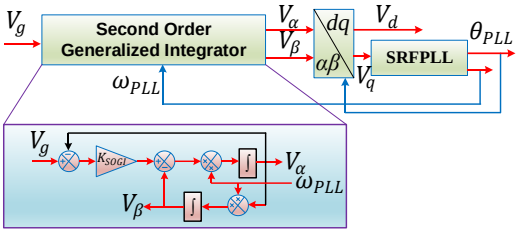

Fig. 1. Grid synchronization using SOGIPLL technique.

The two signals derived from SOGI are transformed to d and q components using the SRFPLL technique, which states that the sine of the phase angle error ($V_q = \sin(\Delta\theta)$) signal is approximated as q-component of the voltage for small angle difference and thus fed through a proportional plus integral (PI) controller to eliminate the error. Then a frequency feedforward term is added to the output and the system frequency is estimated. The estimated frequency is taken as a feedback path and fed to the SOGI generator as shown in Fig. 1. The phase-angle (θ_{PLL}) required for the $\alpha\beta$-dq conversion is derived by the integration of the estimated frequency. In this respect, the conventional SOGI-based PLL uses two feedback paths (one for frequency and one for phase angle) to provide the dq - components of grid voltage signal for the single-phase converter.

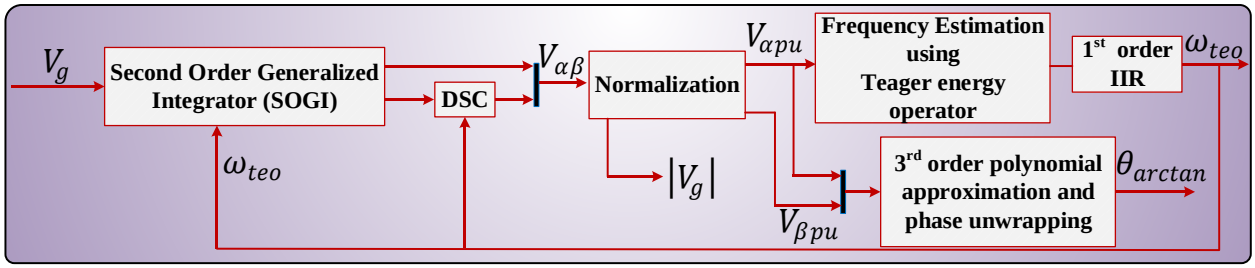

Fig. 2. Proposed frequency-adaptive SOGI based grid synchronization technique.

III. Proposed Frequency-Adaptive Second-Order Generalized Integrator

The grid synchronization using the proposed frequency-adaptive SOGI is shown in Fig. 2. The amplitude, frequency and phase-angle estimations of the grid voltage using the proposed technique are explained in the following sections.

A. Frequency estimation using teager energy operator (TEO)

The frequency of the grid voltage ($V_g(n)$) can be estimated using teager energy of the signal using either 3 or 5 samples depending on the information of the grid voltage amplitude [29]-[30]. Accordingly, a two-step estimation of the grid voltage frequency (ω_g) is carried out as follows.

Step- 1: Let us say, the instantaneous grid voltage ($V_g(n)$) is represented by a cosine signal as

$$V_g(n) = |V_g(n)| \cos(\omega_g n T_s + \varphi_g) \tag{1}$$

So, according to teager energy operator principle, energy of the grid voltage is calculated using three consecutive samples as given by,

$$\begin{aligned} E[V_g(n)] &= \frac{1}{{T_s}^2} \times [V_g(n)^2 - V_g(n-1)V_g(n+1)] \\ &= |V_g(n)|^2 \sin^2(\omega_g T_s) \\ &= |V_g(n)|^2 (\omega_g T_s)^2 \end{aligned} \tag{2}$$

The discrete difference of the grid voltage signal ($V_g\dot{(}n)$) as per discrete energy separation algorithm (DESA)-II can be obtained as [29],

$$\begin{aligned} V_g\dot{(}n) &= \frac{V_g(n+1) - V_g(n-1)]}{2T_s} \\ &= \frac{|V_g(n+1)| \cos(\omega_g(n+1)T_s + \varphi_g) - |V_g(n-1)| \cos(\omega_g(n-1)T_s + \varphi_g)}{2T_s} \\ &= V_g(n) \sin(\omega_g T_s) \sin(\omega_g T_s + \varphi_g) \end{aligned} \tag{3}$$

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The teager energy of the rate of the change of the grid voltage ($V_g(\dot{n})$) is given by,

$$E\left[\dot{V_g}(n)\right] = \frac{1}{4 \times {T_s}^2} \times [\{V_g(n+1) - V_g(n-1)^2\} - \left(V_g(n+2) - V_g(n)\right) \times \left(V_g(n) - V_g(n-2)\right)] \quad (4)$$

Putting the value for $V_g(n)$ in (4), and solving trigonometric identities we get,

$$E\left[\dot{V_g}(n)\right] = \left|V_g(n)\right|^2 \sin^4(\omega_g T_s) \quad (5)$$

Dividing (5) by (2) and solving for f_g, we get,

$$f_g = \frac{1}{2\Pi T_s}\left(\sin^{-1}\left(\sqrt{\frac{E\left[\dot{V_g}(n)\right]}{E\left[V_g(n)\right]}}\right)\right) \quad (6)$$

The implementation of (6) is shown in Fig. 3 (a). Here, it is observed that frequency estimation takes five samples ($5T_s$) to solve (6), provided the amplitude of the signal, i.e., $\left|V_g(n)\right|$ is unknown. However, if $\left|V_g(n)\right|$ is known, frequency can be estimated from (2), using only three consecutive samples by following step 2. The grid voltage normalization technique is explained in the following section.

Step- 2: From (3) we get,

$$\sin^2(\omega_g T_s) = \frac{E\left[V_g(n)\right]}{\left|V_g(n)\right|^2}$$

$$\sin^2(\omega_g T_s) = E\left[V_g(n)\right], \quad \text{if } \left|V_g(n)\right| = 1.0 \text{ p.u.} \quad (7)$$

$$\omega_g = \frac{1}{T_s}\sin^{-1}\sqrt{E\left[V_g(n)\right]}$$

$$f_g = \frac{1}{2\pi T_s}\sin^{-1}\sqrt{E\left[V_g(n)\right]}$$

Approximation of '$\sin^{-1}$' to reduce computational burden is done using its Taylor series expansion under the assumption that the sampling frequency ($f_s = 10$ KHz) > 8 times the fundamental frequency (f =50 Hz)) as given by,

$$\sin^{-1}(x) \approx x \quad (8)$$

Thus (7) is simplified as

$$f_g = \frac{1}{2\Pi T_s}\left(\sqrt{[V_{pu}(n)^2 - V_{pu}(n-1)V_{pu}(n+1)]}\right) \quad (9)$$

The approximation model is shown in Fig. 3(b).

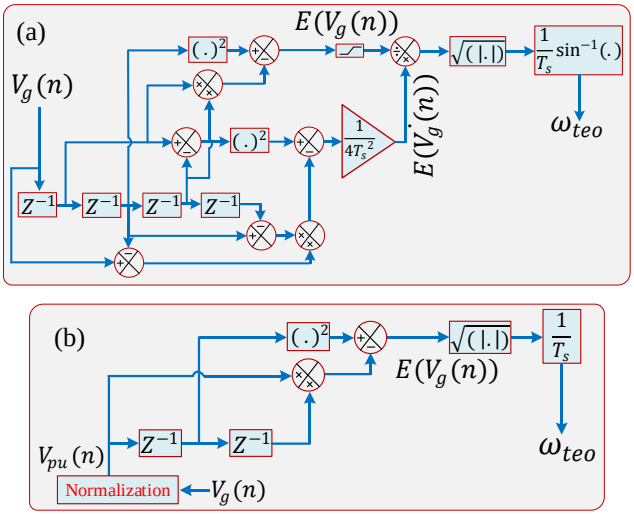

Fig. 3. Frequency estimation of grid voltage (V_g) using teager energy operator in discrete domain: (a) actual model and (b) simplified model.

B. Phase estimation using third-order polynomial approximation of arctangent function and unwrapping

As mentioned in the previous section, for phase estimation, arctangent function is used over the $\alpha\beta$-components which are extracted using the proposed frequency-adaptive SOGI as given by,

$$\theta_{arctan} = \arctan\left(\frac{V_\beta}{V_\alpha}\right) \quad (10)$$

Generally, arctan [.], function requires high computational burden to be implemented in low cost digital signal processor. To avoid such computationally demanding function, a third-order polynomial approximation of the function is used as given by [31],

$$\theta_{arctan} = \arctan(x) \quad (11)$$

$$\cong \frac{\pi}{2} \times \frac{{V_\beta}^3 + {V_\beta}^2 V_\alpha + 0.6404 V_\beta {V_\alpha}^2}{{V_\beta}^3 + 1.6404 {V_\beta}^2 V_\alpha + 1.6404 V_\beta {V_\alpha}^2 + {V_\alpha}^3}$$

The unwrapping of the estimated phase-angle (θ_{arctan}) is done using four quadrant approximations as given by,

$$If \begin{cases} V_\beta > 0 \text{ and } V_\alpha > 0 \text{ then } \theta_{arctan} = \theta_{arctan}; \\ V_\beta > 0 \text{ and } V_\alpha < 0 \text{ then } \theta_{arctan} = \pi - \theta_{arctan}; \\ V_\beta < 0 \text{ and } V_\alpha < 0 \text{ then } \theta_{arctan} = \pi + \theta_{arctan}; \\ V_\beta < 0 \text{ and } V_\alpha > 0 \text{ then } \theta_{arctan} = 2\pi - \theta_{arctan}; \end{cases} \quad (12)$$

C. Amplitude estimation with grid voltage normalization

In the proposed technique, the fundamental grid voltage amplitude is estimated from the absolute values of the in-phase

(V_α) and in-quadrature (V_β) components extracted using the SOGIQSG unit. Unlike the conventional SOGIPLL technique, the frequency to the SOGIQSG unit is provided by the simplified teager energy operator as shown in Fig. 4(b). The frequency domain transfer functions of the in-phase ($V_\alpha(s)$) and in-quadrature signals ($V_\beta(s)$) with respect to the grid voltage ($V_g(s)$) are given by,

$$G_{\alpha SOGI} = \frac{V_\alpha(s)}{V_g(s)} = \frac{k_{SOGI}\omega_{teo}s}{s^2 + k_{SOGI}\omega_{teo}s + {\omega_{teo}}^2} \tag{13}$$

$$G_{\beta SOGI} = \frac{V_\beta(s)}{V_g(s)} = \frac{k_{SOGI}{\omega_{teo}}^2}{s^2 + k_{SOGI}\omega_{teo}s + {\omega_{teo}}^2} \tag{14}$$

where $\omega_{teo} = 2\pi f_{teo}$ and f_{teo} is the teager estimated frequency. The value of k_{SOGI} is chosen as $\sqrt{2}$ to achieve a good trade-off between the estimation robustness and harmonic rejection capability of the SOGIQSG unit while generating the equivalent voltage components [14]. It can be seen from (13) that $V_\alpha(s)$ is the band pass filtered equivalent in-phase grid voltage signal. In this paper, it is used as the input signal for the proposed frequency estimator after normalization. Using V_α and V_β, the fundamental grid voltage amplitude (corresponding to 50 Hz) is estimated as given by,

$$\left|V_g(n)\right| = \sqrt{{V_\alpha}^2(n) + {V_\beta}^2(n)} \tag{15}$$

The adaptive frequency fed SOGI filtered in-phase voltage component (V_α) is normalized as given by,

$$V_{pu}(n) = V_{apu}(n) = \frac{V_\alpha(n)}{\left|V_g(n)\right|} \tag{16}$$

where $V_{pu}(n)$ is used for the frequency estimation using (9).

D. DC offset elimination

As the proposed frequency estimation requires the normalized grid voltage using V_α and V_β signals, it is obvious that it will be affected by the presence of DC offset in the grid voltage (V_g). To eliminate this V_β is passed through a frequency-adaptive ½ fundamental cycle delayed signal cancellation (DSC) principle as given by,

$$V_\beta = 0.5 \times V_\beta \times \left(1 - e^{\left(\frac{-T_0}{2 \times T_s}\right)}\right) \tag{17}$$

The proposed frequency estimation is used to tune the DSC block to avoid any offset in the estimated amplitude or phase-angle. The output of the DSC is used for the normalization process as discussed above.

IV. SIMULATION RESULTS

The proposed adaptive frequency-fed SOGI based grid synchronization is modelled using the MATLAB®/SIMULINK software. The parameters such as gain of SOGI (k_{SOGI}), cut-off frequency of the infinite impulse response (IIR) filter (f_c) and sampling frequency (f_s) for the proposed frequency estimation technique are selected as 1.414, 20 Hz and 10 kHz respectively.

The dynamics of the estimated frequency, amplitude and phase-angle error using the proposed technique during various grid voltage transients are investigated with and without the addition of steady-state disturbances (5% DC offset and harmonics with 5% THD) as shown in Fig. 4(a) and Fig. 4(b) respectively. The considered transients are, 50% sag at t = 0.25 s, -45° PAJ at t = 0.5 s and +1 Hz frequency variations at t = 0.8s. The proposed method (Type-IV) is compared with the conventional SOGIPLL (Type-I) [13], frequency-fixed SOGIPLL (FFSOGIPLL) (Type-II) [28], and the method explained in [27] (Type-III). The parameters selected for the proposed technique is kept the same for other techniques as well for a fair comparison. The settling time for PLL in case of SOGIPLL and FFSOGIPLL is set as 120 ms.

The parameters chosen for comparison among the above-mentioned grid synchronization techniques are the overshoot (in %) and settling time (t_s). To have a clear picture on the effect of each disturbance (sag, PAJ and frequency variations) on the estimated frequency, amplitude and phase-error, these parameters are recorded separately as given in TABLE-I, TABLE-II, and TABLE-III. While considering the frequency dynamics during the transients, it is observed that the proposed technique provides the fastest response in comparison to other techniques. Similar to the technique in [27], no overshoot during the step change in frequency is observed with the proposed technique. However, during sag and PAJ, the proposed technique is observed to experience more overshoot as compared to the rest of the techniques. Similarly, the proposed technique retains its faster dynamics in the estimated amplitude as given in TABLE-II. The overshoot observed for the proposed technique at the point of frequency step is 1%. The value is highest for [27] as 1.5%. During the PAJ, a lower amplitude overshoot as compared to [27] is noticed for the proposed technique while it is slightly higher than PLL techniques. During the sag inception, the overshoot is observed to be lesser than PLL techniques and higher as compared to [27].

The dynamics observed in the estimated phase-angle error as given by TABLE-III reveals that in comparison to SOGIPLL and FFSOGIPLL, the proposed technique provides more robustness during PAJ and frequency variations both in terms of overshoot and amplitude. However, during voltage sag its lower settling time is compromised with higher overshoot. As compared to [27], the proposed technique provides 20 ms lesser settling time during all the transient events and comparable overshoots.

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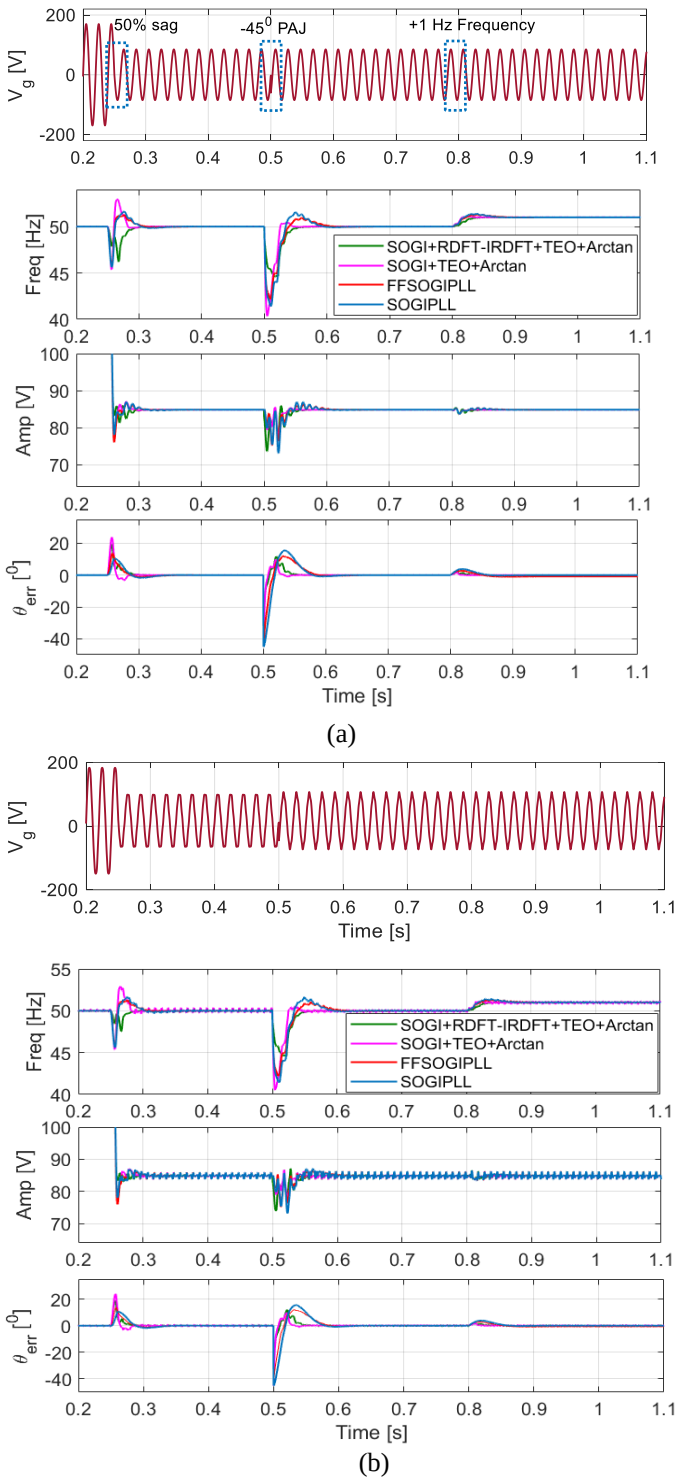

Fig. 4. Grid synchronization dynamics comparison during 50% sag at t = 0.25s, -45° PAJ at t = 0.5 s and +1 Hz frequency variations at t = 0. 8 s: (a) with undistorted grid voltage, (b) with grid voltage distortion having 5% DC offset and harmonics (5% THD).

In contrast, with the addition of harmonics, in the grid voltage, [27] provides the best harmonic rejection capability as it contains an additional DFT based BPF. The harmonic rejection performance of the proposed technique is observed to be in between [27] and the SOGIPLL and is comparable with FFSOGIPLL. This concludes that the proposed grid synchronization technique can provide a good trade-off among computation complexity, dynamic performance, and steady-state harmonic rejection capability. The harmonic rejection capability of the proposed technique can further be enhanced by slightly controlling the gain of SOGI BPF at the expense of extra delay which will be demonstrated in the experimental section.

TABLE I. FREQUENCY DYNAMICS DURING GRID EVENTS

Grid Event	Type-I		Type-II		Type-III		Type-IV	
	O	t_s	O	t_s	O	t_s	O	t_s
+1 Hz Var.	1.4	120	1	110	0	70	0	50
-45° PAJ	16	120	12	110	14	70	18	50
50% sag	8	120	8	110	6	70	10	50

TABLE II. AMPLITUDE DYNAMICS DURING GRID EVENTS

Grid Event	Type-I		Type-II		Type-III		Type-IV	
	O	t_s	O	t_s	O	t_s	O	t_s
+1 Hz Var.	1.4	120	1	110	1.6	70	1	50
-45° PAJ	5	120	5	110	12	70	6	50
50% sag	7	110	9	110	1	70	7	50

TABLE III. PHASE ERROR DYNAMICS DURING GRID EVENTS

Grid Event	Type-I		Type-II		Type-III		Type-IV	
	O	t_s	O	t_s	O	t_s	O	t_s
+1 Hz Var.	1.2	120	1	110	0.6	70	0.5	50
-45° PAJ	4	120	4	110	3	70	2	50
50% sag	0.9	120	1	110	3	70	6	50

*Type-I: SOGIPLL, Type-II: FFSOGIPLL, Type-III: Ref [27] and Type-IV: Proposed Technique.

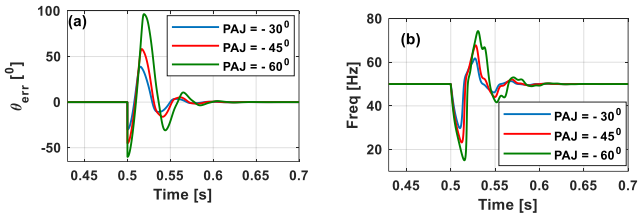

Fig. 5. (a) Phase-angle error and (b) Frequency dynamics with fast SOGIPLL (t_s = 60 ms) during the combination of 50% voltage sag and various PAJs.

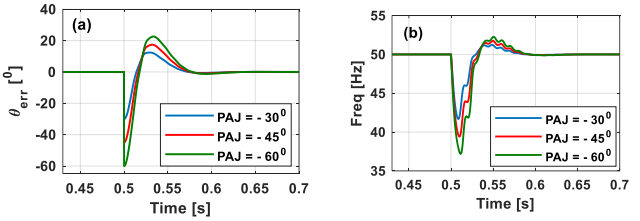

Fig. 6. (a) Phase-angle error and (b) Frequency dynamics with slow SOGIPLL (t_s = 120 ms) during the combination of 50% voltage sag and various PAJs.

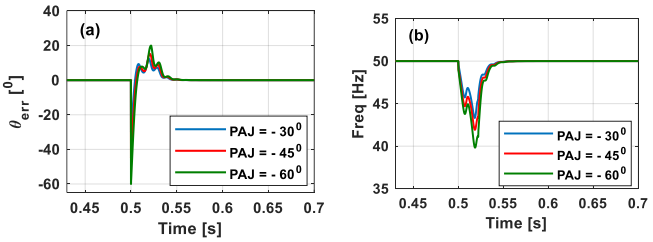

Fig. 7. (a) Phase-angle error and (b) Frequency dynamics with [27] during the combination of 50% voltage sag and various PAJs.

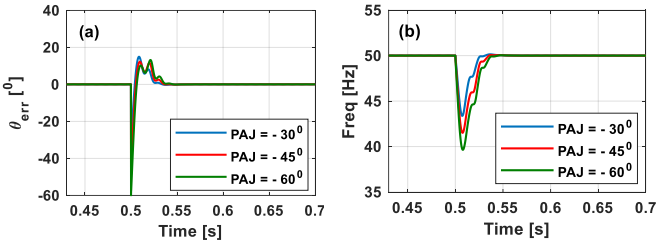

Fig. 8. (a) Phase-angle error and (b) Frequency dynamics with the proposed technique during the combination of 50% voltage sag and various PAJs.

Further the grid synchronization performance of the proposed technique is investigated assuming a realistic grid fault having both voltage sag and PAJs at the same instance (at t = 0.5s). Three different PAJs are tested such as -30°, -45° and -60° along with 50% voltage sag. The phase-error and frequency dynamics of the proposed technique (Type-IV) are compared with the fast SOGIPLL with settling time 60 ms (Type-Ia), the slow SOGIPLL with settling time 120 ms (Type-Ib), and the ref [27] (Type-III) as shown in Fig. 5, Fig.6, Fig.7 and Fig.8 respectively. The overshoots (in %) and the settling times (in ms) observed in the estimated phase-angle error and frequency are measured for all the techniques and provided in TABLE-IV and TABLE-V respectively. It can be observed that for all the techniques, higher amount of PAJs lead to higher overshoots. By reducing the settling time of SOGIPLL from 120 ms to 60 ms, more spurious dynamics are observed in case of frequency (for instance when the amount of PAJ added is 60°). On the other hand, both [27] and proposed technique show improved dynamics as compared to the PLL based techniques in terms of both the settling time and the overshoots. Moreover, the overshoots of the proposed technique are less as compared to [27] at higher PAJs, while they are almost identical at lower PAJs. However, the settling time of the proposed technique is observed to be lesser than [27] for all of the PAJs. In the case of [27], the delay is due to the additional use of BPF.

TABLE IV. PHASE ERROR DYNAMICS DURING VARIOUS PAJs

PAJs	Type-I		Type-Ia		Type-III		Type-IV	
	O	t_s	O	t_s	O	t_s	O	t_s
-30°	2	120	13	60	2	70	2	50
-45°	5	120	15	60	4	70	3	50
-60°	6	120	27	60	5	70	4	50

TABLE V. FREQUENCY DYNAMICS DURING VARIOUS PAJs

PAJs	Type-I		Type-Ia		Type-III		Type-IV	
	O	t_s	O	t_s	O	t_s	O	t_s
-30°	14	120	40	60	12	70	12	50
-45°	22	120	56	60	14	70	13	50
-60°	26	120	80	60	20	70	20	50

*Type-I: Slow SOGIPLL, Type-Ia: Fast SOGIPLL, Type-III: Ref [27] and Type-IV: Proposed Technique.

Furthermore, the proposed technique and [27] are compared with [32] in which the combinations of Kalman filter and frequency locked-loop (FLL) is used for grid synchronization. In [32], the test cases 3 (frequency step), 4 (voltage sag) and 6 (PAJ) are considered for comparison. The settling times for the estimated frequency during the grid events are provided in TABLE-VI. It is observed that for test cases 3 and 6, the settling times for frequency is 5 and 4 fundamental time periods (i.e., 100 ms and 80 ms) respectively. While the settling time for test case 4 is 30 ms. In contrast, the settling time of the proposed technique during frequency step and PAJs is observed to be lesser than four fundamental time periods (i.e., 50 ms). Similarly, response time of [27] is observed to be 70 ms, which is again lesser than the settling time observed in case of [32]. However, during voltage sag, the settling times of both [27] and the proposed technique are observed to be higher than [32].

TABLE VI. SETTLING TIME COMPARISON DURING VARIOUS GRID EVENTS

Grid Event	[32] *t_s	[27] t_s	Proposed t_s
Voltage sag	30	70	50
Phase-angle jump	80	70	50
Frequency Variation	100	70	50

* The values given are as per [32].

V. EXPERIMENTAL RESULTS

The performance of the proposed hybrid SOGIPLL is tested experimentally during real time grid transients and distortions. The experimental setup used for validation is shown in Fig. 9. The grid transients such as voltage sag, frequency variations and phase-jump scenarios are programmed in real time using a programmable AC power supply (REGATRON 4-quadrant grid simulator). The algorithm for the proposed frequency-adaptive SOGI based synchronization is developed using MATLAB/SIMULINK coder. The software is interfaced with real time hardware using a dSPACE1103 (DS1103) control board and a personal computer (PC). The line to ground voltage is measured using a voltage sensor (LEM LV 25– 400) and fed to the controller desk. The measured voltage is attenuated by ± 10 V to be compatible with the DS1103 control board. The experimental outcome obtained are discussed below. The grid voltage events programmed for the comparison of the synchronization techniques are provided in Fig. 10.

Fig. 9. Experimental Set up for real time implementation of the proposed technique.

A. Results

The frequency dynamics of the proposed technique is compared with Types-I, II and III. Two different PLL settling times, 120 ms and 60 ms are considered for comparison. The experimental results of comparisons for 120 ms PLL settling time are given in Fig. 11 (a), (b) and (c) during +1 Hz frequency variation, -45° PAJ and 50% sag in the grid voltage respectively.

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The obtained results match with that of simulation analysis. Additionally, the dynamics for 60 ms PLL settling time are also investigated using experiments as shown in Figs. 12 (a), (b), and (c). It is observed that the proposed technique and Type-III outperforms the SOGIPLL and FFSOGIPLL technique in terms of overshoots observed in the frequency dynamics. The higher overshoot observed for 60 ms PLL settling time as compared to that for 120 ms is attributed to the increase in the proportional gain parameter of the PLL [21].

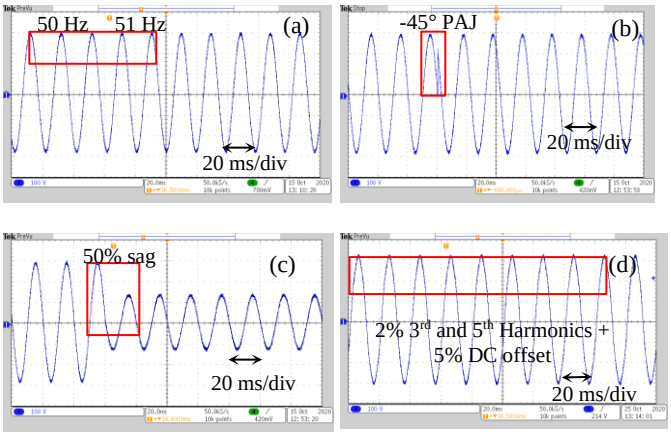

Fig. 10. Grid voltage disturbances: (a) +1 Hz Frequency variations, (b) -45° PAJ and (c) 50% sag, and (d) Harmonics (2% 3rd and 5th) + 5% DC offset.

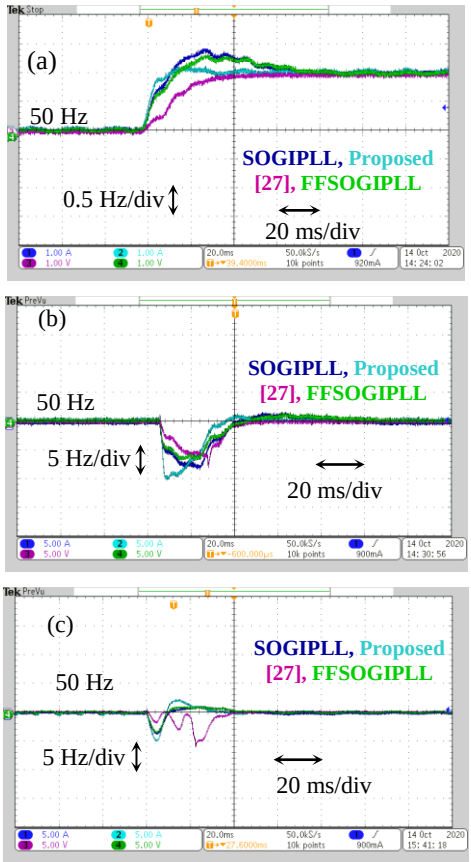

Fig. 11. Frequency dynamics during (a) +1 Hz Frequency variations (b) -45^0 PAJ and (c) 50% sag. (PLL settling time = 120 ms): Ch-1: SOGIPLL, Ch-2: Proposed, Ch-3: ref [27], Ch-4: FFSOGIPLL.

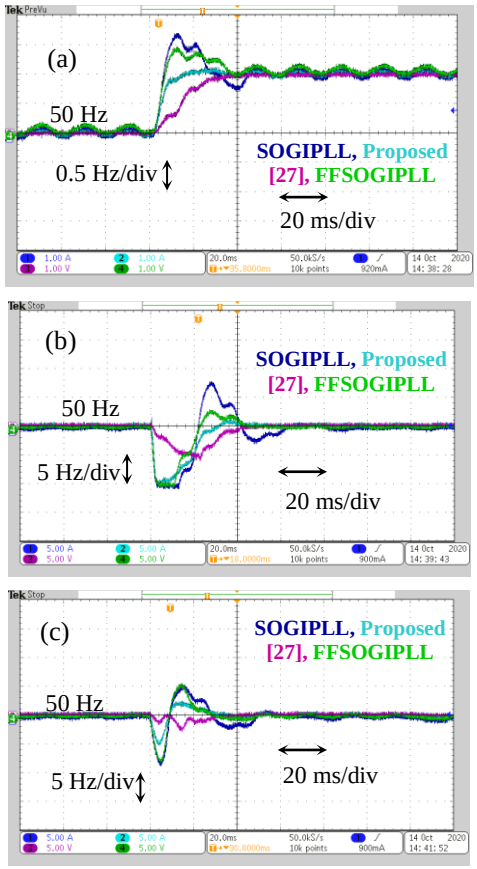

Fig. 12. Frequency dynamics during (a) +1 Hz Frequency variations (b) -45^0 PAJ and (c) 50% sag. (PLL settling time = 60 ms): Ch-1: SOGIPLL, Ch-2: Proposed, Ch-3: ref [27], Ch-4: FFSOGIPLL.

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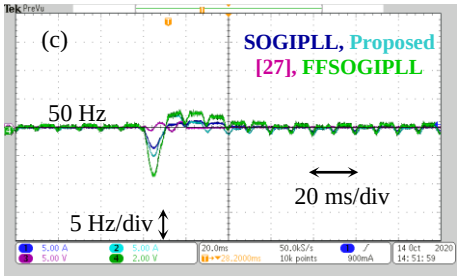

Fig. 13. Frequency dynamics with 2% 3rd and 5th harmonics during (a) +1 Hz Frequency variations (b) -45^0 PAJ and (c) 50% sag. (PLL settling time = 120 ms and k_{SOGI} = 1.414): Ch-1: SOGIPLL, Ch-2: Proposed, Ch-3: ref [27], Ch-4: FFSOGIPLL.

In the second part of the experiment, the impact of varying the gain of the SOGI BPF (k_{SOGI}) on the various grid synchronization techniques during harmonically polluted grid is demonstrated. The harmonics considered are 2% 3rd and 5th. The results with SOGI BPF gain of 1.414 (used for simulation) are shown in Figs. 13 (a), (b), and (c) and for 0.707 are shown in Figs. 14 (a), (b), and (c). It is observed that with decreasing gain, the harmonic rejection capability of the proposed technique along with SOGIPLL and FFSOGIPLL is improved with additional delay. However, for Type-III, the performance is observed to be superior as compared to others.

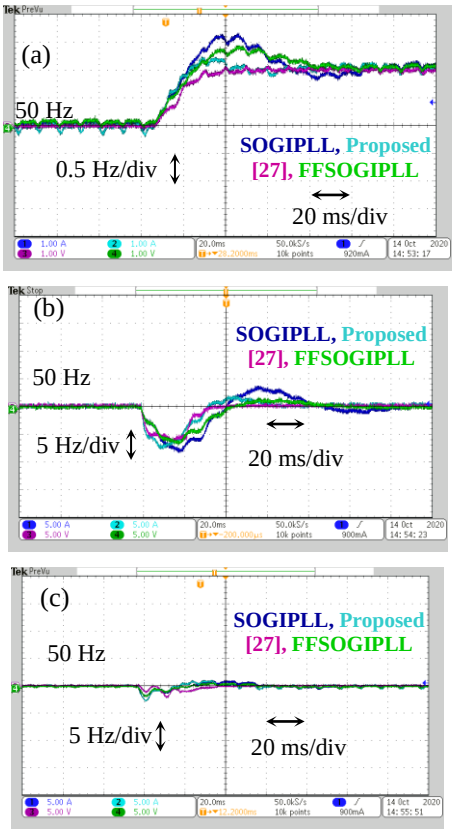

Fig. 14. Frequency dynamics with 2% 3rd and 5th harmonics during (a) +1 Hz Frequency variations (b) -45^0 PAJ and (c) 50% sag. (PLL settling time = 120 ms and k_{SOGI} = 0.707): Ch-1: SOGIPLL, Ch-2: Proposed, Ch-3: ref [27], Ch-4: FFSOGIPLL.

Further the impact of the addition of 5% DC offset in the grid voltage on the frequency estimation by the proposed and other techniques is analysed. Especially without and with delayed signal cancellation filter responses are studied as shown in Fig. 15. It can be observed that without the use of DSC filter, excluding Type-III, all the other three techniques contain ripples in the estimated frequency (refer to Fig. 15 (a)). On the other hand, as shown in Fig. 15 (b), the fixed frequency (corresponding to 50 Hz) DSC filter can eliminate the frequency ripple as long as the grid frequency remains at 50 Hz. When the frequency changes to 51 Hz, the ripples again appear although comparatively lesser. In contrast, this issue is eliminated by making DSC frequency-adaptive (with frequency estimation) as shown in Fig. 15 (c).

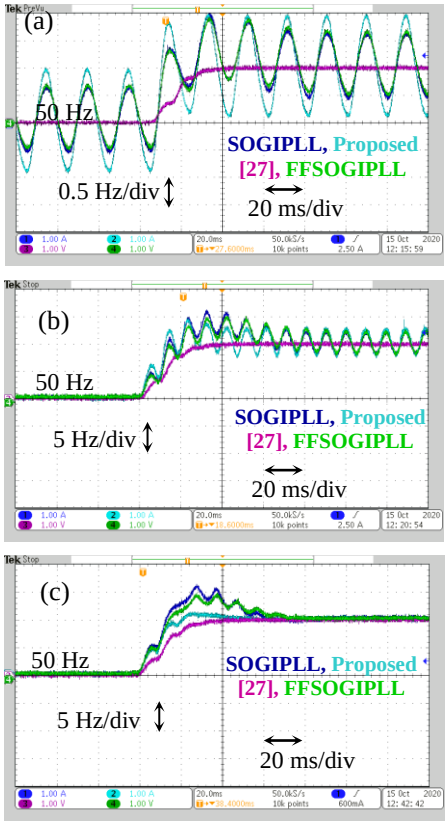

Fig. 15. Impact of addition of 5% DC offset in the grid voltage on frequency estimation: (a) no use of DSC, (b) use of fixed frequency DSC, and (c) use of frequency-adaptive DSC: Ch-1: SOGIPLL, Ch-2: Proposed, Ch-3: ref [27], Ch-4: FFSOGIPLL.

B. Discussion

In case of the PLL based grid synchronization techniques, the closed-loop gain parameters are affected by the selection of the settling time and bandwidth (refer (19) in Appendix). Higher settling time reduces the proportional gain of the PLL loop. Additionally, with higher settling time the bandwidth of the PLL loop decreases which ensures a better harmonic rejection capability. On the other hand, lower settling time increases the bandwidth of the PLL and thereby increases the proportional gain. The increase in the proportional gain further increases the integral gain as well. With the increase of both the gain parameters of the PLL loop, more overshoots are observed

in the estimated frequency during grid transients such as voltage sag, frequency variations and PAJs. This can be inferred from Fig. 11 and Fig. 12.

On the contrary, the proposed synchronization technique is free from the PLL gain tuning issue. However, it uses the SOGI BPF for pre-filtering and normalization. The band width of the SOGI BPF is controlled by the selection of the gain of SOGI i.e., k_{SOGI} (refer (13) and (14)). Lower value of k_{SOGI} increases steady-state disturbance rejection capability while higher value improves the transient dynamics. This can be observed from Fig. 13 and Fig. 14. The SOGI acts the same way for PLL based techniques. The presence of the DC offset is a common problem for the PLL and the proposed technique as it results in ripples in the estimated frequency. This problem is overcome by using a delayed signal cancellation technique for the in-quadrature component output of the SOGI which eliminates the amplitude mismatch. It further removes the ripple content in the estimated frequency. The poor frequency dynamics by PLL as a result of grid transients is fed to this delay signal cancellation filter during frequency adaptability. This is improved by feeding the estimated frequency using the proposed technique. This is shown in Fig. 15.

C. Computational Complexity

Computational complexity is compared on the basis of the use of number of mathematical operators such as additions (+), subtractions (−), multiplications (×) and divisions (÷). It is also compared with the use of number of trigonometric functions (sin, cos) and square root (√) functions. It can be noticed from TABLE-VII, that the proposed technique (Type-IV) contains the least number of mathematical operators. Moreover, it does not use any trigonometric operators unlike the other three techniques. On the other hand, ref [27] (Type-III) uses the highest number of operators as it uses an additional BPF for pre-filtering and normalization. In contrast, for the rest of the three techniques SOGI is used as a common BPF.

TABLE VII. COMPARISON OF COMPUTATIONAL COMPLEXITY

Techniques	+	-	×	÷	Trig.	√.
Type-I	7	3	8	5	2	1
Type-II	7	3	9	6	2	1
Type-III	9	5	11	3	2	3
Type-IV	4	3	7	2	0	2

*Type-I: SOGIPLL, Type-II: FFSOGIPLL, Type-III: Ref [27] and Type-IV: Proposed Technique.

The computational complexities of the above four types are further measured and compared using their processing times. The algorithm involved in each type is run individually using MATLAB®/SIMULINK 2018b version in an Intel(R) Core(TM) i5-8250U CPU @ 1.60GHz processor speed. The processing times are recorded using '*Simulink Profiler*' option for each type separately as given in TABLE VIII. It can be observed that the processing time by the CPU is highest (i.e., 6.64s) for the Type-III, while it is lowest (i.e., 4.95s) for the proposed method, Type-IV. As informed from Table VII, Type-III has the highest no of operators and Type-IV the least, leading to the results in Table VIII. Further, the processing times for the PLL techniques are observed to be 5.19s for Type-I and 5.88s for Type-II.

TABLE VIII. COMPARISON OF CPU PROCESSING TIME

Types	Type-I	Type-II	Type-III	Type-IV
CPU Processing Time	5.19s	5.88s	6.64s	4.95s

VI. CONCLUSION

This paper proposes a PLL independent frequency estimation approach for the second-order generalized integrator (SOGI) using the simplified teager energy operator. The proposed enhanced frequency-adaptive SOGI is further used to estimate the amplitude and phase-angle of the grid voltage. The simplified teager energy operator-based frequency estimation requires only three consecutive samples of the normalized grid voltage signal. It is independent of the PLL gain tuning issues.

The grid synchronization performance improvement of the proposed technique is compared with both the PLL techniques and the frequency feedforward technique using simulation and experimental analysis. It is observed that the proposed technique provides robust transient disturbance rejection capability (i.e., lesser settling time and overshoot) in comparison to the PLL based techniques. Moreover, it provides immunity to the steady-state disturbance such as DC offset. Additionally, its grid voltage harmonics rejection capability can be controlled by fine tuning the gain of the SOGI. It does not contain any additional band pass filter and any trigonometric functions during the synchronization. Hence it is computationally efficient in comparison to the frequency feedforward technique.

APPENDIX

The proportional and integral gain (K_{PPLL} and K_{IPLL}) for the PLL based grid synchronization techniques are designed based on the closed-loop transfer function as given by

$$\frac{\theta_{PLL}}{\theta_g} = \frac{K_{PPLL}s + K_{IPLL}}{s^2 + K_{PPLL}s + K_{IPLL}} \tag{18}$$

where θ_{PLL} is the estimated phase-angle by the PLL and θ_g is the actual grid voltage phase-angle. $\Delta\theta$ $(= \theta_g - \theta_{PLL})$ is considered as the linearized approximation of the q-axis component of grid voltage ($V_q = \sin(\Delta\theta) \approx \Delta\theta$). From the settling time (t_s), bandwidth (ω_{bw}) and damping ratio (ζ), the gain parameters (K_{PPLL} and K_{IPLL}) are calculated as given by

$$K_{PPLL} = 2\zeta\omega_{bw} = \frac{9.2}{t_s}, K_{IPLL} = {\omega_{bw}}^2 = \frac{4.6^2}{(\zeta t_s)^2} \tag{19}$$

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