Comparison of a 100-pF Capacitor With a 12 906-Ω Resistor Using a Digital Impedance Bridge

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***Abstract*— We tested a digital impedance bridge in a hybrid structure for comparison of a capacitor with a resistor where the impedance ratio was measured in two separate parts. The modulus of the impedance ratio was matched arbitrarily close to the input-to-output ratio, in magnitude, of a two-stage inductive voltage divider by adjusting the operating frequency of the bridge; the residual deviation between the two together with the phase factor of the impedance ratio was measured using a custom detection system based on a four-channel 24-bit digitizer. The ratio of the inductive voltage divider was calibrated, *in situ*, using a conventional four-arm bridge with two known capacitors. Fluctuations of the source voltages were largely removed through postprocessing of the digitized data, and the measurement results were limited by the digitizer error. We have achieved an overall bridge resolution and stability of 0.02 μF/F in 2 h for measuring a 100-pF capacitor relative to a 12 906-Ω resistor at 1233 Hz. The relative combined standard uncertainty ($k = 1$) is 0.13 μF/F, dominated by the digitizer error.**

***Index Terms*— ac voltage ratio, digital bridge, impedance standard, lock-in detector, noise cancellation.**

I. Introduction

DIGITAL techniques can be readily used to generate two synchronized ac voltages with a phase difference of $\pi/2$. The digital bridges, based on such ac sources, have the potential to greatly simplify comparisons between a capacitor and a resistor. Precise measurements of such impedance ratios are critical to developing quantum-based impedance standards. The present status of the digital bridges as compared with the traditional transformer-based impedance bridges has been recently reviewed [1]. The latter still provides measurements with the highest accuracy for the most demanding applications, including the realization of the capacitance unit from calculable capacitors or the ac quantized Hall resistance (QHR) through a quadrature bridge [2]–[4]. However, the digital bridges have been noticeably improving for impedance comparisons, offering many advantages through computer control and automation [5]–[11]. In particular, Josephson arbitrary waveform synthesizers establish a quantum-based voltage ratio standard that can be used for impedance comparisons at any phase angle [5], [6]. Digital signal sources custom-designed for impedance bridges have also shown great promise. A dual-channel ac voltage source with amplitude ratio stability better than 0.01 μV/V and a phase resolution of 0.2 μrad at 1 kHz has been reported [10]. A fully-digital four-terminal-pair (4TP) bridge, using such a custom-designed voltage ratio source for reference, has been reported for *RC* comparisons with a 1:1 magnitude ratio with a combined uncertainty of 9.2×10^{-8}, showing great promise for the realization of the unit of capacitance from an ac QHR standard [11]. Another interesting approach [12] is to use commercial synthesizers that are then stabilized with a negative feedback loop, minimizing the bridge error signal.

When the voltage ratio of two synthesized sources is used directly as the reference for impedance ratio measurements, as described in the literature [5]–[11], the stability of the voltage ratio can become a major limiting factor for the overall bridge performance. It appears that an underexplored research area is to mimic in the digital domains some analog techniques that are commonly used in the analog bridges to correlate and combine detector voltages, enabling suppression of the effect of source fluctuations. Let us consider the Quad bridge [2], [3], shown in Fig. 1, as an example. The complex impedance ratio of a resistor and a capacitor, with a phase of $\pi/2$, cannot be measured with high accuracy with a single quadrature bridge because the required voltage ratio at a phase angle of $\pi/2$ cannot be accurately produced in an analog bridge. However, two such ratios in sequence, forming a double quadrature bridge with a total phase shift of π, can be measured with high accuracy using a transformer ratio as reference. It is important to observe that although the overall accuracy of a Quad bridge can be very high, the error voltages of the individual quadrature bridges at points A and B (see Fig. 1) fluctuate significantly due to the inevitable fluctuation of the quadrature voltage represented by δV. An elegant feature of the Quad bridge is to combine the error voltages with an *RC* combining network such that it forms, with the main bridge components, a twin-T network from the quadrature voltage to the detector, D; the twin-T network is a notch filter and can be adjusted so that D is immune to δV at the fundamental frequency of the bridge excitation.

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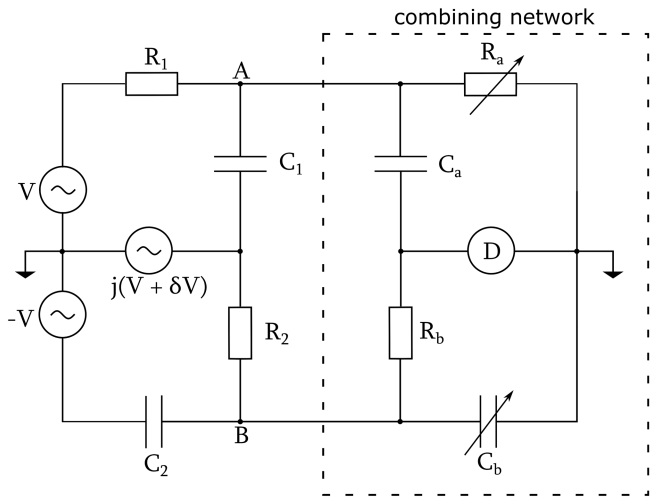

Fig. 1. Schematic of Quad bridge with combining network.

The Quad bridge can be simplified using digital techniques. Specifically, if the detector voltages at points A and B (see Fig. 1) are digitized, their correlation can be analyzed in post-processing and the function of the analog combining network can be replaced by software algorithms. One can further argue that if the detector voltage of a single quadrature bridge is synchronously digitized with the source voltages, their correlation can also be analyzed to suppress the source fluctuations. This article describes our research in this direction, aiming to develop a simple digital bridge for *RC* comparisons.

II. Bridge Setup

The digital impedance bridge, shown in Fig. 2, is designed for comparisons between a 4TP Vishay[1] resistor, with a nominal value of $R_H = 12\ 906\ \Omega$, in an air bath at 23 °C, and a two-terminal-pair (2TP) Andeen–Hagerling capacitor, with a nominal value of $C = 100$ pF. The impedance of the capacitor and the resistor are represented with $Z_1 = (1/j\omega C)$ and $Z_2 = R_H$, respectively, and the associated impedance ratio is represented by a complex number, $re^{j\theta} = (Z_1/Z_2)$. The low port of the 2TP capacitor was connected directly to the low-current port of the resistor without a combining network by following a method described by Small *et al.* [14] to compare 4TP resistors with 2TP capacitors. A current amplifier (Femto DLPCA-200) with transimpedance of Z_3, which is used to detect the bridge error voltage, was connected to the low-potential port of the 4TP resistor. Hence, the cable and the contact resistance between the low-current port of the resistor and the low port of the 2TP capacitor were then considered part of the capacitance standard. As long as the defining planes are applied consistently in calibrations, the inclusion of contact resistance only affects the dissipation factor of the capacitor slightly, with a negligible contribution to the uncertainty of the capacitance measurements.

We used two phase-locked channels (S_1 and S_2) of a Keysight 33500B waveform generator as the main sources

[1]Certain commercial equipment, instruments, or materials are identified in this article to foster understanding. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the materials or equipment identified are necessarily the best available for the purpose.

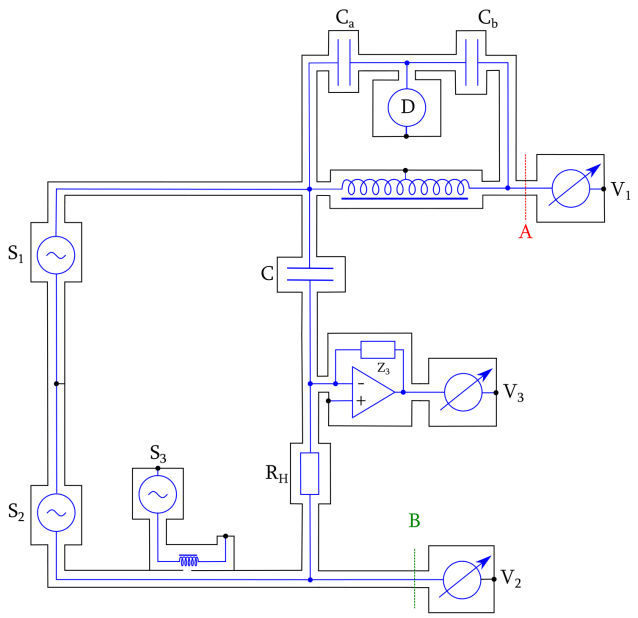

Fig. 2. Schematic of digital impedance bridge for comparison of $Z_1 = (j\omega C)^{-1}$ with $Z_2 = R_H$ ($C = 100$ pF and $R_H = 12\ 906\ \Omega$) at a frequency near 1233 Hz. Z_3 is the feedback resistor of the current amplifier. S_1 (amplitude = 10 V, phase = 90°), S_2 (amplitude = 0.1 V, phase = 0), and S_3 are waveform generators. V_1, V_2, and V_3 are ac voltmeters. V_1 (amplitude = 0.1 V, phase = −90°) and V_2 (nominally, amplitude = 0.1 V, phase = 0) are connected to the high-potential ports (A and B) and are periodically switched to minimize the effect of their gain drift. S_3 is adjusted such that V_3 is nominally 0. Coaxial chokes (omitted for clarity) are placed in every unwanted loop in the bridge circuit [13].

to excite the bridge through a 2TP current loop connecting to the high-current ports of Z_1 and Z_2, applying root mean square (rms) voltages of 7.07 V and 70.7 mV, respectively, to the capacitor and the resistor at a frequency near 1233 Hz. To overcome the limited resolutions of the generator outputs, another synchronized 33500B generator (S_3) was used to inject a fine adjustment signal through a 10 000:1 injection transformer inserted into the lower excitation arm. An external time base was used for both generators with their 10-MHz reference signal locked to the Global Positioning System.

The modulus of the nominal impedance ratio is 100. To avoid the digitizer nonlinearity of sampling the excitation voltages with different amplitudes, a two-stage inductive voltage divider (IVD), with its input-to-output ratio, k_o, having a nominal value of −100, was added between the high port of the capacitor and the voltage measurement system. The operating frequency of the bridge was fine-tuned such that the modulus of the impedance ratio, r, was arbitrarily close to k_o in magnitude and the sampled V_1 and V_2 were nominally equal in amplitude. The IVD ratio may slightly depend on the loading condition and therefore was calibrated, *in situ*, using a conventional four-arm bridge with two capacitors, C_a and C_b, of nominal values of 1 and 100 pF, respectively. A small micrometer-controlled trim capacitor added in parallel to C_b was used to null the in-phase component of the bridge error.

The IVD output (A) and the low-potential port (B) of Z_2 form a 2TP potential loop of a digital bridge with two voltage detectors through a custom coaxial switching fixture, which was described previously [15]. The two detectors were periodically interchanged to minimize the effect of their gain drift.

A small loading change at A and B is equivalent to a small change of the excitation voltage ratio, which is suppressed in the digital domain by correlation with the bridge error signal.

We used a Keysight DAQM909A, a four-channel 24-bit digitizer module in a Keysight DAQ973A data acquisition system, to simultaneously sample V_1, V_2, and V_3, preserving the relative phase difference of the three signals. The digitizer was set with differential input, a sampling rate of 800 000 samples/s, and a record length of 2 400 000 samples for each measurement. The analog bandwidth of the digitizer is approximately 125 kHz. The amplitude and the phase of each sampled voltage were determined using an algorithm of three-parameter least-squares fit as described in IEEE Standard 1057-2017 [16].

The digital bridge (see Fig. 2) relies on accurate measurements of voltage ratios to determine the phase factor of the impedance ratio, $e^{j\theta}$. In the ideal case, the excitation sources would be adjusted to balance the bridge, such that for any measured voltage, V_2, at the high-potential port of Z_2, the measured voltage, V_1, which is scaled down by the IVD from the high-potential port of Z_1, would be equal to a perfect value V_{1p}, achieving the condition of equal current through the two impedances under comparison. The balanced equation is

$$\frac{Z_1}{Z_2} = -\frac{k_o V_{1p}}{V_2}. \tag{1}$$

In practice, the balance is never perfect, and the source drift always exists. The combined effect can be represented by an error voltage, δV, superimposed on the ideal voltage V_{1p}, and we have $V_1 = V_{1p} + \delta V$. The effect of the error voltage is automatically balanced through the feedback resistor Z_3 of the current amplifier. The common low-potential port is kept at virtual ground, and the detected error voltage, V_3, relates to δV through

$$\frac{Z_1}{Z_3} = -\frac{k_o \delta V}{V_3}. \tag{2}$$

The phase difference between V_3 and δV is approximately 90°. We define the gain factor $g = (j/k_o)(Z_1/Z_3)$. Hence, $j\delta V + gV_3 = 0$. The bridge dynamics can be understood as a superposition of the two voltage-balancing actions governed by (1) and (2).

III. Test Results and Discussions

A. Equal Voltage Test

The measurement accuracy of the DAQM909A for ac voltage ratios depends on not only the resolution of the digitizer but also the gain stability of the input amplifiers. To determine the limitations of the digitizer, we connected two input channels of a DAQM909A in parallel to the same sinewave voltage, with an rms value of 0.1 V at 1 kHz, similar to the tests described in the previous article [15] when the two SR860 lock-in detectors were used to measure large ac signals. The best results were obtained when the two input channels, set at the 0.3-V input range, were periodically interchanged through the coaxial switching fixture, creating two virtually identical digitizing channels. The Allan deviation of the measured unity voltage ratio as a function of the averaging time follows a straight line in a log-log plot, with its slope consistent with averaging over white noise. It reaches below 0.01 μV/V in approximately 4 h, about a factor of 10 lower than what was achieved using the SR860s.

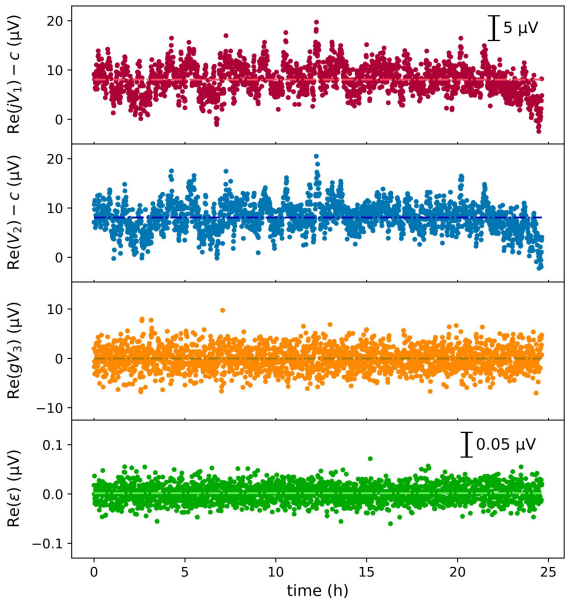

Fig. 3. Real components of recorded voltages as a function of time: 1) jV_1; 2) V_2; 3) V_3 scaled with the gain factor; and 4) ε. jV_1 and V_2 are shifted by $c = 10^5$ μV.

B. Digitized Bridge Voltage

A major advantage of the digital bridge is that the excitation voltages and the error signal can be fully digitized, and the bridge dynamics can be analyzed in postprocessing. All the test results presented herein were acquired with the bridge setup shown in Fig. 2. The gain of the transimpedance amplifier was set at 10^7 V/A, and the corresponding Z_3 was approximately 10 MΩ; the 3-dB bandwidth at this setting is 50 kHz. Figs. 3 and 4 show the measured V_1, V_2, V_3 values, and the bridge error voltage, ε, as a function of time that were acquired with S_1 and S_2 set at 1233.19734 Hz, a phase of 90° and 0°, and an amplitude of 10 and 0.1 V, respectively. The complex amplitude of S_3 set at the same frequency was automatically controlled through a computer to minimize the mean bridge error (V_3), using a simple proportional-integral feedback algorithm.

The phase difference between V_1 and V_2 is approximately −90°. The digitized voltages are phase normalized such that the phase of V_2 is 0. Their complex components are more conveniently compared between jV_1 and V_2. The real parts of jV_1 and V_2 (see Fig. 3) fluctuated, on the order of 10 μV, exceeding a factor of 10 more than the imaginary counterparts (see Fig. 4). This reflects that the digital sources have better phase stabilities than amplitude stabilities. The real component of V_2 closely follows that of jV_1, resulting from the feedback action that minimizes the bridge error signal.

For better comparison, the error voltage V_3 is shown after being scaled with an estimated gain factor. Re(gV_3) is dominated by white noise, and its mean is effectively locked

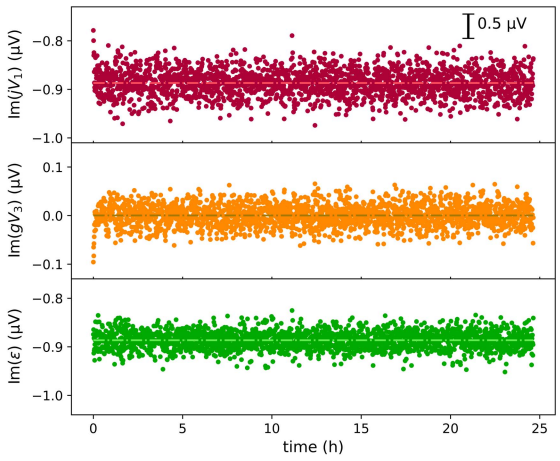

Fig. 4. Imaginary components of recorded voltages as function of time: 1) jV_1; 2) V_3 scaled with the gain factor; and (3) ε.

to 0 through the feedback (see Fig. 3). The fluctuations of $\mathrm{Im}(gV_3)$ form a mirror image of $\mathrm{Im}(jV_1)$, with its mean also locked to 0 (see Fig. 4).

We can qualitatively understand how the detected error voltage V_3 relates to the source fluctuation δV by considering that the transimpedance amplifier together with Z_1 and Z_2 form a summing amplifier. Since Z_1/k_o and Z_2 are nominally equal in magnitude and differ by 90° in phase, we have $V_1 + jV_2 \approx -\delta V$.

We define

$$\varepsilon = j\delta V + gV_3. \tag{3}$$

The real and imaginary components of ε are shown in Figs. 3 and 4, respectively. Both components follow a white noise distribution, with a standard deviation of less than 0.05 μV, indicating a strong correlation between δV and gV_3.

C. Correlation Analysis and Noise Cancellation

To analyze the dynamics of the bridge balancing more rigorously, we applied Kirchhoff's law to the bridge circuit

$$\frac{k_o V_1}{Z_1} + \frac{V_2}{Z_2} + \frac{V_3}{Z_3} = 0. \tag{4}$$

Using conventional notations, we define α and β as the real and imaginary part of the deviation, respectively, from the nominal impedance ratio that is perfectly matched to the IVD ratio in magnitude

$$\frac{Z_1}{Z_2} = \lambda(1 + \alpha + j\beta) \tag{5}$$

where $\lambda = jk_o$.

Combining (4) and (5), we rewrite

$$1 - \frac{jV_1}{V_2} = -\alpha - j\beta - \frac{1}{\lambda}\frac{Z_1}{Z_3}\frac{V_3}{V_2}. \tag{6}$$

We define

$$u = 1 - \frac{jV_1}{V_2} \tag{7}$$

$$v = \frac{V_3}{V_2}. \tag{8}$$

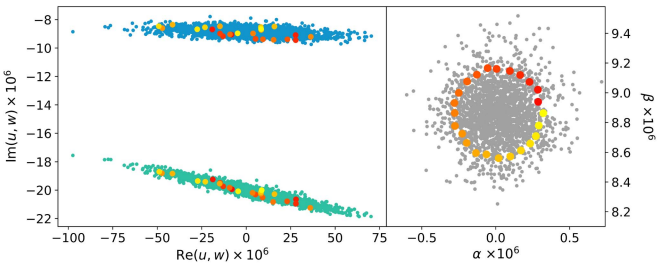

Fig. 5. (a) Imaginary part versus real part: u in light blue and w in cyan. w shifted lower by $j20 \times 10^{-6}$ for clarity. (b) β versus α. 24 data points of the fitting residuals distributed close to the perimeter of a circle are colored progressively in (b); the corresponding u and w points in (a) show their correlation.

Equation (6) becomes

$$u = -\alpha - j\beta + gv. \tag{9}$$

Using a linear fitting between the complex variables u and v, we can determine g. We then have

$$\alpha = \mathrm{Re}(gv - u) \tag{10}$$

$$\beta = \mathrm{Im}(gv - u). \tag{11}$$

To visualize the effectiveness of the linear fitting, we plot the imaginary part versus the real part for u and $w = |g|v$ in Fig. 5(a). The natural fluctuation of u is mainly along the real axis, covering a range of about 150 μV/V, reflecting that the digital sources have better phase stabilities than amplitude stabilities. The pattern of w is similar to that of u, except that it is tilted due to a phase shift of the current amplifier. The residuals of the linear fitting can be seen in Fig. 5(b), showing α versus β. The residual data points distribute tightly in a circle of radius about 0.5 μV/V, indicating that the fluctuations of u and v largely cancel out in determining α and β.

Fig. 6 shows α as a function of time over a period of 24 h. The distribution of the data points is consistent with a constant that is buried in white noise. Each data point in the lower panel takes about 36 s to acquire, and all the data points stay within $\pm 0.7 \times 10^{-6}$. Averaging 256 points, or about 2 h worth of data, produces a new set of averaged data that fluctuates within $\pm 0.02 \times 10^{-6}$ about their mean. The fluctuations can be attributed predominantly to the limited resolution of the digitizer.

Fig. 7 shows β as a function of time over the same period. The distribution of the data points of β are similar to α and also consistent with a constant value over time. All the data points stay within $\pm 0.7 \times 10^{-6}$. Averaging 256 points also produces a new set of averaged data that fluctuates within $\pm 0.02 \times 10^{-6}$ about their mean.

The Allan deviations of α and β are shown in Fig. 8. Both decrease to 2×10^{-8} level in about 3 h and show a monotonic downward trend over the test time window, demonstrating the stability of the digital bridge.

D. Results and Uncertainty Analysis

The digital impedance bridge enables us to measure the capacitance of C in reference to R_H with a Type A uncertainty ($k = 1$) of 0.02 μF/F. Repeated measurements show that the

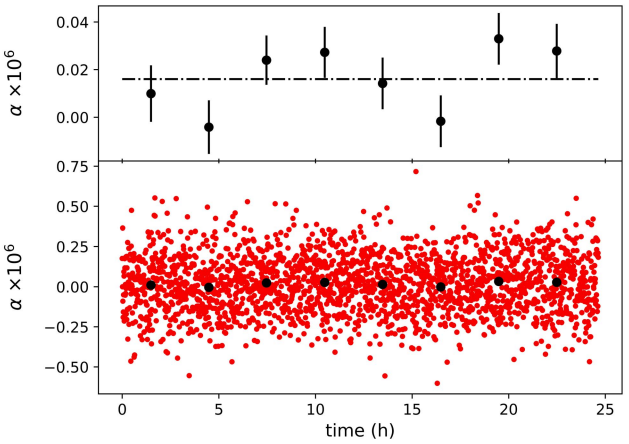

Fig. 6. Determined α as a function of time. The black dots were obtained by averaging 256 points, or about 2 h worth of data. The error bars in the top graph denote the 1-σ standard deviation of the 256 points.

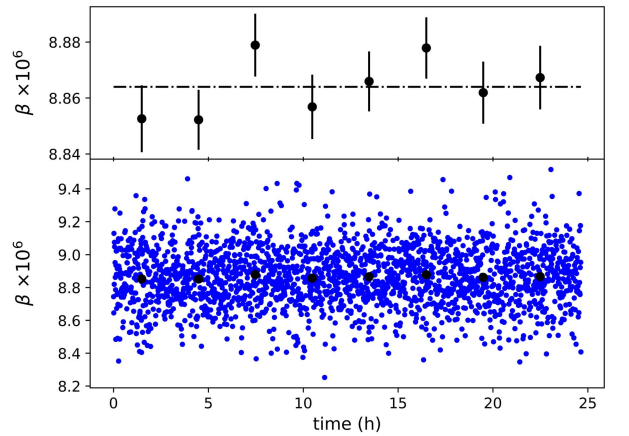

Fig. 7. Determined β as a function of time. The black dots were obtained by averaging 256 points, or about 2 h worth of data. The error bars in top graph denote the 1-σ standard deviation of the 256 points.

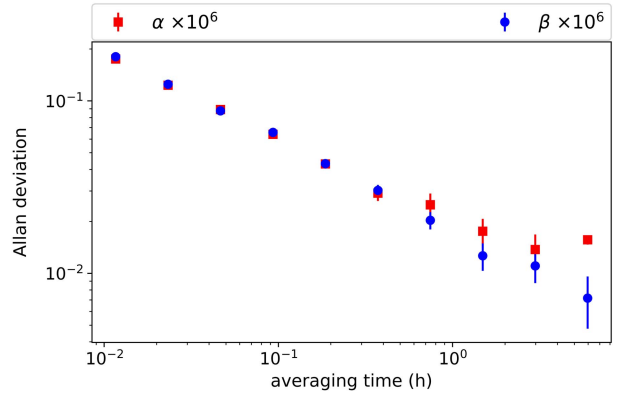

Fig. 8. Squares and circles are the real and imaginary parts of the deviation from the nominal impedance ratio. Error bars are 1-σ standard deviation of the Allan deviation.

results of C using the digital bridge are consistent, within 0.11 μF/F, with its capacitance measured against the Farad Bank, which is used to maintain the capacitance unit at the National Institute of Standards and Technology (NIST), Gaithersburg, MD, USA, and is traceable to the calculable capacitor [17]. The difference can be partly attributed to the frequency dependence of C because the digital bridge functions near 1233 Hz to keep the impedance ratio close to 100:1 in magnitude while the capacitance measurement relative to the Farad Bank has been restricted to 1592 Hz. However, the largest uncertainty source for the digital bridge is the digitizer error as shown in Table I.

TABLE I
UNCERTAINTY BUDGET ($k = 1$)

	Relative standard uncertainty ($\times 10^{-6}$)
Type A	0.02
Digitizer error	0.10
Frequency dependence of C_a (1 pF) and C_b (100 pF)	0.07
C_a and C_b relative to Farad Bank	0.03
R_H relative to dc QHR	0.01
Frequency dependence of R_H	0.01
Relative combined standard uncertainty	0.13

The digital errors associated with the digitizer may arise from aliasing and spectral leakage. Stray capacitances in the digitizer may also cause crosstalk between the ADC channels and leakage to the ground. These errors have been estimated experimentally and numerically by varying the sampling rate and the record length, combined with temporarily introducing extra cross capacitances and changing from the differential input mode to the single-ended mode. Sensitivity to harmonics has been estimated experimentally and numerically by including selected harmonic base functions in the sine fit, adding simulated harmonic content to the digitized data record before the sine fit, and physically injecting additional third harmonic voltage into the bridge excitation. Possible offset error in the detected V_3 due to non-linearity of the current amplifier and the ADC, causing intermodulation distortion, was also accessed by changing the gain settings of the amplifier and the ADC; no correlated change was detected within the limit of the bridge resolution.

In the future, we plan to modify the front analog circuit of the digitizer to reduce its error. The uncertainty for the frequency dependence determination, which has currently been limited by the stability of a reference 1-pF cross capacitor at NIST, can also be significantly reduced [17], [18].

IV. CONCLUSION

We evaluated a digital impedance bridge in a hybrid structure for comparison of a capacitor with a resistor where the impedance ratio was measured in two separate parts. The modulus of the impedance ratio was matched arbitrarily close to the input-to-output ratio, in magnitude, of a two-stage IVD by adjusting the operating frequency of the bridge; the residual deviation between the two together with the phase factor of the impedance ratio was measured using a custom detection system based on a four-channel 24-bit digitizer. The IVD was calibrated, *in situ*, using a four-arm bridge with two

known capacitors. In contrast to the conventional approach of emphasizing precision and stability of the voltage sources driving the bridge, we adopted an approach that focused on the resolution and stability of the detectors. Fluctuations of the source voltages were largely removed through postprocessing of the digitized data, and the measurement results were limited by the digitizer error. While we have achieved a low Type A uncertainty ($k = 1$) of 0.02 μF/F in 2 h for determining the capacitance of a 100-pF capacitor relative to a 12 906-Ω resistor at 1233 Hz, the combined relative standard uncertainty ($k = 1$) is 0.13 μF/F. Even though the uncertainty is not as low as for a conventional IVD-based double-quadrature bridge which has the modulus of the nominal impedance ratio equal to one, the digital bridge discussed here has a key advantage. The modulus of the nominal impedance ratio of the digital bridge is 100. This approach has the advantage of shortening the measurement chain from a 12 906-Ω resistor to a 100-pF capacitor by two 10:1 ratio steps. In the future, we plan to focus our research on reducing the digitizer error for the digital impedance bridge to serve as an alternative system at NIST for realizing the capacitance unit.

The detection system based on the DAQM909A for measuring ac voltage ratios compares favorably to the system based on the SR860 lock-in detectors which we evaluated previously [15]. We achieved a factor of 10 improvement in terms of the Allan deviations for the impedance ratio measurements over a comparable averaging window. We can attribute the improvement to the higher resolution of the modern data acquisition board and the customized demodulation method in post-processing, which is not accessible with the commercial lock-in detectors.

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