# Verifying Sequential Consistency on Shared-Memory Multiprocessors by Model Checking

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#### Abstract

The memory model of a shared-memory multiprocessor is a contract between the designer and programmer of the multiprocessor. The sequential consistency memory model specifies a total order among the memory (read and write) events performed at each processor. A trace of a memory system satisfies sequential consistency if there exists a total order of all memory events in the trace that is both consistent with the total order at each processor and has the property that every read event to a location returns the value of the last write to that location.

Descriptions of shared-memory systems are typically parameterized by the number of processors, the number of memory locations, and the number of data values. It has been shown that even for finite parameter values, verifying sequential consistency on general shared-memory systems is undecidable. We observe that, in practice, shared-memory systems satisfy the properties of causality and data independence. Causality is the property that values of read events flow from values of write events. Data independence is the property that all traces can be generated by renaming data values from traces where the written values are distinct from each other. If a causal and data independent system also has the property that the logical order of write events to each location is identical to their temporal order, then sequential consistency can be verified algorithmically. Specifically, we present a model checking algorithm to verify sequential consistency on such systems for a finite number of processors and memory locations and an arbitrary number of data values.

### 1 Introduction

Shared-memory multiprocessors are very complex computer systems. Multithreaded programs running on shared-memory multiprocessors use an abstract view of the shared memory that is specified by a memory model. Examples of memory models for multiprocessors include sequential consistency [Lam79], partial store ordering [WG99], and the Alpha memory model [Com98]. The implementation of the memory model, achieved by a protocol running either in hardware or software, is one of the most complex aspects of multiprocessor design. These protocols are commonly referred to as cache-coherence protocols. Since parallel programs running on such systems rely on the memory model for their correctness, it is important to implement the protocols correctly. However, since efficiency is important for the commercial viability of these systems, the protocols are heavily optimized, making them prone to design errors. Formal verification of cache-coherence protocols can detect these errors effectively.

Descriptions of cache-coherence protocols are typically parameterized by the number of processors, the number of memory locations, and the number of data values. Verifying parameterized systems for arbitrary values of these parameters is undecidable for nontrivial systems. Interactive theorem proving is one approach to parameterized verification. This approach is not automated and is typically expensive in terms of the required human effort. Another approach is to model check a parameterized system for small values of the parameters. This is a good debugging technique that can find a number of errors prior to the more time-consuming effort of verification for arbitrary parameter values. In this paper, we present an automatic method based on model checking to verify that a cache-coherence protocol with fixed parameter values is correct with respect to the sequential consistency memory model.

The sequential consistency memory model [Lam79] specifies a total order among the memory events (reads and writes) performed locally at each processor. This total order at a processor is the order in which memory events occur at that processor. A trace of a memory system satisfies sequential consistency if there exists a total order of all memory events that is both consistent with the local total order at each processor, and has the property that every read to a location returns the latest (according to the total order) value written to that location. Surprisingly, verifying sequential consistency, even for fixed parameter values, is undecidable [AMP96]. Intuitively, this is because the witness total order could be quite different from the global temporal order of events for some systems. An event might need to be logically ordered after an event that occurs much later in a run. Hence any algorithm needs to keep track of a potentially unbounded history of a run.

In this paper, we consider the problem of verifying that a shared-memory system S(n, m, v) with n processors, m locations and v data values is sequentially consistent. We present a method that can check sequential consistency for any fixed n and m and for arbitrary v. The correctness of our method depends on two assumptions —causality and data independence. The property of causality arises from the observation that protocols do not conjure up data values; data is injected into the system by the initial values stored in the memory and by the writes performed by the processors. Therefore every read operation r to location l is associated with either the initial value of l or some write operation v to l that wrote the value read by v. The property of data independence arises

from the observation that protocols do not examine data values; they just forward the data from one component of the system (cache or memory) to another. Since protocol behavior is not affected by the data values, we can restrict our attention, without loss of generality, to unambiguous runs in which the written data values to a location are distinct from each other and from the initial value. We have observed that these two assumptions are true of shared-memory systems that occur in practice [LLG<sup>+</sup>90, KOH<sup>+</sup>94, BDH<sup>+</sup>99, BGM<sup>+</sup>00].

For a causal and unambiguous run, we can deduce the association between a read and the associated write just by looking at their data values. This leads to a vast simplification in the task of specifying the witness total order for sequential consistency. It suffices to specify for each location, a total order on the writes to that location. By virtue of the association of write events and read events, the total order on the write events can be extended to a partial order on all memory events (both reads and writes) to that location. If a read event r reads the value written by the write event w, the partial order puts r after w and all write events preceding w, and before all write events succeeding w. As described before, sequential consistency specifies a total order on the memory events for each processor. Thus, there are n total orders, one for each processor, and m partial orders, one for each location, imposed on the graph of memory events of a run. A necessary and sufficient condition for the run to be sequentially consistent is that this graph is acyclic. We further show that existence of a cycle in this graph implies the existence of a nice cycle in which no two processor edges (imposed by the memory model) are for the same processor and no two location edges (imposed by the write order) are for the same location. This implies that a nice cycle can have at most  $2 \times min(\{n, m\})$ edges; we call a nice cycle with  $2 \times k$  edges a k-nice cycle. Further if the memory system is symmetric with respect to processor and location ids, then processor and location edges occur in a certain canonical order in the nice cycle. These two observations drastically reduce the number of cycles for any search.

We finally argue that a number of causal and data independent shared-memory systems occurring in practice also have the property that the witness write order at each location is simply the temporal order of the write events. In other words, a write event w is ordered before w' if w occurs before w'. We call this a simple write order, and it is in fact the correct witness for a number of shared-memory systems. For cache-based shared-memory systems, the intuitive explanation is that at any time there is at most one cache with write privilege to a location. The write privilege moves from one cache to another with time. Hence, the logical timestamps [Lam78] of the writes to a location order them exactly according to their global temporal order. We show that the proof that a simple write order is a correct witness for a memory system can be performed by model checking [CE81, QS81]. Specifically, the proof for the memory system S(n, m, v) for fixed n and m and arbitrary v is broken into  $min(\{n, m\})$  model checking lemmas, where the k-th lemma checks for the existence of canonical k-nice cycles.

The rest of the paper is organized as follows. Sections 2 and 3 formalize shared-memory systems and our assumptions of causality and data indepen-

dence about them. Section 4 defines the sequential consistency memory model. Section 5 defines the notions of a witness and a constraint graph for an unambiguous and causal run. Section 6 and 7 show that it is sufficient to search for canonical nice cycles in the constraint graph. Section 8 shows how to use model checking to detect canonical nice cycles in the constraint graphs of the runs of a memory system. Finally, we discuss related work in Section 9 and conclude in Section 10.

### 2 Shared-memory systems

Let  $\mathbb{N}$  denote the set of positive integers and  $\mathbb{W}$  denote the set of non-negative integers. For any  $n \geq 1$ , let  $\mathbb{N}_n$  denote the set of positive integers up to n and  $\mathbb{W}_n$  denote the set of non-negative integers up to n.

A memory system is parameterized by the number of processors, the number of memory locations, and the number of data values. The value 0 is used to model the initial value of all memory locations. In a memory system with n processors, m memory locations, and v data values, read and write events denoted by R and W can occur at any processor in  $\mathbb{N}_n$ , to any location in  $\mathbb{N}_m$ , and have any data value in  $\mathbb{W}_v$  (the data values in  $\mathbb{N}_v$  together with the initial value 0). Formally, we define the following sets of events parameterized by the number of processors n, the number of locations m, and the number of data values v, where  $n, m, v \geq 1$ .

- 1.  $E^r(n, m, v) = \{R\} \times \mathbb{N}_n \times \mathbb{N}_m \times \mathbb{W}_v$  is the set of read events.
- 2.  $E^w(n, m, v) = \{W\} \times \mathbb{N}_n \times \mathbb{N}_m \times \mathbb{W}_v \text{ is the set of } write \text{ events.}$
- 3.  $E(n,m,v)=E^r(n,m,v)\cup E^w(n,m,v)$  is the set of memory events.
- 4.  $E^a(n,m,v) \supseteq E(n,m,v)$  is the set of all events.
- 5.  $E^a(n, m, v) \setminus E(n, m, v)$  is the set of internal events.

The set of all finite sequences of events in  $E^a(n, m, v)$  is denoted by  $E^a(n, m, v)^*$ . A memory system S(n, m, v) is a regular subset of  $E^a(n, m, v)^*$ . A sequence  $\sigma \in S(n, m, v)$  is said to be a run. We denote by S(n, m) the union  $\bigcup_{v>1} S(n, m, v)$ .

Consider any  $\sigma \in E^a(n, m, v)^*$ . We denote the length of  $\sigma$  by  $\lceil \sigma \rceil$  and write  $\sigma(i)$  for the i-th element of the sequence. The set of indices of the memory events in  $\sigma$  is denoted by  $dom(\sigma) = \{1 \le k \le |\sigma| \mid \sigma(k) \in E(n, m, v)\}$ . For every memory event  $e = \langle a, b, c, d \rangle \in E(n, m, v)$ , we define op(e) = a, proc(e) = b, loc(e) = c, and data(e) = d. The set of memory events by processor i for all  $1 \le i \le n$  is denoted by  $P(\sigma, i) = \{k \in dom(\sigma) \mid proc(\sigma(k)) = i\}$ . The set of memory events to location i for all  $1 \le i \le m$  is denoted by  $L(\sigma, i) = \{k \in dom(\sigma) \mid loc(\sigma(k)) = i\}$ . For all  $1 \le i \le m$ , the set of write events to location i is denoted by  $L^w(\sigma, i) = \{k \in L(\sigma, i) \mid op(\sigma(k)) = W\}$ , and the set of read events to location i is denoted by  $L^r(\sigma, i) = \{k \in L(\sigma, i) \mid op(\sigma(k)) = R\}$ .

```
typedef Msg \{m : \{ACKS, ACKX\}, a : \mathbb{N}_m, d : \mathbb{W}_v\} \cup \{m : \{INVAL\}, a : \mathbb{N}_m\};
typedef CacheEntry \{d: \mathbb{W}_v, s: \{INV, SHD, EXC\}\};
cache: array \mathbb{N}_n of array \mathbb{N}_m of CacheEntry;
inQ: array \mathbb{N}_n \ of \ Queue(Msg);
owner: array \mathbb{N}_m of \mathbb{W}_n;
Initial predicate
\forall i \in \mathbb{N}_n, j \in \mathbb{N}_m : (cache[i][j] = \langle 0, SHD \rangle \land inQ[i].isEmpty \land owner[j] \neq 0)
Events
\langle R, i, j, k \rangle
                   cache[i][j].s \neq INV \land cache[i][j].d = k \rightarrow
\langle W, i, j, k \rangle
                   cache[i][j].s = EXC \rightarrow
                       cache[i][j].d := k
\langle ACKX, i, j \rangle cache[i][j].s \neq EXC \land owner[j] \neq 0 \rightarrow
                       if owner[j] \neq i then cache[owner[j]][j].s := INV;
                       owner[j] := 0;
                       for each (p \in \mathbb{N}_n)
                            if (p = i) then
                                inQ[p] := append(inQ[p], \langle ACKX, j, cache[owner[j]][j].d\rangle)
                            else if (p \neq owner[j] \land cache[p][j].s \neq INV) then
                                inQ[p] := append(inQ[p], \langle INVAL, j \rangle)
\langle ACKS, i, j \rangle
                   cache[i][j].s = INV \land owner[j] \neq 0 \rightarrow
                       cache[owner[j]][j].s := SHD;
                       owner[j] := 0;
                       inQ[i] := append(inQ[i], \langle ACKS, j, cache[owner[j]][j].d\rangle);
\langle \mathit{UPD}, i \rangle
                   \neg isEmpty(inQ[i]) \rightarrow
                       let msg = head(inQ[i]) in
                            if (msg.m = INVAL) then
                                cache[i][msg.a].s := INV
                            else if (msg.m = ACKS) then {
                                cache[i][msg.a] := \langle SHD, msg.d \rangle;
                                owner[msg.a] := i
                            } else {
                                cache[i][msg.a] := \langle EXC, msg.d \rangle;
                                owner[msg.a] := i
                       inQ[i] := tail(inQ[i])
```

Figure 1: Example of memory system

The subsequence obtained by projecting  $\sigma$  onto  $dom(\sigma)$  is denoted by  $\overline{\sigma}$ . If  $\sigma \in S(n, m, v)$ , the sequence  $\overline{\sigma}$  is a trace of S(n, m, v). Similarly, if  $\sigma \in S(n, m)$ , the sequence  $\overline{\sigma}$  is a trace of S(n, m).

**Example.** Consider the memory system in Figure 1. It is a highly simplified model of the protocol used to maintain cache coherence within a single node in the Piranha chip multiprocessor system [BGM<sup>+</sup>00]. The system has three variables — cache, in Q and owner— and five events—the memory events  $\{R, W\}$  and the internal events  $\{ACKX, ACKS, UPD\}$ . The variables inQ and owner need some explanation. For each processor i, there is an input queue inQ[i] where incoming messages are put. The type of inQ[i] is Queue. The operations is Empty, head and tail are defined on Queue, and the operation append is defined on  $Queue \times Msg$ . They have the obvious meanings and their definitions have been omitted in the figure. For each memory location j, either owner[j] = 0 or owner[j] contains the index of a processor. Each event is associated with a guarded command. The memory events R and W are parameterized by three parameters —processor i, location j and data value k. The internal events ACKX and ACKS are parameterized by two parameters —processor i and location j. The internal event UPD is parameterized by processor i. A state is a valuation to the variables. An initial state is a state that satisfies the initial predicate. An event is *enabled* in a state if the guard of its guarded command is true in the state. The variables are initialized to an initial state and updated by nondeterministically choosing an enabled event and executing the guarded command corresponding to it. A run of the system is any finite sequence of events that can be executed starting from some initial state.

A processor i can perform a read to location j if  $cache[i][j].s \in \{SHD, EXC\}$ , otherwise it requests owner[j] for shared access to location j. The processor owner[j] is the last one to have received shared or exclusive access to location j. The request by i has been abstracted away but the response of owner[j] is modeled by the action ACKS[i][j], which sends a ACKS message containing the data in location j to i and temporarily sets owner[j] to 0. Similarly, processor i can perform a write to location j if cache[i][j].s = EXC, otherwise it requests owner[j] for exclusive access to location j. The processor owner[j] responds by sending a ACKX message to i and INVAL messages to all other processors that have a valid copy of location j. owner[j] is set to i when processor i reads the ACKS or ACKX message from inQ[i] in the event UPD[i]. Note that new requests for j are blocked while owner[j] = 0. A processor i that receives an INVAL message for location j sets cache[i][j].s to INV.

# 3 Causality and data independence

In this section, we will state our main assumptions on memory systems — causality and data independence.

We assume that the runs of memory systems are *causal*. That is, every read event to location m "reads" either the initial value of m or the value "written" to m by some write event. We believe that this assumption is reasonable because

memory systems do not conjure up data values; they just move around data values that were introduced by initial values or write events. We state the causality assumption formally as follows.

**Assumption 1 (Causality)** For all  $n, m, v \ge 1$ , for all traces  $\tau$  of S(n, m, v), and for all locations  $1 \le i \le m$ , if  $x \in L^r(\tau, i)$ , then either  $data(\tau(x)) = 0$  or there is  $y \in L^w(\tau, i)$  such that  $data(\tau(x)) = data(\tau(y))$ .

The memory system in Figure 1 is causal. Only the write event W introduces a fresh data value in the system by updating the cache; the internal events ACKS, ACKX and UPD move data around and the read event R reads the data present in the cache. Therefore, the data value of a read operation must either be the initial value 0 or the value introduced by a write event, thus satisfying Assumption 1.

Memory systems occurring in practice also have the property of data independence, that is, control decisions are oblivious to the data values. A cache line carries along with the actual program data a few state bits for recording whether it is in shared, exclusive or invalid mode. Typically, actions do not depend on the value of the data in the cache line. This can be observed, for example, in the memory system shown in Figure 1. Note that there are no predicates involving the data fields of the cache lines and the messages in any of the internal events of the system. In such systems, renaming the data values of a run results in yet another run of the system. Moreover, every run can be obtained by data value renaming from some run in which the initial value and values of write events to any location i are all distinct from each other. In order to define data independence formally, we define below the notion of an unambiguous run and the notion of data value renaming.

Formally, a run  $\sigma$  of S(n,m,v) is unambiguous if for all  $1 \leq i \leq m$  and  $x \in L^w(\sigma,i)$ , we have  $(1) \ data(\sigma(x)) \neq 0$ , and  $(2) \ data(\sigma(x)) \neq data(\sigma(y))$  for all  $y \in L^w(\sigma,i) \setminus \{x\}$ . In an unambiguous run, every write event to a location i has a value distinct from the initial value of i and the value of every other write to i. The trace  $\overline{\sigma}$  corresponding to an unambiguous run  $\sigma$  is called an  $unambiguous \ trace$ . If a run is both unambiguous and causal, each read event to location i with data value 0 reads the initial value of i, and each read event with a nonzero data value reads the value written by the unique write event with a matching data value. Thus, a read event can be paired with its source write event just by comparing data values.

A function  $\lambda: \mathbb{N}_m \times \mathbb{W} \to \mathbb{W}$  is called a renaming function if  $\lambda(j,0) = 0$  for all  $1 \leq j \leq m$ . Intuitively, the function  $\lambda$  provides for each memory location c and data value d the renamed data value  $\lambda(c,d)$ . Since 0 models the fixed initial value of all locations, the function  $\lambda$  does not rename the value 0. Let  $\lambda^d$  be a function on E(n,m,v) such that for all  $e = \langle a,b,c,d \rangle \in E(n,m)$ , we have  $\lambda^d(e) = \langle a,b,c,\lambda(c,d) \rangle$ . The function  $\lambda^d$  is extended to sequences in  $E(n,m,v)^*$  in the natural way.

We state the data independence assumption formally as follows.

Assumption 2 (Data independence) For all  $n, m, v \ge 1$  and sequences  $\tau \in E(n, m, v)^*$ , we have that  $\tau$  is a trace of S(n, m, v) iff there is an unambiguous trace  $\tau'$  of S(n, m) and a renaming function  $\lambda : \mathbb{N}_m \times \mathbb{W} \to \mathbb{W}_v$  such that  $\tau = \lambda^d(\tau')$ .

Assumptions 1 and 2 are motivated by the data handling in typical cache-coherence protocols. We can have these assumptions be true on protocol descriptions by imposing restrictions on the operations allowed on variables that contain data values [Nal99]. For example, one restriction can be that no data variable appears in the guard expression of an internal event or in the control expression of a conditional.

### 4 Sequential consistency

Suppose S(n, m, v) is a memory system for some  $n, m, v \ge 1$ . The sequential consistency memory model [Lam79] is a correctness requirement on the runs of S(n, m, v). In this section, we define sequential consistency formally.

We first define the simpler notion of a sequence being serial. For all  $\tau \in E(n, m, v)^*$  and  $1 \le i \le |\tau|$ , let  $upto(\tau, i)$  be the set  $\{1 \le k \le i \mid op(\tau(k)) = W \land loc(\tau(k)) = loc(\tau(i))\}$ . In other words, the set  $upto(\tau, i)$  is the set of write events in  $\tau$  to location  $loc(\tau(i))$  occurring not later than i. A sequence  $\tau \in E(n, m, v)^*$  is serial if for all  $1 \le u \le |\tau|$ , we have

$$data(\tau(u)) = 0, if upto(\tau, u) = \emptyset$$
  
$$data(\tau(u)) = data(\tau(max(upto(\tau, u)))), if upto(\tau, u) \neq \emptyset.$$

Thus, a sequence is serial if every read to a location i returns the value of the latest write to i if one exists, and the initial value 0 otherwise.<sup>1</sup>

The sequential consistency memory model M is a function that maps every sequence of memory events  $\tau \in E(n,m,v)^*$  and processor  $1 \leq i \leq n$  to a total order  $M(\tau,i)$  on  $P(\tau,i)$  defined as follows: for all  $u,v \in P(\tau,i)$ , we have  $\langle u,v \rangle \in M(\tau,i)$  iff u < v. A sequence  $\tau$  is sequentially consistent if there is a permutation f on  $\mathbb{N}_{|\tau|}$  such that the following conditions are satisfied.

```
C1 For all 1 \le u, v \le |\tau| and 1 \le i \le n, if \langle u, v \rangle \in M(\tau, i) then f(u) < f(v).
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C2 The sequence 
$$\tau' = \tau_{f^{-1}(1)} \tau_{f^{-1}(2)} \dots \tau_{f^{-1}(|\tau|)}$$
 is serial.

Intuitively, the sequence  $\tau'$  is a permutation of the sequence  $\tau$  such that the event at index u in  $\tau$  is moved to index f(u) in  $\tau'$ . According to C1, this permutation must respect the total order  $M(\tau,i)$  for all  $1 \leq i \leq n$ . According to C2, the permuted sequence must be serial. A run  $\sigma \in S(n,m,v)$  is sequentially consistent if  $\overline{\sigma}$  satisfies M. The memory system S(n,m,v) is sequentially consistent iff every run of S(n,m,v) is sequentially consistent.

<sup>&</sup>lt;sup>1</sup>The decision to model the initial values of all locations by the value 0 is implicit in our definition of a serial sequence.

The memory system in Figure 1 is supposed to be sequentially consistent. Here is an example of a sequentially consistent run  $\sigma$  of that memory system, the corresponding trace  $\tau$  of  $\sigma$ , and the sequence  $\tau'$  obtained by permuting  $\tau$ .

Sequential consistency orders the event  $\tau(2)$  before the event  $\tau(3)$  at processor 2. Let f be the permutation on  $\mathbb{N}_3$  defined by f(1) = 2, f(2) = 1, and f(3) = 3. The sequence  $\tau'$  is the permutation of  $\tau$  under f. It is easy to check that both conditions C1 and C2 mentioned above are satisfied.

In order to prove that a run of a memory system is sequentially consistent, one needs to provide a reordering of the memory events of the run. This reordering should be serial and should respect the total orders imposed by sequential consistency at each processor. Since the memory systems we consider in this paper are data independent, we only need to show sequential consistency for the unambiguous runs of the memory system. This reduction is stated formally in the following theorem.

**Theorem 4.1** For all  $n, m \ge 1$ , every trace of S(n, m) is sequentially consistent iff every unambiguous trace of S(n, m) is sequentially consistent.

**Proof**: The  $\Rightarrow$  case is trivial.

 $(\Leftarrow)$  Let  $\tau$  be a trace of S(n,m,v) for some  $v \geq 1$ . From Assumption 2 there is an unambiguous trace  $\tau'$  of S(n,m) and a renaming function  $\lambda: \mathbb{N}_m \times \mathbb{W} \to \mathbb{W}_v$  such that  $\tau = \lambda^d(\tau')$ . Since  $\tau'$  is sequentially consistent, we know that conditions C1 and C2 are satisfied by  $\tau'$ . It is not difficult to see that both conditions C1 and C2 are satisfied by  $\lambda^d(\tau')$  as well. Therefore  $\tau$  is sequentially consistent.

#### 5 Witness

Theorem 4.1 allows us to prove that a memory system S(n, m, v) is sequentially consistent by proving that all unambiguous runs in S(n, m) is sequentially consistent. In this section, we reduce the problem of checking sequential consistency on an unambiguous run to the problem of detecting a cycle in a constraint graph.

Consider a memory system S(n,m,v) for some fixed  $n,m,v\geq 1$ . A witness  $\Omega$  for S(n,m,v) maps every trace  $\tau$  of S(n,m,v) and location  $1\leq i\leq m$  to a total order  $\Omega(\tau,i)$  on the set of writes  $L^w(\tau,i)$  to location i. If the trace  $\tau$  is unambiguous, the total order  $\Omega(\tau,i)$  on the write events to location i can be extended to a partial order  $\Omega^e(\tau,i)$  on all memory events (including read

events) to location i. If a read event r reads the value written by the write event w, the partial order puts r after w and all write events preceding w, and before all write events succeeding w. Formally, for every unambiguous trace  $\tau$  of S(n, m, v), location  $1 \le i \le m$ , and  $x, y \in L(\tau, i)$ , we have that  $\langle x, y \rangle \in \Omega^e(\tau, i)$  iff one of the following conditions holds.

- 1.  $data(\tau(x)) = data(\tau(y)), op(\tau(x)) = W, and op(\tau(y)) = R.$
- 2.  $data(\tau(x)) = 0$  and  $data(\tau(y)) \neq 0$ .
- 3.  $\exists a, b \in L^w(\tau, i)$  such that  $\langle a, b \rangle \in \Omega(\tau, i)$ ,  $data(\tau(a)) = data(\tau(x))$ , and  $data(\tau(b)) = data(\tau(y))$ .

We now show that the relation  $\Omega^e(\tau, i)$  is a partial order. First, we need the following lemma about  $\Omega^e(\tau, i)$ .

**Lemma 5.1** For all unambiguous traces  $\tau$  of S(n, m, v), locations  $1 \leq i \leq m$  and  $r, s, t \in L(\tau, i)$ , if  $\langle r, s \rangle \in \Omega^e(\tau, i)$ , then either  $\langle r, t \rangle \in \Omega^e(\tau, i)$  or  $\langle t, s \rangle \in \Omega^e(\tau, i)$ .

**Proof**: Since  $\langle r,s\rangle \in \Omega^e(\tau,i)$ , either  $data(\tau(s)) \neq 0$  or there is a  $x \in L^w(\tau,i)$  such that  $data(\tau(s)) = data(\tau(x))$ . Since  $\tau$  is an unambiguous trace, we have that  $data(\tau(x)) \neq 0$ . Therefore, we get that  $data(\tau(s)) \neq 0$  in both cases. If  $data(\tau(t)) = 0$  we immediately get that  $\langle t,s\rangle \in \Omega^e(\tau,i)$ . So suppose  $data(\tau(t)) \neq 0$ . Since  $\tau$  is unambiguous, there is  $y \in L^w(\tau,i)$  such that  $data(\tau(t)) = data(\tau(y))$ . We have three cases from the definition of  $\langle r,s\rangle \in \Omega^e(\tau,i)$ .

- 1.  $data(\tau(r)) = data(\tau(s))$ ,  $op(\tau(r)) = W$ , and and  $op(\tau(s)) = R$ . Since  $\Omega$  is a total order on  $L^w(\tau, i)$ , either  $\langle r, y \rangle \in \Omega(\tau, i)$  or  $\langle y, r \rangle \in \Omega(\tau, i)$ . In the first case, we have  $\langle r, t \rangle \in \Omega^e(\tau, i)$ . In the second case, we have  $\langle t, s \rangle \in \Omega^e(\tau, i)$ .
- 2.  $data(\tau(r)) = 0$  and  $data(\tau(s)) \neq 0$ . We get that  $\langle r, t \rangle \in \Omega^e(\tau, i)$ .
- 3.  $\exists a,b \in L^w(\tau,i)$  such that  $\langle a,b \rangle \in \Omega(\tau,i)$ ,  $data(\tau(a)) = data(\tau(r))$ , and  $data(\tau(b)) = data(\tau(s))$ . Since  $\Omega$  is a total order on  $L^w(\tau,i)$ , either  $\langle a,y \rangle \in \Omega(\tau,i)$  or  $\langle y,a \rangle \in \Omega(\tau,i)$ . In the first case, we have  $\langle r,t \rangle \in \Omega^e(\tau,i)$ . In the second case, we have by transitivity  $\langle y,b \rangle \in \Omega(\tau,i)$  and therefore  $\langle t,s \rangle \in \Omega^e(\tau,i)$ .

**Lemma 5.2** For all unambiguous traces  $\tau$  of S(n, m, v) and locations  $1 \le i \le m$ , we have that  $\Omega^e(\tau, i)$  is a partial order.

**Proof**: We show that  $\Omega^e(\tau, i)$  is irreflexive. In other words, for all  $1 \leq x \leq |\tau|$ , we have that  $\langle x, x \rangle \notin \Omega^e(\tau, i)$ . This is an easy proof by contradiction by assuming  $\langle x, x \rangle \in \Omega^e(\tau, i)$  and performing a case analysis over the three resulting conditions.

We show that  $\Omega^e(\tau,i)$  is anti-symmetric. In other words, for all  $1 \leq x < y \leq |\tau|$ , if  $\langle x,y \rangle \in \Omega^e(\tau,i)$  then  $\langle y,x \rangle \notin \Omega^e(\tau,i)$ . We do a proof by contradiction. Suppose both  $\langle x,y \rangle \in \Omega^e(\tau,i)$  and  $\langle y,x \rangle \in \Omega^e(\tau,i)$ . We reason as in the proof of Lemma 5.1 to obtain  $data(\tau(x)) \neq 0$  and  $data(\tau(y)) \neq 0$ . Therefore there are  $a,b \in L^w(\tau,i)$  such that  $data(\tau(a)) = data(\tau(x))$  and  $data(\tau(b)) = data(\tau(y))$ . We perform the following case analysis.

- 1. a = b. Either op(x) = R and op(y) = R, or op(x) = W and op(y) = R, or op(x) = R and op(y) = W. In the first case  $\langle x, y \rangle \not\in \Omega^e(\tau, i)$  and  $\langle y, x \rangle \not\in \Omega^e(\tau, i)$ . In the second case  $\langle y, x \rangle \not\in \Omega^e(\tau, i)$ . In the third case  $\langle x, y \rangle \not\in \Omega^e(\tau, i)$ .
- 2.  $\langle a,b\rangle \in \Omega(\tau,i)$ . We have  $data(\tau(x)) \neq data(\tau(y))$  since  $\tau$  is unambiguous. Since  $\Omega(\tau,i)$  is a total order, we have  $\langle b,a\rangle \notin \Omega(\tau,i)$ . Therefore  $\langle y,x\rangle \notin \Omega^e(\tau,i)$ .
- 3.  $\langle b, a \rangle \in \Omega(\tau, i)$ . This case is symmetric to Case 2.

Finally, we show that  $\Omega^e(\tau, i)$  is transitive. Suppose  $\langle x, y \rangle \in \Omega^e(\tau, i)$  and  $\langle y, z \rangle \in \Omega^e(\tau, i)$ . From Lemma 5.1, either  $\langle x, z \rangle \in \Omega^e(\tau, i)$  or  $\langle z, y \rangle \in \Omega^e(\tau, i)$ . We have shown  $\Omega^e(\tau, i)$  to be anti-symmetric. Therefore  $\langle x, z \rangle \in \Omega^e(\tau, i)$ .

#### 5.1 Constraint graph

Suppose  $\tau$  is an unambiguous trace of S(n,m,v). We have that  $M(\tau,i)$  is a total order on  $P(\tau,i)$  for all  $1 \leq i \leq n$  from the definition of sequential consistency. We also have that  $\Omega^e(\tau,j)$  is a partial order on  $L(\tau,j)$  for all  $1 \leq j \leq m$  from Lemma 5.2. The union of the n total orders  $M(\tau,i)$  and m partial orders  $\Omega^e(\tau,j)$  imposes a graph on  $dom(\tau)$ . The acyclicity of this graph is a necessary and sufficient condition for the trace  $\tau$  to satisfy sequential consistency. We define a function G that for every witness  $\Omega$  returns a function  $G(\Omega)$ . The function  $G(\Omega)$  maps every unambiguous trace  $\tau$  of S(n,m,v) to the graph  $\langle dom(\tau), \bigcup_{1 \leq i \leq n} M(\tau,i) \cup \bigcup_{1 \leq j \leq m} \Omega^e(\tau,j) \rangle$ . The work of Gibbons and Korach [GK97] defines a constraint graph on the memory events of a run that is similar to  $G(\Omega)(\tau)$ .

**Theorem 5.3** For all  $n, m, v \geq 1$ , every unambiguous trace of S(n, m, v) is sequentially consistent iff there is a witness  $\Omega$  such that the graph  $G(\Omega)(\tau)$  is acyclic for every unambiguous trace  $\tau$  of S(n, m, v).

**Proof**: ( $\Rightarrow$ ) Suppose  $\tau$  is an unambiguous trace of S(n, m, v). Then  $\tau$  satisfies sequential consistency. There is a permutation f on  $\mathbb{N}_{|\tau|}$  such that conditions C1 and C2 are satisfied. For all  $1 \leq i \leq m$ , define  $\Omega(\tau, i)$  to be the total order on  $L^w(\tau, i)$  such that for all  $x, y \in L^w(\tau, i)$ , we have  $\langle x, y \rangle \in \Omega(\tau, i)$  iff f(x) < f(y). We show that the permutation f is a linearization of the vertices in  $G(\Omega)(\tau)$  that preserves all the edges. In other words, if  $\langle x, y \rangle \in M(\tau, i)$  for some  $1 \leq i \leq n$  or  $\langle x, y \rangle \in \Omega^e(\tau, j)$  for some  $1 \leq j \leq m$ , then f(x) < f(y). If

 $\langle x,y\rangle \in M(\tau,i)$  then we have from C1 that f(x) < f(y). We show below that if  $\langle x,y\rangle \in \Omega^e(\tau,j)$  then f(x) < f(y).

Let  $\tau' = \tau_{f^{-1}(1)}\tau_{f^{-1}(2)}\dots\tau_{f^{-1}(|\tau|)}$ . For all  $1 \leq u \leq |\tau|$  we have that  $\tau(u) = \tau'(f(u))$ . We first show for all  $a \in L^w(\tau, j)$  and  $x \in L(\tau, j)$ , if  $data(\tau(a)) = data(\tau(x))$  then  $f(a) \leq f(x)$ . Since  $\tau$  is unambiguous, we have that  $data(\tau(a)) = data(\tau(x)) \neq 0$ . Therefore  $data(\tau'(f(a))) = data(\tau'(f(x))) \neq 0$ . We have that either  $op(\tau'(f(x))) = R$  or x = a. In the first case  $f(a) \in upto(\tau', f(x))$  which implies that f(a) < f(x), and in the second case f(a) = f(x). Therefore  $f(a) \leq f(x)$ .

If  $\langle x,y\rangle\in\Omega^e(\tau,j)$  then we have three cases. In each case, we show that f(x)< f(y).

- 1.  $data(\tau(x)) = data(\tau(y)), op(\tau(x)) = W$ , and  $op(\tau(y)) = R$ . Since  $\tau$  is unambiguous  $data(\tau(x)) = data(\tau(y)) \neq 0$ . We get that  $data(\tau'(f(y))) \neq 0$  which means that  $upto(\tau', f(y)) \neq \emptyset$  and  $f(x) \in upto(\tau', f(y))$ . Therefore f(x) < f(y).
- 2.  $data(\tau(x)) = 0$  and  $data(\tau(y)) \neq 0$ . Since  $x \neq y$  we have  $f(x) \neq f(y)$ . Suppose f(y) < f(x). Since  $data(\tau(y)) \neq 0$  there is  $b \in L^w(\tau, j)$  such that  $data(\tau(b)) = data(\tau(y))$ . Therefore we have that  $f(b) \leq f(y) < f(x)$ . Therefore the set  $upto(\tau', f(x)) \neq \emptyset$ . Since  $\tau'$  is unambiguous and  $data(\tau'(f(x))) = 0$  we have a contradiction.
- 3.  $\exists a,b \in L^w(\tau,j)$  such that  $\langle a,b \rangle \in \Omega(\tau,j)$ ,  $data(\tau(a)) = data(\tau(x))$ , and  $data(\tau(b)) = data(\tau(y))$ . We show f(x) < f(y) by contradiction. Suppose f(x) = f(y). Then x = y and  $data(\tau(a)) = data(\tau(b))$ . Since  $\tau$  is unambiguous we get a = b which contradicts  $\langle a,b \rangle \in \Omega(\tau,j)$ . Suppose f(y) < f(x). We have that  $f(a) \leq f(x)$  and  $f(b) \leq f(y)$ . Since  $\langle a,b \rangle \in \Omega(\tau,j)$ , we have f(a) < f(b) from the definition of  $\Omega$ . Thus we have  $f(a) < f(b) \leq f(y) < f(x)$  Therefore  $f(a) \neq max(upto(\tau',f(x)))$ . Since  $\tau'$  is unambiguous and  $data(\tau'(f(a))) = data(\tau'(f(x)))$  we have a contradiction.
- ( $\Leftarrow$ ) Suppose  $\tau$  is a trace of S(n, m, v). Then there is a witness Ω such that G(Ω)(τ) is acyclic. Let f be a linearization of the vertices in G(Ω)(τ) that respects all edges. Then C1 is satisfied. Let τ' denote  $τ_{f^{-1}(1)}τ_{f^{-1}(2)} \dots τ_{f^{-1}(|τ|)}$ . Then we have that  $τ'(x) = τ(f^{-1}(x))$  for all  $1 \le x \le |τ'|$ . For any  $1 \le x \le |τ'|$ , suppose loc(τ'(x)) = j. There are two cases.
  - 1.  $data(\tau'(x)) = 0$ . We show that  $upto(\tau', x) = \emptyset$ . Consider any vertex  $1 \leq y \leq |\tau'|$  such that  $op(\tau'(y)) = W$  and  $loc(\tau'(y)) = j$ . Then  $\tau(f^{-1}(x)) = 0$  and  $\tau(f^{-1}(y)) \neq 0$ . Therefore  $\langle f^{-1}(x), f^{-1}(y) \rangle \in \Omega^e(\tau, j)$  and  $\langle f^{-1}(x), f^{-1}(y) \rangle$  is an edge in  $G(\Omega)(\tau)$ . Therefore  $f(f^{-1}(x)) < f(f^{-1}(y))$  or x < y. Thus we have that  $upto(\tau', x) = \emptyset$ .
  - 2.  $data(\tau'(x)) \neq 0$ . We show that  $upto(\tau', x) \neq \emptyset$  and if  $y = max(upto(\tau', x))$  then  $data(\tau'(x)) = data(\tau'(y))$ . From Assumption 1, there is  $a \in L^w(\tau', j)$  such that  $data(\tau'(a)) = data(\tau'(x))$  and since  $\tau'$  is unambiguous this

write is unique. Therefore  $data(\tau(f^{-1}(a))) = data(\tau(f^{-1}(x)))$ . Either  $f^{-1}(a) = f^{-1}(x)$  or  $op(\tau(f^{-1}(x))) = R$  in which case  $\langle f^{-1}(a), f^{-1}(x) \rangle \in \Omega^e(\tau, j)$ . In both cases, we have  $a \leq x$  and therefore  $upto(\tau', x) \neq \emptyset$ . Consider any vertex  $1 \leq b \leq |\tau'|$  such that  $op(\tau'(b)) = W$ ,  $loc(\tau'(b)) = j$ , and a < b. Then  $\langle f^{-1}(a), f^{-1}(b) \rangle \in \Omega(\tau, j)$  and  $\langle f^{-1}(x), f^{-1}(b) \rangle \in \Omega^e(\tau, j)$ . Therefore x < b. We thus get  $a = max(upto(\tau', x))$ .

Theorems 4.1 and 5.3 can be combined easily to yield the following theorem.

Corollary 5.4 For all  $n, m \ge 1$ , every trace of S(n, m) is sequentially consistent iff there is a witness  $\Omega$  such that the graph  $G(\Omega)(\tau)$  is acyclic for every unambiguous trace  $\tau$  of S(n, m).

#### 5.2 Simple witness

Corollary 5.4 suggests that in order to prove that the memory system S(n, m, v) is sequentially consistent, we produce a witness  $\Omega$  and show for every unambiguous trace  $\tau$  of S(n,m) that the graph  $G(\Omega)(\tau)$  is acyclic. But the construction of the witness is still left to the verifier. In this section, we argue that a simple witness, which orders the write events to a location exactly in the order in which they occur, suffices for a number of memory systems occurring in practice. Formally, a witness  $\Omega$  is simple if for all traces  $\tau$  of S(n, m, v) and locations  $1 \leq i \leq m$ , we have  $\langle x, y \rangle \in \Omega(\tau, i)$  iff x < y for all  $x, y \in L^w(\tau, i)$ .

Consider the memory system of Figure 1. We argue informally that a simple witness is a good witness for this memory system. Permission to perform writes flows from one cache to another by means of the ACKX message. Note that for each location j, the variable owner[j] is set to 0 (which is not the id of any processor) when an ACKX message is generated. When the ACKX message is received at the destination (by the UPD event), the destination moves to EXC state and sets owner[j] to the destination id. A new ACKX message is generated only when  $owner[j] \neq 0$ . Thus, the memory system has the property that each memory location can be held in EXC state by at most one cache. Moreover, writes to the location j can happen only when the cache has the location in EXC state. Therefore, at most one cache can be performing writes to a memory location. This indicates that the logical order of the write events is the same as their temporal order. In other words, a simple witness is the correct witness for demonstrating that a run is sequentially consistent.

In general, for any memory system in which at any time at most one processor can perform write events to a location, a simple witness is very likely to be the correct witness. Most memory systems occurring in practice [LLG<sup>+</sup>90, KOH<sup>+</sup>94, BDH<sup>+</sup>99, BGM<sup>+</sup>00] have this property. In Section 8, we describe a model checking algorithm to verify the correctness of a memory system with respect to a simple witness. If a simple witness is indeed the desired witness and the memory system is designed correctly, then our algorithm will be able to verify its correctness. Otherwise, it will produce an error trace suggesting

to the verifier that either there is an error in the memory system or the simple witness is not the correct witness. Thus our method for checking sequential consistency is clearly sound. We have argued that it is also complete on most shared-memory systems that occur in practice.

### 6 Nice cycle reduction

For some  $n, m, v \geq 1$ , let S(n, m, v) be a memory system and  $\Omega$  a witness for it. Let  $\tau$  be an unambiguous trace of S(n, m, v). Corollary 5.4 tells us that the absence of cycles in the graphs  $G(\Omega)(\tau)$  generated by the unambiguous traces of S(n, m) is a necessary and sufficient condition for every trace of S(n, m) to be sequentially consistent. In this section, we show that it suffices to detect a special class of cycles called nice cycles. In Section 8, we will show that detection of nice cycles can be performed by model checking.

We fix some  $k \geq 1$  and use the symbol  $\oplus$  to denote addition over the additive group with elements  $\mathbb{N}_k$  and identity element k. A k-nice cycle in  $G(\Omega)(\tau)$  is a sequence  $u_1, v_1, \ldots, u_k, v_k$  of distinct vertices in  $\mathbb{N}_{|\tau|}$  such that the following conditions are true.

- 1. For all  $1 \le x \le k$ , we have  $\langle u_x, v_x \rangle \in M(\tau, i)$  for some  $1 \le i \le n$  and  $\langle v_x, u_{x \oplus 1} \rangle \in \Omega^e(\tau, j)$  for some  $1 \le j \le m$ .
- 2. For all  $1 \le x < y \le k$  and for all  $1 \le i, j \le n$ , if  $\langle u_x, v_x \rangle \in M(\tau, i)$  and  $\langle u_y, v_y \rangle \in M(\tau, j)$  then  $i \ne j$ .
- 3. For all  $1 \le x < y \le k$  and for all  $1 \le i, j \le m$ , if  $\langle v_x, u_{x \oplus 1} \rangle \in \Omega^e(\tau, i)$  and  $\langle v_y, u_{y \oplus 1} \rangle \in \Omega^e(\tau, j)$  then  $i \ne j$ .

In a k-nice cycle, no two edges belong to the relation  $M(\tau,i)$  for any processor i. Similarly, no two edges belong to the relation  $\Omega^e(\tau,j)$  for any location j. The above definition also implies that if a cycle is k-nice then  $k \leq \min(\{n,m\})$ .

**Theorem 6.1** If the graph  $G(\Omega)(\tau)$  has a cycle, then it has a k-nice cycle for some k such that  $1 \le k \le \min(\{n, m\})$ .

**Proof:** Suppose  $G(\Omega)(\tau)$  has no k-nice cycles but does have a cycle. Consider the shortest such cycle  $u_1, \ldots, u_l$  where  $l \geq 1$ . For this proof, we denote by  $\oplus$  addition over the additive group with elements  $\mathbb{N}_l$  and identity element l. Then for all  $1 \leq x \leq l$  either  $\langle u_x, u_{x \oplus 1} \rangle \in M(\tau, i)$  for some  $1 \leq i \leq n$  or  $\langle u_x, u_{x \oplus 1} \rangle \in \Omega^e(\tau, i)$  for some  $1 \leq i \leq m$ .

Since the cycle  $u_1, \ldots, u_l$  is not k-nice for any k, there are  $1 \le a < b \le l$  such that either (1)  $\langle u_a, u_{a \oplus 1} \rangle \in M(\tau, i)$  and  $\langle u_b, u_{b \oplus 1} \rangle \in M(\tau, i)$  for some  $1 \le i \le n$ , or (2)  $\langle u_a, u_{a \oplus 1} \rangle \in \Omega^e(\tau, i)$  and  $\langle u_b, u_{b \oplus 1} \rangle \in \Omega^e(\tau, i)$  for some  $1 \le i \le m$ .

Case (1). We have from the definition of M that  $u_a < u_{a \oplus 1}$  and  $u_b < u_{b \oplus 1}$ . Either  $u_a < u_b$  or  $u_b < u_a$ . If  $u_a < u_b$  then  $u_a < u_{b \oplus 1}$  or  $\langle u_a, u_{b \oplus 1} \rangle \in M(\tau, i)$ . If  $u_b < u_a$  then  $u_b < u_{a \oplus 1}$  or  $\langle u_b, u_{a \oplus 1} \rangle \in M(\tau, i)$ . In both cases, we have a contradiction since the cycle can be made shorter.

Case (2). From Lemma 5.1, either  $\langle u_a, u_b \rangle \in \Omega^e(\tau, i)$  or  $\langle u_b, u_{a \oplus 1} \rangle \in \Omega^e(\tau, i)$ . In both cases, we have a contradiction since the cycle can be made shorter.

### 7 Symmetry reduction

Suppose S(n, m, v) is a memory system for some  $n, m, v \ge 1$ . In this section, we use symmetry arguments to further reduce the class of cycles that need to be detected in constraint graphs. Each k-nice cycle has  $2 \times k$  edges with one edge each for k different processors and k different locations. These edges can potentially occur in any order yielding a set of isomorphic cycles. But if the memory system S(n, m, v) is symmetric with respect to processor and memory location ids, presence of any one of the isomorphic nice cycles implies the existence of a nice cycle in which the edges are arranged in a canonical order. Thus, it suffices to search for a cycle with edges in a canonical order.

We discuss processor symmetry in Section 7.1 and location symmetry in Section 7.2. We combine processor and location symmetry to demonstrate the reduction from nice cycles to canonical nice cycles in Section 7.3.

#### 7.1 Processor symmetry

For any permutation  $\lambda$  on  $\mathbb{N}_n$ , the function  $\lambda^p$  on E(n, m, v) permutes the processor ids of events according to  $\lambda$ . Formally, for all  $e = \langle a, b, c, d \rangle \in E(n, m, v)$ , we define  $\lambda^p(e) = \langle a, \lambda(b), c, d \rangle$ . The function  $\lambda^p$  is extended to sequences in  $E(n, m, v)^*$  in the natural way.

**Assumption 3 (Processor symmetry)** For every permutation  $\lambda$  on  $\mathbb{N}_n$  and for all traces  $\tau$  of the memory system S(n, m, v), we have that  $\lambda^p(\tau)$  is a trace of S(n, m, v).

We argue informally that the memory system in Figure 1 satisfies Assumption 3. The operations performed by the various parameterized actions on the state variables that store processor ids are symmetric. Suppose s is a state of the system. We denote by  $\lambda^p(s)$  the state obtained by permuting the values of variables that store processors ids according to  $\lambda$ . Then, for example, if the action UPD(i) in some state s yields state t, then the action  $UPD(\lambda(i))$  in state  $\lambda^p(s)$  yields the state  $\lambda^p(t)$ . Thus, from any run  $\sigma$  we can construct another run  $\lambda^p(\sigma)$ . If a shared-memory system is described with symmetric types, such as scalarsets [ID96], used to model variables containing processor ids, then it has the property of processor symmetry by construction.

The following lemma states that the sequential consistency memory model is symmetric with respect to processor ids. It states that two events in a trace  $\tau$  ordered by sequential consistency remain ordered under any permutation of processor ids.

**Lemma 7.1** Suppose  $\lambda$  is a permutation on  $\mathbb{N}_n$ . Suppose  $\tau$  and  $\tau'$  are traces of S(n, m, v) such that  $\tau' = \lambda^p(\tau)$ . Then for all  $1 \leq x, y \leq |\tau|$ , and for all  $1 \leq i \leq n$ , we have that  $\langle x, y \rangle \in M(\tau, i)$  iff  $\langle x, y \rangle \in M(\tau', \lambda(i))$ .

**Proof**: For all  $1 \le x, y \le |\tau|$  and for all  $1 \le i \le n$ , we have that

The following lemma states that the partial order  $\Omega^e$  obtained from a simple witness  $\Omega$  is symmetric with respect to processor ids. It states that two events to location i ordered by  $\Omega^e(\tau,i)$  in a trace  $\tau$  remain ordered under any permutation of processor ids.

**Lemma 7.2** Suppose  $\Omega$  is a simple witness for the memory system S(n, m, v) and  $\lambda$  is a permutation on  $\mathbb{N}_n$ . Suppose  $\tau$  and  $\tau'$  are unambiguous traces of S(n, m, v) such that  $\tau' = \lambda^p(\tau)$ . Then for all  $1 \leq x, y \leq |\tau|$  and for all  $1 \leq i \leq m$ , we have that  $\langle x, y \rangle \in \Omega^e(\tau, i)$  iff  $\langle x, y \rangle \in \Omega^e(\tau', i)$ .

**Proof**: We have  $\langle x, y \rangle \in \Omega(\tau, i)$  iff x < y iff  $\langle x, y \rangle \in \Omega(\tau', i)$ . From the definition of  $\Omega^e(\tau, i)$  we have the following three cases.

- 1.  $data(\tau(x)) = data(\tau(y)), op(\tau(x)) = W, op(\tau(y)) = R \text{ iff } data(\tau'(x)) = data(\tau'(y)), op(\tau'(x)) = W, op(\tau'(y)) = R.$
- 2.  $data(\tau(x)) = 0$  and  $data(\tau(y)) \neq 0$  iff  $data(\tau'(x)) = 0$  and  $data(\tau'(y)) \neq 0$ .
- 3.  $\exists a, b \in L^w(\tau, i)$  such that a < b,  $data(\tau(a)) = data(\tau(x))$ ,  $data(\tau(b)) = data(\tau(y))$  iff  $\exists a, b \in L^w(\tau', i)$  such that a < b,  $data(\tau'(a)) = data(\tau'(x))$ ,  $data(\tau'(b)) = data(\tau'(y))$ .

#### 7.2 Location symmetry

For any permutation  $\lambda$  on  $\mathbb{N}_m$ , the function  $\lambda^l$  on E(n, m, v) permutes the location ids of events according to  $\lambda$ . Formally, for all  $e = \langle a, b, c, d \rangle \in E(n, m, v)$ , we define  $\lambda^l(e) = \langle a, b, \lambda(c), d \rangle$ . The function  $\lambda^l$  is extended to sequences in  $E(n, m, v)^*$  in the natural way.

Assumption 4 (Location symmetry) For every permutation  $\lambda$  on  $\mathbb{N}_m$  and for all traces  $\tau$  of the memory system S(n, m, v), we have that  $\lambda^l(\tau)$  is a trace of S(n, m, v).

We can argue informally that the memory system in Figure 1 satisfies Assumption 4 also. The operations performed by the various parameterized actions on the state variables that store location ids are symmetric. Suppose s is a state of the system. We denote by  $\lambda^l(s)$  the state obtained by permuting the values of variables that store location ids according to  $\lambda$ . Then, for example, if the action UPD(i) in some state s yields state t, then the action  $UPD(\lambda(i))$  in state

 $\lambda^l(s)$  yields the state  $\lambda^l(t)$ . If scalarsets are used for modeling variables containing location ids, the shared-memory system will have the property of location symmetry by construction.

The following lemma states that the sequential consistency memory model is symmetric with respect to location ids. It states that two events in a trace  $\tau$  ordered by sequential consistency remain ordered under any permutation of location ids.

**Lemma 7.3** Suppose  $\lambda$  is a permutation on  $\mathbb{N}_m$ . Suppose  $\tau$  and  $\tau'$  are traces of S(n, m, v) such that  $\tau' = \lambda^l(\tau)$ . Then for all  $1 \leq x, y \leq |\tau|$ , and for all  $1 \leq i \leq n$ , we have that  $\langle x, y \rangle \in M(\tau, i)$  iff  $\langle x, y \rangle \in M(\tau', i)$ .

**Proof**: For all  $1 \le x, y \le |\tau|$  and for all  $1 \le i \le m$ , we have that

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 \langle x, y \rangle \in M(\tau, i)  \Leftrightarrow \quad proc(\tau(x)) = proc(\tau(y)) = i \text{ and } x < y  \Leftrightarrow \quad proc(\tau'(x)) = proc(\tau'(y)) = i \text{ and } x < y  \Leftrightarrow \quad \langle x, y \rangle \in M(\tau', i).
```

The following lemma states that the partial order  $\Omega^e$  obtained from a simple witness  $\Omega$  is symmetric with respect to location ids. It states that two events to location i ordered by  $\Omega^e(\tau,i)$  in a trace  $\tau$  remain ordered under any permutation of location ids.

**Lemma 7.4** Suppose  $\Omega$  is a simple witness for the memory system S(n, m, v) and  $\lambda$  is a permutation on  $\mathbb{N}_m$ . Suppose  $\tau$  and  $\tau'$  are unambiguous traces of S(n, m, v) such that  $\tau' = \lambda^l(\tau)$ . Then for all  $1 \leq x, y \leq |\tau|$  and for all  $1 \leq i \leq m$ , we have that  $\langle x, y \rangle \in \Omega^e(\tau, i)$  iff  $\langle x, y \rangle \in \Omega^e(\tau', \lambda(i))$ .

**Proof**: We have  $\langle x, y \rangle \in \Omega(\tau, i)$  iff x < y iff  $\langle x, y \rangle \in \Omega(\tau', \lambda(i))$ . From the definition of  $\Omega^e(\tau, i)$  we have the following three cases.

- 1.  $data(\tau(x)) = data(\tau(y)), \ op(\tau(x)) = W, \ op(\tau(y)) = R \ iff \ data(\tau'(x)) = data(\tau'(y)), \ op(\tau'(x)) = W, \ op(\tau'(y)) = R.$
- 2.  $data(\tau(x)) = 0$  and  $data(\tau(y)) \neq 0$  iff  $data(\tau'(x)) = 0$  and  $data(\tau'(y)) \neq 0$ .
- 3.  $\exists a, b \in L^w(\tau, i)$  where a < b,  $data(\tau(a)) = data(\tau(x))$ , and  $data(\tau(b)) = data(\tau(y))$  iff  $\exists a, b \in L^w(\tau', \lambda(i))$  where a < b,  $data(\tau'(a)) = data(\tau'(x))$ , and  $data(\tau'(b)) = data(\tau'(y))$ .

### 7.3 Combining processor and location symmetry

We fix some  $k \geq 1$  and use the symbol  $\oplus$  to denote addition over the additive group with elements  $\mathbb{N}_k$  and identity element k. A k-nice cycle  $u_1, v_1, \ldots, u_k, v_k$  is canonical if  $\langle u_x, v_x \rangle \in M(\tau, x)$  and  $\langle v_x, u_{x \oplus 1} \rangle \in \Omega^e(\tau, x \oplus 1)$  for all  $1 \leq x \leq 1$ 

k. In other words, the processor edges in a canonical nice cycle are arranged in increasing order of processor ids. Similarly, the location edges are arranged in increasing order of location ids. The following theorem claims that if the constraint graph of a run has a nice cycle then there is some run with a canonical nice cycle as well.

**Theorem 7.5** Suppose  $\Omega$  is a simple witness for the memory system S(n, m, v). Let  $\tau$  be an unambiguous trace of S(n, m, v). If the graph  $G(\Omega)(\tau)$  has a k-nice cycle, then there is an unambiguous trace  $\tau''$  of S(n, m, v) such that  $G(\Omega)(\tau'')$  has a canonical k-nice cycle.

**Proof**: Let  $u_1, v_1, \ldots, u_k, v_k$  be a k-nice cycle in  $G(\Omega)(\tau)$ . Let  $1 \leq i_1, \ldots, i_k \leq n$  and  $1 \leq j_1, \ldots, j_k \leq m$  be such that  $\langle u_x, v_x \rangle \in M(\tau, i_x)$  and  $\langle v_x, u_{x \oplus 1} \rangle \in \Omega^e(\tau, j_{x \oplus 1})$  for all  $1 \leq x \leq k$ . Let  $\alpha$  be a permutation on  $\mathbb{N}_n$  that maps  $i_x$  to x for all  $1 \leq x \leq k$ . Then from Assumption 3 there is a trace  $\tau'$  of S(n, m, v) such that  $\tau' = \alpha^p(\tau)$ . Let  $\beta$  be a permutation on  $\mathbb{N}_m$  that maps  $j_x$  to x for all  $1 \leq x \leq k$ . Then from Assumption 4 there is a trace  $\tau''$  of S(n, m, v) such that  $\tau'' = \beta^l(\tau')$ . For all  $1 \leq x \leq k$ , we have that

```
 \langle u_x, v_x \rangle \in M(\tau, i_x)  \Leftrightarrow \langle u_x, v_x \rangle \in M(\tau', \alpha(i_x)) = M(\tau', x)  from Lemma 7.1 
 \Leftrightarrow \langle u_x, v_x \rangle \in M(\tau'', x)  from Lemma 7.3.
```

For all  $1 \le x \le k$ , we also have that

```
 \begin{array}{ll} \langle v_x,u_{x\oplus 1}\rangle \in \Omega^e(\tau,j_{x\oplus 1}) \\ \Leftrightarrow & \langle v_x,u_{x\oplus 1}\rangle \in \Omega^e(\tau',j_{x\oplus 1}) \\ \Leftrightarrow & \langle v_x,u_{x\oplus 1}\rangle \in \Omega^e(\tau'',\beta(j_{x\oplus 1})) = \Omega^e(\tau'',x\oplus 1) \end{array} \text{ from Lemma 7.2}
```

Therefore  $u_1, v_1, \ldots, u_k, v_k$  is a canonical k-nice cycle in  $G(\Omega)(\tau'')$ .

Finally, Corollary 5.4 and Theorems 6.1 and 7.5 yield the following theorem.

Corollary 7.6 Suppose there is a simple witness  $\Omega$  such that for all unambiguous traces  $\tau$  of S(n,m) the graph  $G(\Omega)(\tau)$  does not have a canonical k-nice cycle for all  $1 \le k \le \min(\{n,m\})$ . Then every trace of S(n,m) is sequentially consistent.

# 8 Model checking memory systems

Suppose S(n, m, v) is a memory system for some  $n, m, v \ge 1$ . Let  $\Omega$  be a simple witness for S(n, m). In this section, we present a model checking algorithm that, given a k such that  $1 \le k \le \min(\{n, m\})$ , determines whether there is a trace  $\tau$  in S(n, m) such that the graph  $G(\Omega)(\tau)$  has a canonical k-nice cycle. Corollary 7.6 then allows us to verify sequential consistency on S(n, m, v) by  $\min(\{n, m\})$  such model checking lemmas. We fix some k such that  $1 \le k \le \min(\{n, m\})$ . We use the symbol  $\oplus$  to denote addition over the additive group

```
Automaton Constrain_k(j) for 1 \le j \le k
States \{a, b\}
Initial state a
Accepting states \{a, b\}
                                                                          Automaton Constrain_k(j) for k < j \le m
Alphabet E(n, m, 2)
                                                                          States \{a\}
Transitions
                                                                          Initial state a
[] \neg (op(e) = W \land loc(e) = j)\rightarrow s' = s
                                                                          Accepting states \{a\}
Alphabet E(n, m, 2)
[] \ s = a \land op(e) = W \land loc(e) = j \land data(e) = 0\rightarrow s' = a
                                                                          Transitions
                                                                          [] \neg (op(e) = W \land loc(e) = j) \lor data(e) = 0\rightarrow s' = s
 [] \ s = a \land op(e) = W \land loc(e) = j \land data(e) = 1   \rightarrow s' = b 
 [] \ s = b \land op(e) = W \land loc(e) = j \land data(e) = 2   \rightarrow s' = b
```

Figure 2: Automaton  $Constrain_k(j)$ 

Figure 3: Automaton  $Check_k(i)$ 

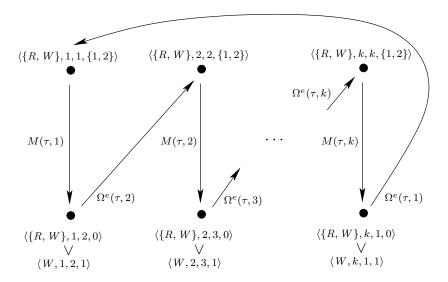


Figure 4: Canonical k-nice cycle

with elements  $\mathbb{N}_k$  and identity element k. The model checking algorithm makes use of m automata named  $Constrain_k(j)$  for  $1 \leq j \leq m$ , and k automata named  $Check_k(i)$  for  $1 \leq i \leq k$ . We define these automata formally below.

For all memory locations  $1 \leq j \leq m$ , let  $Constrain_k(j)$  be the regular set of sequences in E(n,m,2) represented by the automaton in Figure 2. The automaton  $Constrain_k(j)$ , when composed with S(n,m,v), constrains the write events to location j. If  $1 \leq j \leq k$  then  $Constrain_k(j)$  accepts traces where the first few (0 or more) write events have data value 0 followed by exactly one write with data value 1 followed by (0 or more) write events with data value 2. If  $k < j \leq m$  then  $Constrain_k(j)$  accepts traces where all writes to location j have data value 0.

For all  $1 \le i \le k$ , let  $Check_k(i)$  be the regular set of sequences in E(n, m, 2) represented by the automaton in Figure 3. The automaton  $Check_k(i)$  accepts a trace  $\tau$  if there are events x and y at processor i, with x occurring before y, such that x is an event to location i with data value 1 or 2 and y is an event to location  $i \oplus 1$  with data value 0 or 1. Moreover, the event y is required to be a write event if its data value is 1.

In order to check for canonical k-nice cycles, we compose the memory system S(n, m, 2) with  $Constrain_k(j)$  for all  $1 \leq j \leq m$  and with  $Check_k(i)$  for all  $1 \leq i \leq k$  and use a model checker to determine if the resulting automaton has a run.

Any accepting run of the composed system has  $2 \times k$  events which can be arranged as shown in Figure 4 to yield a canonical k-nice cycle. Each processor i for  $1 \le i \le k$  and each location j for  $1 \le j \le k$  supplies 2 events. Each event is marked by a 4-tuple denoting the possible values for that event. For

example, the 4-tuple  $\langle \{R,W\},1,1,\{1,2\} \rangle$  denotes a read event or a write event by processor 1 to location 1 with data value 1 or 2. The edge labeled by  $M(\tau,i)$  is due to the total order imposed by sequential consistency on the events at processor i. The edge labeled by  $\Omega^e(\tau,j)$  is due to the partial order imposed by the simple witness on the events to location j. For example, consider the edge labeled  $\Omega^e(\tau,2)$  with the source event labeled by  $\langle \{R,W\},1,2,0\rangle \vee \langle W,1,2,1\rangle$  and the sink event labeled by  $\langle \{R,W\},2,2,\{1,2\}\rangle$ . In any run of the composed system, the write events to location 2 with value 0 occur before the write event with value 1 which occurs before the write events with value 2. Since  $\Omega$  is a simple witness, the partial order  $\Omega^e(\tau,2)$  orders all events labeled with 0 before all events labeled with 1 or 2. Hence any event denoted by  $\langle \{R,W\},1,2,0\rangle$  is ordered before any event denoted by  $\langle \{R,W\},2,2,\{1,2\}\rangle$ . Moreover, the unique write event to location 2 with data value 1 is ordered before any event denoted by  $\langle \{R,W\},2,2,\{1,2\}\rangle$ .

We have given an intuitive argument above that a canonical k-nice cycle can be constructed from any run in the composed system. The following theorem proves that it is necessary and sufficient to check that the composed system has a run.

**Theorem 8.1** There is a canonical k-nice cycle in  $G(\Omega)(\tau)$  for some unambiguous trace  $\tau$  of S(n,m) iff there is a trace  $\tau'$  of S(n,m,2) such that  $\tau' \in Constrain_k(j)$  for all  $1 \leq j \leq m$  and  $\tau' \in Check_k(i)$  for all  $1 \leq i \leq k$ .

**Proof**: ( $\Rightarrow$ ) Suppose there is a canonical k-nice cycle  $u_1, v_1, \ldots, u_k, v_k$  in the graph  $G(\Omega)(\tau)$  for some unambiguous trace  $\tau$  of S(n, m). Then  $\langle u_x, v_x \rangle \in M(\tau, x)$  and  $\langle v_x, u_{x \oplus 1} \rangle \in \Omega^e(\tau, x \oplus 1)$  for all  $1 \le x \le k$ . From the definition of  $\Omega^e(\tau, x)$ , we have that  $data(\tau(x)) \ne 0$  for all  $1 \le x \le k$ . Therefore, for all  $1 \le x \le k$ , there is a unique write event  $w_x$  such that  $data(\tau(w_x)) = data(\tau(u_x))$ .

For all  $1 \leq j \leq m$ , let  $V_j$  be the set of data values written by the write events to location j in  $\tau$ , and let  $f_j: V_j \to \mathbb{N}_{|\tau|}$  be the function such that  $f_j(v)$  is the index of the unique write event to location j with data value v. We define a renaming function  $\lambda: \mathbb{N}_m \times \mathbb{W} \to \mathbb{W}_2$  as follows. For all  $k < j \leq m$  and  $v \in \mathbb{W}$ , we have  $\lambda(j,x) = 0$ . For all  $1 \leq j \leq k$  and  $v \in \mathbb{W}$ , we split the definition into two cases. For  $v \in V_j$ , we have

$$\lambda(j, v) = 0, & \text{if } f_j(v) < w_j \\ 1, & \text{if } f_j(v) = w_j \\ 2, & \text{if } f_j(v) > w_j.$$

For  $v \notin V_j$ , we have

$$\lambda(j, v) = 0, \text{ if } v = 0$$

$$2, \text{ if } v \neq 0.$$

From Assumption 2, there is a trace  $\tau'$  of S(n, m, 2) such that  $\tau' = \lambda^d(\tau)$ . In  $\tau'$ , for every location j such that  $1 \leq j \leq k$  every write event before  $w_j$  has the data value 0, the write event at  $w_j$  has the data value 1, and the write

events after  $w_j$  have the data value 2. Moreover, for every location j such that  $k < j \le m$  every write event has the data value 0. Therefore  $\tau' \in Constrain_k(i)$  for all  $1 \le i \le k$ .

We show that  $\tau' \in Check_k(i)$  for all  $1 \leq i \leq k$ . Since  $\langle u_i, v_i \rangle \in M(\tau, i)$ , we have that  $u_i < v_i$  for all  $1 \leq i \leq k$ . We already have that  $data(\tau'(u_i)) = data(\tau'(w_i)) = 1$  for all  $1 \leq i \leq k$ . Therefore all we need to show is that for all  $1 \leq i \leq k$  we have  $data(\tau'(v_i)) = 0$  or  $op(\tau'(v_i)) = W$  and  $data(\tau'(v_i)) = 1$ . Since  $\langle v_i, u_{i \oplus 1} \rangle \in \Omega^e(\tau, i \oplus 1)$ , one of the following conditions hold.

- 1.  $data(\tau(v_i)) = data(\tau(u_{i\oplus 1})), \ op(\tau(v_i)) = W, \ and \ op(\tau(u_{i\oplus 1})) = R.$  We have that  $op(\tau'(v_i)) = op(\tau(v_i)) = W$ . Since  $data(\tau(v_i)) = data(\tau(u_{i\oplus 1}))$  we have  $data(\tau'(v_i)) = data(\tau'(u_{i\oplus 1})) = 1$ . Thus, we get  $op(\tau'(v_i)) = W$  and  $data(\tau'(v_i)) = 1$ .
- 2.  $data(\tau(v_i)) = 0$  and  $data(\tau(u_{i\oplus 1})) \neq 0$ . From the definition of  $\lambda$ , we get that  $data(\tau'(v_i)) = 0$ .
- 3.  $\exists a \in L^w(\tau, i \oplus 1)$  such that  $\langle a, w_{i \oplus 1} \rangle \in \Omega(\tau, i \oplus 1)$  and  $data(\tau(a)) = data(\tau(v_i))$ . Since  $\langle a, b \rangle \in \Omega(\tau, i \oplus 1)$  and  $\Omega$  is a simple witness we get a < b. Therefore  $\lambda(i \oplus 1, data(\tau(a))) = 0$ . Thus  $\lambda(i \oplus 1, data(\tau(v_i))) = 0$  and  $data(\tau'(v_i)) = 0$ .

Thus, in all cases we have that either  $data(\tau'(v_i)) = 0$  or  $op(\tau'(v_i)) = W$  and  $data(\tau'(v_i)) = 1$ . Therefore  $\tau' \in Check_k(i)$ .

 $(\Leftarrow)$  Suppose there is a trace  $\tau'$  of S(n, m, 2) such that  $\tau' \in Constrain_k(j)$ for all  $1 \leq j \leq m$  and  $\tau' \in Check_k(i)$  for all  $1 \leq i \leq k$ . For all  $1 \leq i \leq k$ , let  $1 \leq u_i < v_i \leq |\tau'|$  be such that the automaton  $Check_k(i)$  enters state b for the first time on observing  $\tau'(u_i)$  and enters state err for the first time on observing  $\tau'(v_i)$ . Therefore we have  $proc(\tau'(u_i)) = i$ ,  $loc(\tau'(u_i)) = i$ , and  $data(\tau'(u_i)) \in \{1,2\}.$  We also have  $proc(\tau'(v_i)) = i, loc(\tau'(v_i)) = i \oplus 1,$  and either  $data(\tau'(v_i)) = 0$  or  $op(\tau'(v_i)) = W$  and  $data(\tau'(v_i)) = 1$ . From Assumption 2, there is an unambiguous trace  $\tau$  of S(n,m) and a renaming function  $\lambda: \mathbb{N}_m \times \mathbb{W} \to \mathbb{W}_2$  such that  $\tau' = \lambda^d(\tau)$ . We will show that  $u_1, v_1, \ldots, u_k, v_k$ is a canonical k-nice cycle in  $G(\Omega)(\tau)$ . Since  $proc(\tau(u_i)) = proc(\tau(v_i)) = i$ and  $u_i < v_i$ , we have  $\langle u_i, v_i \rangle \in M(\tau, i)$  for all  $1 \leq i \leq k$ . We show that  $\langle v_i, u_{i \oplus 1} \rangle \in \Omega^e(\tau, i \oplus 1)$  for all  $1 \leq i \leq k$ . First  $loc(\tau(v_i)) = loc(\tau(u_{i \oplus 1})) = i \oplus 1$ . For all  $u, v \in L^w(\tau, i)$ , if  $\lambda(i, data(\tau(u))) < \lambda(i, data(\tau(v)))$  then u < v from the property of  $Constrain_k(i)$ . Since  $data(\tau'(u_{i\oplus 1})) \in \{1,2\}$ , we have from the property of a renaming function that  $data(\tau(u_{i\oplus 1})) \neq 0$ . There are two cases on  $\tau'(v_i)$ .

1.  $data(\tau'(v_i)) = 0$ . There are two subcases:  $data(\tau(v_i)) = 0$  or  $\lambda(i \oplus 1, data(\tau(v_i))) = 0$ . In the first subcase, since  $data(\tau(u_{i\oplus 1})) \neq 0$ , we have  $\langle v_i, u_{i\oplus 1} \rangle \in \Omega^e(\tau, i \oplus 1)$ . In the second subcase, there are  $a, b \in L^w(\tau, i \oplus 1)$  such that  $data(\tau(a)) = data(\tau(v_i))$  and  $data(\tau(b)) = data(\tau(u_{i\oplus 1}))$ . Since  $data(\tau'(a)) = 0$  and  $data(\tau'(b)) \in \{1, 2\}$ , we get from the definition of  $Constrain_k(i \oplus 1)$  that a < b or  $\langle a, b \rangle \in \Omega(\tau, i \oplus 1)$ . Therefore  $\langle v_i, u_{i\oplus 1} \rangle \in \Omega^e(\tau, i \oplus 1)$ .

2.  $op(\tau'(v_i)) = W$  and  $data(\tau'(v_i)) = 1$ . We have that  $op(\tau(v_i)) = W$ . There is an event  $b \in L^w(\tau, i \oplus 1)$  such that  $data(\tau(b)) = data(\tau(u_{i \oplus 1}))$ . There are two subcases:  $data(\tau'(u_{i \oplus 1})) = 1$  or  $data(\tau'(u_{i \oplus 1})) = 2$ . In the first subcase, we have  $v_i = b$  since  $Constrain_k(i \oplus 1)$  accepts traces with a single write event labeled with 1. Therefore  $data(\tau(v_i)) = data(\tau(u_{i \oplus 1}))$ ,  $op(\tau(v_i)) = W$  and  $op(\tau(u_{i \oplus 1})) = R$ , and we get  $\langle v_i, u_{i \oplus 1} \rangle \in \Omega^e(\tau, i \oplus 1)$ . In the second subcase, since  $data(\tau'(a)) = 1$  and  $data(\tau'(b)) = 2$ , we get from the definition of  $Constrain_k(i \oplus 1)$  that a < b or  $\langle a, b \rangle \in \Omega(\tau, i \oplus 1)$ . Therefore  $\langle v_i, u_{i \oplus 1} \rangle \in \Omega^e(\tau, i \oplus 1)$ .

Therefore  $u_1, v_1, \ldots, u_k, v_k$  is a canonical k-nice cycle in  $G(\Omega)(\tau)$ .

**Example.** We now give an example to illustrate the method described in this section. Although the memory system in Figure 1 is sequentially consistent, an earlier version had an error. The assignment owner[j] := 0 was missing in the guarded command of the action  $\langle ACKS, i, j \rangle$ . We modeled the system in TLA+ [Lam94] and model checked the system configuration with two processors and two locations using the model checker TLC [YML99]. The error manifests itself while checking for the existence of a canonical 2-nice cycle. The erroneous behavior is when the system starts in the initial state with all cache lines in SHD state and owner[1] = owner[2] = 1, and then executes the following sequence of 12 events:

- 1.  $\langle ACKX, 2, 2 \rangle$
- $2. \langle UPD, 2 \rangle$
- 3.  $\langle ACKS, 1, 2 \rangle$
- 4.  $\langle ACKX, 2, 2 \rangle$
- 5.  $\langle ACKX, 1, 1 \rangle$
- 6.  $\langle UPD, 1 \rangle$
- 7.  $\langle UPD, 1 \rangle$
- 8.  $\langle W, 1, 1, 1 \rangle$
- 9.  $\langle R, 1, 2, 0 \rangle$
- 10.  $\langle UPD, 2 \rangle$
- 11.  $\langle W, 2, 2, 1 \rangle$
- 12.  $\langle R, 2, 1, 0 \rangle$

After event 2, owner[2] = 2, cache[1][2].s = INV, and cache[2][2].s = EXC. Now processor 1 gets a shared ack message  $\langle ACKS, 1, 2 \rangle$  for location 2. Note that in the erroneous previous version of the example, this event does not set owner[2] to 0. Consequently owner[2] = 2 and cache[2][2].s = SHD after event 3. An exclusive ack to processor 2 for location 2 is therefore allowed to happen at event 4. Since the shared ack message to processor 1 in event 3 is still sitting in inQ[1], cache[1][2].s is still INV. Therefore event 4 does not generate an INVAL message to processor 1 for location 2. At event 5, processor 1 gets an exclusive ack message for location 1. This event also inserts an INVAL message on location 1 in inQ[2] behind the ACKX message on location 2. After the UPD events to processor 1 in events 6 and 7, we have cache[1][1].s = EXC and cache[1][2].s = SHD. Processor 1 writes 1 to location 1 and reads 0 from location 2 in the next two events, thereby sending automaton  $Check_2(1)$  to the

state err. Processor 2 now processes the ACKX message to location 2 in the UPD event 10. Note that processor 2 does not process the INVAL message to location 1 sitting in inQ[2]. At this point, we have cache[2][1].s = SHD and cache[2][2].s = EXC. Processor 2 writes 1 to location 2 and reads 0 from location 1 in the next two events, thereby sending automaton  $Check_2(2)$  to the state err. Since there has been only one write event of data value 1 to each location, the run is accepted by  $Constrain_2(1)$  and  $Constrain_2(2)$  also.

Note that while checking for canonical k-nice cycles  $Constrain_k(j)$  has 2 states for all  $1 \le j \le k$  and 1 state for  $k < j \le m$ . Also  $Check_k(i)$  has 3 states for all  $1 \le i \le k$ . Therefore, by composing  $Constrain_k(j)$  and  $Check_k(i)$  with the memory system S(n, m, 2) we increase the state of the system by a factor of at most  $2^k \times 3^k$ . Actually, for all locations  $k < j \le m$  we are restricting write events to have only the data value 1. Therefore, in practice we might reduce the set of reachable states.

### 9 Related work

Descriptions of shared-memory systems are parameterized by the number of processors, the number of memory locations, and the number of data values. The specification for such a system can be either an invariant or a shared-memory model. These specifications can be verified for some fixed values of the parameters or for arbitrary values of the parameters. The contribution of this paper is to provide a completely automatic method based on model checking to verify the sequential consistency memory model for fixed parameter values. We now describe the related work on verification of shared-memory systems along the two axes mentioned above.

A number of papers have looked at invariant verification. Model checking has been used for fixed parameter values [MS91, CGH<sup>+</sup>93, EM95, ID96], while mechanical theorem proving [LD92, PD96] has been used for arbitrary parameter values. Methods combining automatic abstraction with model checking [PD95, Del00] have been used to verify snoopy cache-coherence protocols for arbitrary parameter values. McMillan [McM01] has used a combination of theorem proving and model checking to verify the directory-based FLASH cache-coherence protocol [KOH<sup>+</sup>94] for arbitrary parameter values. A limitation of all these approaches is that they do not explicate the formal connection between the verified invariants and shared-memory model for the protocol.

There are some papers that have looked at verification of shared-memory models. Systematic manual proof methods [LLOR99, PSCH98] and theorem proving [Aro01] have been used to verify sequential consistency for arbitrary parameter values. These approaches require a significant amount of effort on the part of the verifier. Our method is completely automatic and is a good debugging technique which can be applied before using these methods. The approach of Henzinger et al. [HQR99] and Condon and Hu [CH01] requires a manually constructed finite state machine called the serializer. The serializer generates the witness total order for each run of the protocol. By model checking

the system composed of the protocol and the serializer, it can be easily checked that the witness total order for every run is a trace of serial memory. This idea is a particular instance of the more general "convenient computations" approach of Katz and Peled [KP92]. In general, the manual construction of the serializer can be tedious and infeasible in the case when unbounded storage is required. Our work is an improvement since the witness total order is deduced automatically from the simple write order. Moreover, the amount of state we add to the cache-coherence protocol in order to perform the model checking is significantly less than that added by the serializer approach. The "test model checking" approach of Nalumasu et al. [NGMG98] can check a variety of memory models and is automatic. Their tests are sound but incomplete for sequential consistency. On the other hand, our method offers sound and complete verification for a large class of cache-coherence protocols.

Recently Glusman and Katz [GK01] have shown that, in general, interpreting sequential consistency over finite traces is not equivalent to interpreting it over infinite traces. They have proposed conditions on shared-memory systems under which the two are equivalent. Their work is orthogonal to ours and a combination of the two will allow verification of sequential consistency over infinite traces for finite parameter values.

### 10 Conclusions

We now put the results of this paper in perspective. Assumption 1 about causality and Assumption 2 about data independence are critical to our result that reduces the problem of verifying sequential consistency to model checking. Assumption 3 about processor symmetry and Assumption 4 about location symmetry are used to reduce the number of model checking lemmas to  $min(\{n,m\})$  rather than exponential in n and m.

In this paper, the read and write events have been modeled as atomic events. In most real machines, each read or write event is broken into two separate events —a request from the processor to the cache, and a response from the cache to the processor. Any memory model including sequential consistency naturally specifies a partial order on the requests. If the memory system services processor requests in order then the order of requests is the same as the order of responses. In this case, the method described in this paper can be used by identifying the atomic read and write events with the responses. The case when the memory system services requests out of order is not handled by this paper.

The model checking algorithm described in the paper is sound and complete with respect to a simple witness for the memory system. In some protocols, for example the *lazy caching* protocol [ABM93], the correct witness is not simple. But the basic method described in the paper where data values of writes are constrained by automata can still be used if ordering decisions about writes can be made before the written values are read. The lazy caching protocol has this property and extending the methods described in the paper to handle it is part of our future work. We would also like to extend our work to handle other

memory models.

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