

Accelerating Binarized Neural Networks via Bit-Tensor-Cores in Turing GPUs

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Abstract—Despite foreseeing tremendous speedups over conventional deep neural networks, the performance advantage of binarized neural networks (BNNs) has merely been showcased on general-purpose processors such as CPUs and GPUs. In fact, due to being unable to leverage bit-level-parallelism with a word-based architecture, GPUs have been criticized for extremely low utilization (1%) when executing BNNs. Consequently, the latest tensorcores in NVIDIA Turing GPUs start to experimentally support bit computation. In this work, we look into this brand new bit computation capability and characterize its unique features. We show that the stride of memory access can significantly affect performance delivery and a data-format co-design is highly desired to support the tensorcores for achieving superior performance than existing software solutions without tensorcores. We realize the tensorcore-accelerated BNN design, particularly the major functions for fully-connect and convolution layers — bit matrix multiplication and bit convolution. Evaluations on two NVIDIA Turing GPUs show that, with ResNet-18, our BTC-BNN design can process ImageNet at a rate of 5.6K images per second, 77% faster than state-of-the-art. Our BNN approach is released on <https://github.com/pnnl/TCBNN>.



1 INTRODUCTION

BINARIZED-neural-network (BNN) [1], [2], [3] is an alternative type of deep-neural-networks (DNNs). Compared to general DNNs, such as multi-layer-perceptrons (MLPs) and convolution-neural-networks (CNNs), the major difference of BNN is that it uses a single bit to represent each entry of the input and weight matrices. BNN evolved from DNN through binarized-weight-network (BWN) [4]. It was firstly observed that if the weight matrix can be binarized to +1 and -1, the floating-point (FP) multiplications can be degraded to addition (i.e., `mul +1`) and subtraction (i.e., `mul -1`). Later, it was further observed that if the input matrix can be binarized as well, then even the floating-point additions and subtractions in BWN can be degraded to logical operations (i.e., `xnor` for bit dot-product and `popc` for bit accumulation) [1], [2], [3].

BNNs bring several advantages over the full-precision DNNs: (a) *Reduced and simplified computation*. Through binarization, each segment of 32 FP fused-multiply-add (FMA) operations can be aggregated into an `xnor` operation and a `popc` operation, leading to theoretically 16× speedups; (b) *Reduced data movement and storage*. Through binarization, the whole memory hierarchy and network, including registers, caches, scratchpad, DRAM, NoC, etc. can accommodate 32× in both bandwidth and capacity; (c) *Reduced cost* which comprises energy reduction from simplified hardware design and smaller chip area; (d) *Resilience*. It has been reported that compared with differentiable DNNs, the discrete BNNs exhibit superior stability and robustness against adversarial attacks [5], [6].

On the flip side of the coin, binarization reduces the model's capacity and discretizes the parameter space, lead-

ing to certain accuracy loss. With the tremendous effort from the machine learning (ML) community [2], [7], [8], [9], accuracy of BNNs have been dramatically improved. The top-1 training accuracy of BNN-based AlexNet and ResNet-18 on ImageNet dataset has achieved 46.1% [8] and 56.4% [10] (54.3% and 61% with boosting [11]), with respect to 56.6% and 69.3% for full-precision DNN [12]. A latest BNN work even reported a top-1 accuracy of 70.7% [13].

Although BNN is not likely to substitute DNNs because of reduced model capacity, for many HPC [14], [15], [16] and cloud applications [17], [18], when certain accuracy levels can be achieved, alternative factors such as latency, energy, hardware cost, resilience, etc. become more prominent. This is especially the case for actual deployment [19].

Despite featuring various advantages, the expected performance gain of BNN has rarely been demonstrated on general purpose processors such as GPUs. This is mainly because: (i) the fundamental design mismatch between bit-based algorithms and word-based architecture; (ii) BNN designs at this stage are mainly driven by the algorithm community on how to improve the training accuracy; little system and architectural support have been provided on high performance delivery. Due to (i), most existing BNN implementations are realized as hardware accelerators (e.g., through FPGA [20], [21], [22], [23], [24], [25]) where the operand bit-width can be flexibly adjusted. Due to (ii), BNN developers are still relying on full-precision software frameworks such as TensorFlow and PyTorch over CPUs and GPUs to emulate the BNN execution. As a result, the lack of architectural & system support hinders the performance delivery and the general adoption of BNNs.

This situation has been lately changed for GPUs. On the software side, a recent work [26] proposed the binarized software tensor core, or BSTC, relying on GPU's low-level hardware intrinsics for efficient 2D bit-block processing, such as *bit matrix multiplication* (BMM) and *bit convolution* (BConv). On the hardware side, the latest NVIDIA Turing GPUs started to support BMM experimentally in their *Tensor*

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TABLE 1: Bit-Software-Tensor-Core (BSTC) [26] vs. Bit-Tensorcore (BTC). *uint32* refers to *unsigned int*. *uint64* refers to *unsigned long long int*. *INTU* refer to *integer units*. *SFU* refer to *special function units*.

	BSTC	BTC
Datatype	Bit (uint32, uint64)	Bit (uint32)
Functionality	Bit Matrix Multiplication	Bit Matrix Multiplication
Tile-A size	32×32 or 64×64	8×128
Tile-B size	32×32 or 64×64	128×8
Tile-C size	32×32 or 64×64	8×8
Hardware units	INTUs and SFUs	TensorCore Units (TCUs)
Processing level	per warp	per warp
GPU Platforms	Kepler or later (≥CC-3.0)	Turing GPUs (≥CC-7.5)

Core Units (TCUs) [27]. We label this new bit-capability as Bit-Tensor-Core, or BTC. Table 1 compares the major features of BSTC and BTC.

In this work, we focus on these bit-tensorcores in Turing GPUs and investigate how they can be fully leveraged for advanced performance delivery for BNNs. This paper thus makes the following major **contributions**: (i) To the best of our knowledge, this is the first work to investigate this brand new bit-computation capability of GPU tensorcores¹. We designed orchestrated microbenchmarks to investigate the low-level features of BTC. In particular, we observed that the value of stride exhibits considerable performance impact on memory fetch from the global memory via Warp-Matrix-Multiplication-API (WMMA). (ii) Based on our observations, we proposed a new bit data format specially for bit-computation on GPU tensorcores. We showed that without this new bit format, BTC might not exhibit performance advantage over existing software solutions; (iii) BTC currently only supports XOR-based bit-matrix-multiplication. In terms of convolution, traditional approaches [28], [29] that transform convolution to matrix-multiplication fail to work properly for BNNs due to the challenge in padding [30]. In this work, we propose a new approach that can fully leverage the bit-computation capability of BTC while effectively resolving this padding issue. We evaluated our design on two NVIDIA Turing GPUs, the results showed that our BTC-based BMM design could bring up to 4.4× speedup over the vendor’s *Cutlass* [31] implementation. Regarding BNN inference performance, compared with state-of-the-art solution [26], our BTC-based approach achieved on average 2.20× and 2.25× in latency, and 1.99× and 1.62× in throughput for VGG-16 and ResNet-18 on ImageNet. As bit-computation is increasingly common in many HPC and data-analytics scenarios [32], [33], [34], [35], [36], [37], our techniques can be extended to other applications.

2 RELATED WORK

We focus on the performance issues of BNN implementation and the GPU tensorcores in this section. Regarding the algorithm design for BNNs, please refer to this survey [30].

BNN Implementation The major purpose of BNN implementation is to leverage the system and architectural features of the platforms to satisfy the stringent latency and throughput constraints when deploying BNNs in HPC, cloud and embedded applications, while reducing the area and energy cost [20], [21], [22], [23], [24], [25], [39], [40], [41].

1. To the best of our knowledge, this feature has not appeared in vendor’s library like cuBLAS, cuDNN, TensorRT or other library up to now except *Cutlass* in which it is supported as an experimental, unverified function.

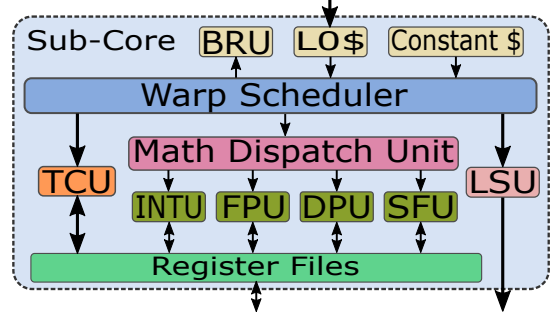


Fig. 1: A subcore of a Turing GPU SM. *BRU* is branch unit. *\$* refers to cache. *LSU* is the load-store-unit. *INTU* is the integer-unit. *FPU* is the floating-point-unit. *DPU* is the double-precision-unit. *SFU* is the special-function-unit [38]. *TCU* is the tensorcore-unit, which has its independent data path.

Most of these implementations focus on FPGA [20], [21], [22], [23], [24], [41] due to FPGA’s design flexibility at the bit level. Regarding general-purpose platforms, an existing CPU work [40] relies on the AVX/SSE vector instructions to derive good bit computation performance. It focuses on BMM and transforms Bconv to BMM through *im2col()* with costly pre- and post-processing. Another evaluation work [42] compares CPU, GPU, FPGA and ASIC based BNN designs, clarifying that the major performance restriction of CPUs and GPUs is *the extremely low utilization due to the challenge in extracting fine-grained parallelism*. Noticeably, the reported GPU utilization is 1% only [42]. To improve GPU utilization and extract bit-level-parallelism, a recent work [26] proposed the binarized-soft-tensor-core on top of GPU’s SMs and leverages low-level hardware intrinsics for harvesting the bit capability of GPUs. For BSTC, the performance gains from better utilization of the conventional integer/-logic units (i.e., INTUs and SFUs, see Figure 1). This work is different as we focus on the brand new bit computation capability of the latest Turing TCUs, and showcase how to gain the most performance from this new functional units.

GPU Tensorcore Driven by the demand of training large-scale DNNs, designing specialized low-precision dense matrix multiplication accelerators has become a popular trend. Particularly, Google presented *Tensor-Processing-Units* [43]; Intel announced the *Nervana Neural-Network-Processors* for tensor operations; NVIDIA integrated the *Tensorcore Units* into their Volta and Turing GPUs; Qualcomm included the *Hexagon-Tensor-Accelerator* into their Hexagon 855 chip.

This work focuses on the tensorcores of GPUs (see Figure 1). Since being firstly introduced in the Volta architecture [44], the tensorcore becomes one of the spot-light for GPGPU research. The relevant works can be summarized in two categories: (a) **Characterization**. In [45] and [46], Jia et al. dissected the Volta V100 and the Turing T4 GPUs through microbenchmarking. They depicted the detailed mapping mechanism from elements of a matrix tile to registers of a warp-lane in the HMMA instructions for FP16 matrix multiplication. They found that the 32 threads of a warp are essentially divided into 8 thread groups, where the 4 threads per group cooperatively work on the same regions of matrix *C* by fetching elements from different parts of matrix *A* and matrix *B*. Markidis et al. [47] studied the programmability, performance and precision of the Volta tensorcores and proposed a technique to compensate the accuracy loss due to precision degradation from FP32 to FP16. Raihan et al. [48] investigated the design details of the tensorcores in Volta and Turing GPUs and built

an architecture model for the tensorcores in GPGPU-Sim. They characterized the WMMA APIs and clarified how the operand sub-matrix elements were mapped for FP16 GEMM in Volta tensorcores, and FP16/Int8/Int4 GEMM in Turing tensorcores. However, they did not investigate the 1-bit computation mode. Hickmann and Bradford [49] proposed a testing method for assessing the compliance of IEEE standard, hardware microarchitecture, and internal precision of the Volta tensorcores. **(b) Application.** Haidar et al. [50] proposed a mixed-precision iterative refinement method to approach FP64 precision using FP16-based GPU tensorcores in LU factorization, acting as the first effort to apply GPU tensorcores for non-machine-learning applications. Sorna et al. [51] applied FP16 tensorcores for FFT acceleration. Blanchard et al. [52] thoroughly analyzed the rounding error of matrix multiplication and LU factorization when using the tensorcores. Dakkak et al. [53] showed that the tensorcores, which were originally designed for 2D FP16 GEMM, can be adopted for 1D array reduction and scan.

Most of these works, however, focused on FP16 mixed-precision matrix-multiply in Volta tensorcores. They either evaluated their performance, programmability, accuracy, hardware design, or looked into alternative applications other than GEMM, aiming to preserve higher precision. None of them have investigated the latest bit computation capability of the GPU tensorcores. In addition, no existing works, to the best of our knowledge, have ever reported the potential performance impact from the stride of segmented memory load, and how to circumvent the challenges in accelerating convolutions through the tensorcores. Furthermore, until writing the paper, we have not seen any works leverage GPU tensorcores for the acceleration of BNs.

3 GPU BIT TENSORCORES

3.1 GPU Tensorcores

Since the Volta architecture (CC-7.0), NVIDIA GPUs have introduced a novel type of function units known as *Tensorcores* into the streaming multiprocessors (SMs) for accelerating low-precision general matrix multiplication (GEMM). In Volta, each tensorcore processes 64 FP16 FMA operations per cycle [54]. The only supported datatype for Volta tensorcores is FP16. For Turing (CC-7.5), more datatypes are supported, including FP16, signed/unsigned int-8, int-4, and recently a bit as well. Please refer to [45], [48], [54] for more hardware details about Volta and Turing TCUs.

3.2 CUDA WMMA

Since CUDA Runtime-9.0, the *Warp Matrix Multiplication API* (WMMA) has been introduced for operating the tensorcores in Volta and Turing GPUs. The idea is to partition the three input and one output matrices into tiles, where each warp processes the multiplication of one tile ($T_D = T_A \times T_B + T_C$). WMMA provides the necessary primitives to operate on the bit-tiles (e.g., loading input tiles, tiled multiplication, storing output tile): *load_matrix_sync*, *mma_sync*, *store_matrix_sync*. These primitives are executed by the 32 threads of a warp cooperatively. For FP16, the tile is further partitioned into 32 fragments while each thread fetches a fragment of data into its register files. Although

```
1 namespace experimental {
2   namespace precision { struct b1; } // define 1-bit datatype
3   enum bmmaBitOp { bmmaBitOpXOR = 1 }; //only XOR is supported as the mul-op for BTC
4   enum bmmaAccumulateOp { bmmaAccumulateOpPOPC = 1 }; } //popc acts as the acc-op for BTC
```

Listing 1: WMMA 1-bit definition and operations in *crt/mma.h*

```
1 wmma.load.a.sync.aligned.row.m8n8k128.global.b1 {%r21}, {%rd8}, %r20; //load_matrix_sync()
2 wmma.load.b.sync.aligned.col.m8n8k128.global.b1 {%r22}, {%rd5}, %r20; //load_matrix_sync()
3 wmma.load.c.sync.aligned.row.m8n8k128.global.s32 [%rd30], {%r55,%r64}, %r60; //load_matrix_sync()
4 wmma.mma.xor.popc.sync.aligned.row.col.m8n8k128.s32.b1.b1.s32 {%r23,%r24}, {%r21}, {%r22},
5   {%r19,%r19}; //bmma_sync()
6 wmma.store.d.sync.aligned.row.m8n8k128.global.s32 [%rd34], {%r63,%r64}, %r60; //store_matrix_sync()
```

Listing 2: PTX code for Bit-Matrix-Multiply-API (BMMA)

the vendor’s official documents have not revealed the exact mapping schemes, existing works have figured them out through microbenchmarking [45], [48].

3.3 Cutlass Library

Currently the vendor’s high-performance linear-algebra library *cuBLAS* has not supported BMM on Turing tensorcores. However, their open-source GEMM library – *Cutlass* [31] has integrated it as an experimental and non-verified feature. BMM is realized using the WMMA API. The input matrix A is in row-major bit format (compacted as 32-bit unsigned int), B is in column-major bit format (also compacted as 32-bit unsigned int). The accumulated input matrix C and the result matrix D are in row-major 32-bit signed int format. C and D are usually the same matrix. BMM in *Cutlass* conducts 0/1 dot-product while BNN demands +1/-1 dot-product, as will be discussed later.

4 BTC CHARACTERIZATION

To operate on the bit datatype for Turing GPUs, CUDA WMMA defines the 1-bit precision and the bit operations in an independent “*experimental*” namespace, as listed in Listing 1. XOR and POPC for bits (+1/-1) correspond to multiply and accumulate for floating-point/integer datatypes.

Five APIs are provided for loading the bit-tile A , the bit-tile B , the int-tile C , and storing the int-tile D , as well as the multiplication: $D = C + A \times B$. For the bit-matrix-multiply-API (BMMA), only a single computation paradigm is defined: the bit-tile A is in row-major of size (8, 128); the bit-tile B is in column-major of size (128, 8); the int-tile C and D are square matrices in row-/column-major of size (8, 8). The bit-tile A and B are compacted as 32 unsigned ints, each with 32 bits. Therefore, the bit-tile A and B each occupies 128 bytes. The int-tile C and D each occupies $8 \times 8 \times 4 = 256$ bytes. Listing 2 shows the *Parallel Thread Execution* (PTX) – the low-level GPU virtual machine ISA code for the five BMMA APIs. The shape qualifier “m8n8k128” in Line 2-6 indicate that the bit-tile-multiplication processed per warp is in size (8,128) \times (128,8)=(8,8). “sync” means the instruction wait for all warp lanes to synchronize [55] before proceeding. The “layout” qualifier specifies if the tile is stored with a row-major or column-major order in memory. “type” indicates the precision of the tile. Using int32 for tile- C and D is to avoid potential overflow during the accumulation. For matrix-multiplication, tile- C and D are usually in the same size. Thus, the five APIs can be grouped into three set: *load*, *store*, and *computation*. We investigate each of them in the following to figure out potential design guidelines. Regarding the hardware platform, see Section 7 and Table 2.

4.1 BMMA Load

We first concentrate on *bmma_load*, as memory load is the most crucial factor for GEMM on GPU [56]. The load API is

```
1 void load_matrix_sync (fragment<...> &tileA, const T* mptr, unsigned ldm, layout_t layout);
```

It waits for all the threads of a warp to arrive, and then loads a bit tile (i.e, a matrix fragment) from the device memory. It has three parameters. "*mptr*" is a 256-bit aligned pointer pointing to the first element of the matrix in memory. The memory here can be global or shared memory. "*layout*" can be row- or column-major, but for BMMA, there is only a single choice — *mem_row_major* for matrix-A and *mem_col_major* for matrix-B. "*ldm*" is the stride in element between consecutive rows (in row major) or columns (in column major) and must be a multiple of 16 bytes), according to [57]. We find that for shared memory, this is the case; but for global memory, a multiple of 32 is also feasible (despite with unpredicted results). To see the impact of *mptr* (i.e., memory type) and *ldm* on the performance of the load primitive, we measure its average per-thread latency using the `clock()` instruction. We add a memory fence operation before the measurement to ensure that the data fetching has finished.

Figure 2, 3, 4, 5 show the average latency with respect to different values of *ldm* for *load_matrix_sync()* on global and shared memory of RTX-2080 and RTX-2080Ti GPUs. As *ldm* is the stride between consecutive rows of the matrix, it should be application dependent (e.g., for a $1024 \times 1024 \times 1024$ BMM, *ldm* should be 1024) and the raw latency should be irrelevant to *ldm*. However, counterintuitively it has a strong impact on the performance of fetching a bit-tile from the global memory. As can be seen in Figure 2 and Figure 4, *ldm*=128 and 384 exhibit the shortest latency. Regarding shared memory, (1) accessing shared memory shows more than $5 \times$ less latency than global memory; (2) the latency for RTX2080Ti shared memory access is less than RTX2080, and is unchanged with *ldm*.

We then consider "*tileA*", and see how the bit-tile (128×8 bits) is distributed among the lanes of a warp. Similar to [48], we let each lane print out the value of data it fetches. Based on the value, we can identify the mapping mechanism. We find that, similar to FP16 and Int8, lanes in BMMA also establish 8 thread groups — 4 consecutive lanes per group. Each thread group corresponds to a 128 bit row. Within a 128 bit row, each lane accounts for a 32-bit portion (4 bytes). This partially explains why *ldm*=128 delivers the shortest latency: the 32 lanes of the warp constitute a coalesced memory access, where the 32 4-byte access are merged as a single memory request. Regarding why *ldm*=384 also exhibits good performance, we suspect this might be because the Turing L1 data cache is essentially partitioned into two sectors with independent ports, similar to the L1/texture cache in Maxwell and Pascal GPUs [58]. It conserves the data in an interleaving way at a step of 32 bytes. Consequently, *ldm*=256 (32B) may trigger a sector-port conflict for simultaneous memory fetches from the same warp but *ldm*=384 may not. This is confirmed by the observation that *ldm*=128+256X (e.g., 384, 640, 896) all demonstrate relatively low latency in Figure 2 and 5.

4.2 BMMA Store

The store operation is different from the load operation in that each element is a 32-bit signed integer. The store API is:

```
1 void store_matrix_sync (T* mptr, const fragment<...> &tileC, unsigned ldm, layout_t layout);
```

Again, it waits until all warp lanes arrived before storing *tileC* into memory. "*mptr*" must be a 256-bit aligned pointer referring to the first element. "*ldm*" describes the stride in elements between consequent rows in C, and must be a multiple of 16 bytes (with integer, it corresponds to 4 elements). "*layout*" can be row-major or column-major.

We measure the average latency with respect to the stride *ldm* on global and shared memory of RTX-2080 and RTX-2080Ti GPUs, as shown in Figure 6, 7, 8, 9, respectively. Unlike load, the latency histograms for store do not exhibit obvious patterns. We also attempt to investigate how the resulting int-tile *tileC* is distributed among the lanes. Our findings show that: (i) If it is row-major, then within the 8×8 int tile, each two consecutive elements (from a row) are stored in two adjacent registers of a lane. For example, suppose the 8×8 elements are E0 to E63 and each lane uses R4 and R5 to store the integer tile, then (E0, E1) are stored in R4 and R5 of lane-0, (E2, E3) are stored in R4 and R5 of lane-1, and so on. (ii) If it is column-major, then each two consecutive elements (from a column) are stored in two adjacent registers of a lane (i.e., transposed from the row-major layout). When storing, the two adjacent registers are encoded as one `STG.E.64` memory store for the entire warp, as if storing an FP64 data.

4.3 BMMA Computation

Finally, we discuss the bit-matrix-multiply API:

```
1 void bmma_sync(fragment<...> &tileD, const fragment<...> &tileA,  
2 const fragment<...> &tileB, const fragment<...> &tileC,  
3 experimental::bmmaBitOp=experimental::bmmaBitOpXOR,  
4 experimental::bmmaAccumulateOp=experimental::bmmaAccumulateOpPOPC);
```

It waits until all lanes are available for conducting the BMMA operation: $\text{tileD} = \text{POPC}(\text{tileA} \text{ XOR } \text{tileB}) + \text{tileC}$. Unlike the condition for FP16 and Int8 where a group of SASS assembly operations are generated [45], [46], [48], *bmma_sync* is only translated into a single SASS code:

```
1 BMMMA.S6128.XOR.POPC R2, R8.ROW, R9.COL, R2 ;
```

Our idea here is to measure its raw latency and estimate how much parallelism, including warp-level-parallelism (WLP) and instruction-level-parallelism (ILP), are required to saturate the tensorcore pipeline and hide the latency.

Figure 10, 11, 12, 13 illustrate the total latency of increasing the number of repeated *bmma_sync* operations for the same *tileC*/*tileD*, and different *tileC*/*tileD* on the two GPUs. The raw latency of *bmma_sync* is ~ 201 cycles on RTX2080 and ~ 190 cycles on RTX2080Ti. As shown in the figure, the incremental latency with each one more *bmma_sync* operation is 10 cycles when *tileC* & *tileD* are identical for all operations, and is 4 cycles when *tileC* & *tileD* are different on both platforms. This implies that the pipeline stage delay is around 4 cycles. When using the same accumulator, 6 extra cycles are needed. Given the raw latency of ~ 200 cycles, and the fact that Turing GPU SM comprises four sub-cores (each subcore can issue one instruction per cycle), with at maximum 32 warps per SM for Turing (so WLP=32), we

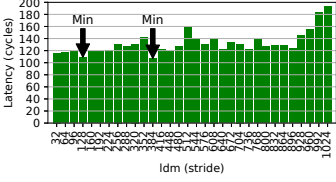


Fig. 2: RTX2080 global mem load

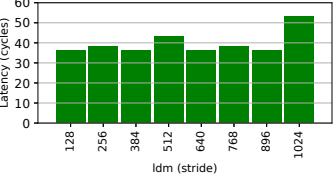


Fig. 3: RTX2080 shared mem load

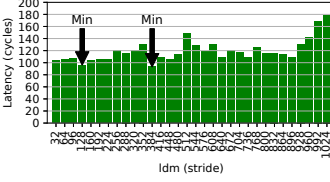


Fig. 4: RTX2080Ti global mem load

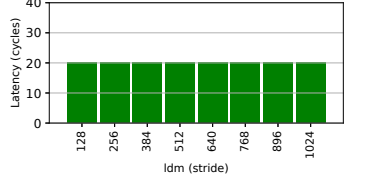


Fig. 5: RTX2080Ti shared mem load

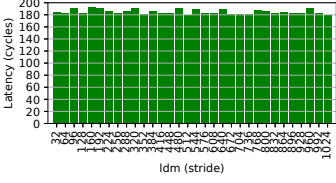


Fig. 6: RTX2080 global mem store

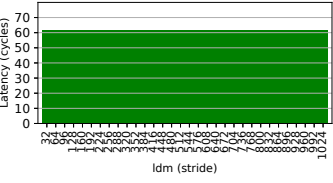


Fig. 7: RTX2080 shared mem store

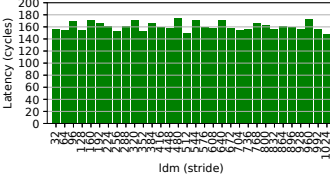


Fig. 8: RTX2080Ti global mem store

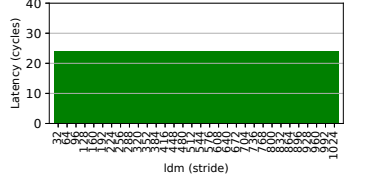


Fig. 9: RTX2080Ti shared mem store

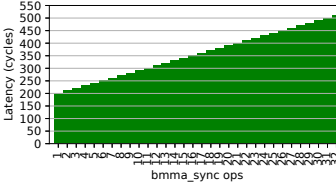


Fig. 10: RTX2080 bmma w/ same C

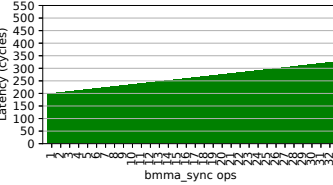


Fig. 11: RTX2080 bmma w/ diff C

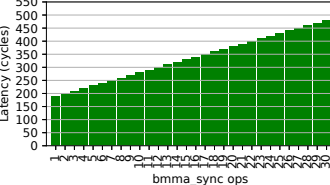


Fig. 12: RTX2080Ti bmma w/ same C

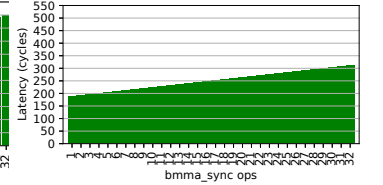


Fig. 13: RTX2080Ti bmma w/ diff C

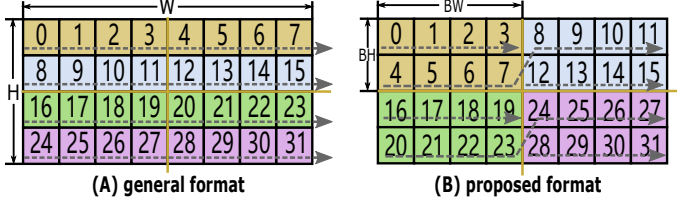
roughly require $ILP=200/4 \times 4/32 \approx 7$ to saturate the entire tensorcore pipeline. In other words, with 8 independent *bmma_sync* operations, we should approach the theoretical computation bandwidth of the tensorcores.

5 BMM AND BCONV WITH BTC

We present our designs for BTC-based BMM and BConv, which are the core functions for the fully-connected layer and convolution layer of BNNs.

5.1 FSB Data Format for BTC

In Section 4.1, we have observed that the value of *ldm* can strongly affect the performance of *load_matrix_sync* from global memory, where *ldm*=128 and 384 exhibit the best performance. Our idea thus is whether we can essentially fix the value of *ldm* firmly to 128 or 384. As a result, rather than storing the bits completely sequential and using the matrix width for *ldm*, as practiced by the *Cutlass* library and suggested by CUDA programming guide, we propose a new 2D bit data format where bits are stored in a unit of 128×8 bit-tile. An analogous example is shown in Figure 14. From the 1D general format to the 2D new format, an array of 8×4 bits ($H=4, W=8$) is converted with a tile size of 4×2 ($BH=2, BW=4$). For BTC, since 384 is not a power of 2, dividing 384 may incur troublesome remainder handling, we thus use 128 as BW and 8 as BH for the new format. If the original bits are organized in row-major, both the in-tile and tile-wise order of the new format are in row-major (as the case in Figure 14); otherwise, both are organized in column-major. Since the new format only changes the way how bits are stored and fetched, no extra space is needed. However, if the width of the original matrix (i.e., *W*) can not be divided by 128 (i.e., BW), for the convenience of index calculation, we pad the row to be a factor of 128, which may occupy some extra space. Note, in order to load via *load_matrix_sync()*, such a kind of padding is required anyway. Similar requirement has been imposed by *pitch*

Fig. 14: Fixed-Stride-Bit (FSB) format based on a tile of $BH \times BW$.

in *cudaMemcpy2D()*. The temporal overhead only occurs at array index calculation, which is almost negligible.

5.2 BMM for FC Layer

BMM in BNN is different from GEMM because: (a) *Input*. The elements of matrix-A and B are binary values: +1 and -1. A normal floating-point or int number is binarized via:

$$x^b = \text{sign}(x) = \begin{cases} 1 & \text{if } x \geq 0 \\ -1 & \text{otherwise} \end{cases} \quad (1)$$

In an FC layer, both A and B have to be binarized ahead of BMM. However, the binarization of B (i.e., weights) can be performed offline after the training; only the binarization of A is in the critical path of inference. Existing work has shown that such a binarization can be achieved efficiently through the `__ballot()` function of GPUs [26]; (b) *Computation*. The dot-product of GEMM is $y_{i,j} = \sum_{k=0}^{n-1} a_{i,k} b_{k,j}$ where *n* is the vector length. In terms of BMM, as *a* and *b* become bit-vectors, if using bit-1 to denote +1, and bit-0 to denote -1, it can be shown that the ± 1 dot-product becomes:

$$v = \vec{a} \cdot \vec{b} = n - 2 \times \text{popc}(\vec{a} \text{ xor } \vec{b}) = 2 \times \text{popc}(\vec{a} \text{ xnor } \vec{b}) - n \quad (2)$$

where *n* is the bit-vector length. *xor* and *xnor* are logical exclusive-or and exclusive-nor. The *xnor* expression has widely been used for BNN algorithm research [1], [3] and FPGA/ASIC implementation [20], [21] while GPU tensorcores currently only support *xor* for BMM computation. *popc* stands for population count, which counts the number of bit-1s in the bit vector. (c) *Output*. The elements of the output matrix-C are full-precision integer values. However, in an FC layer, it can be binarized after a threshold operation

```

1 __global__ void BMM(unsigned -A, unsigned -B, int -C, int A_height, int A_width, int B_width) {
2   using namespace nvcuda::wmma::experimental;
3   int bx = blockDim.x * blockDim.y; int by = blockDim.y;
4   wmma::fragment<wmma::matrix_a, 8, 8, 128, precision::b1, wmma::row_major> a_frag; //tile A
5   wmma::fragment<wmma::matrix_b, 8, 8, 128, precision::b1, wmma::col_major> b_frag; //tile B
6   wmma::fragment<wmma::accumulator, 8, 8, 128, int> c_frag; wmma::fill_fragment(c_frag, 0); //tile C
7   for (int i=0; i < (A_width/128); i++) {
8     load_matrix_sync(a_frag, A+bx*8-A_width/32+i*128/32, A_width); //fetch tile A
9     load_matrix_sync(b_frag, B+by*8-A_width/32+i*128/32, A_width); //fetch tile B
10    bmma_sync(c_frag, a_frag, b_frag, c_frag); //BMM
11    for (int i=0; i < c_frag.num_elements; i++) c_frag.x[i] = A_width-2-c_frag.x[i]; //fix for +1/-1 logic
12    store_matrix_sync(C+(bx*8-B_width+by*8), c_frag, B_width, wmma::mem_row_major); //store tile C
13  }
14  BMM <<< dim3(A_height/16, B_width/8), dim3(32, 2) >>> (...); //invoke BMM kernel

```

Listing 3: BMM baseline implementation

```

1 __global__ void BMM(unsigned -A, unsigned -B, int -C, int A_height, int A_width, int B_width) {
2   using namespace nvcuda::wmma::experimental;
3   __shared__ uint4 As[32], Bs[32]; //buffering (8*128)-8 bit block in shared memory
4   const int laneid = threadIdx.x; const int wx = threadIdx.y; const int wy = threadIdx.z; //tile index
5   const int bx = blockDim.x; const int by = blockDim.y; //block index
6   wmma::fragment<wmma::matrix_a, 8, 8, 128, precision::b1, wmma::row_major> a_frag; //tile A
7   wmma::fragment<wmma::matrix_b, 8, 8, 128, precision::b1, wmma::col_major> b_frag; //tile B
8   wmma::fragment<wmma::accumulator, 8, 8, 128, int> c_frag; wmma::fill_fragment(c_frag, 0); //tile C
9   for (int k=0; k < A_width; k++) {
10    if (wx==0 && wy==0) { //one warp fetches data into shared memory for 16 warps of a thread block
11      As[laneid] = (uint4*)A[(bx*32+laneid)-A_width+k]; Bs[laneid] = (uint4*)B[(by*32+laneid)-B_width+k];
12    }
13    __syncthreads(); //for respecting RAW dependency
14    load_matrix_sync(a_frag, &As[wx*8], 128); load_matrix_sync(b_frag, &Bs[wy*8], 128);
15    bmma_sync(c_frag, a_frag, b_frag, c_frag);
16    __syncthreads(); //for respecting WAR dependency
17    for (int i=0; i < c_frag.num_elements; i++) c_frag.x[i] = (A_width-128)-(2-c_frag.x[i]); //+1/-1 BMM
18    store_matrix_sync(C+(bx*8+wx)-8-B_width+(by*4+wy)-8, c_frag, B_width, wmma::mem_row_major);
19  }
20  BMM <<< dim3(A_height/32, B_width/32), dim3(32, 4) >>> (...);

```

Listing 4: Bit-Matrix-Multiplication

(discussed later), reducing memory access. Therefore, the third difference with GEMM is that the output-C can be binarized before the store.

Design-1 Now we present our three BMM designs based on WMMA, which is the only API for operating the tensor-cores. The baseline design is shown in Listing 3. Each thread block comprises two warps and each warp processes BMM for a 128×8 bit-tile in Line 10. Having two warps per thread block is for achieving the full occupancy of Turing SMs [59].

Design-2 As memory load is the most important factor for matrix multiplication on GPU [56], Design-2 aims at improving the efficiency of memory load. On one hand, using a whole warp to fetch only 128 bits is too lightweight. On the other hand, if coalescing memory access is enforced with each lane fetches 32bits, the total bit length becomes $32 \times 4 \times 8 = 1024$ bits, which is probably too coarse-grained for a BNN FC layer given the matrix size is usually less than 2048. Therefore, motivated by [45], we increase the load granularity per warp-lane to its max value of 128 bits, leveraging the effective LDG.E.128 SASS instruction. With each lane fetching 128 bits, a warp of 32 lanes would fetch a bit segment of 4096 bits, which is sufficient for 4 warps to perform WMMA simultaneously. As a result, we use a representative warp to fetch 4096 bits of A and 4096 bits of B from global memory to shared memory, which are then dispatched to 16 warps for WMMA execution, as listed in Listing 4. Essentially, each thread block processes a BMM of $(128, 32) \times (32, 128)$ while each warp processes $(128, 8) \times (8, 128)$. Line 11-12 show how to invoke 128-bit global memory load through vectorization [45]. Note that `load_matrix_sync` is $5 \times$ faster on shared memory than global memory (Section 4.1).

Design-3 We adopt our new FSB format for BMM. Listing 5 shows the design with the output matrix binarized. As can be seen, after BMM, each warp holds a tile of C in size of 8×8 . We use `__ballot()` to binarize the 64 elements using the entire 32 lanes in Line 17-18. In order to write an 8-bit

```

1 #define FLIPBITS(n,b) ((n)^(1u<<(b)-1)) //flip the last b bits of n
2 __global__ void BMMb(unsigned -A, unsigned -B, unsigned -C, int A_height, int A_width, int B_width) {
3   using namespace nvcuda::wmma::experimental;
4   int bx = blockDim.x * blockDim.y; int by = blockDim.y;
5   __shared__ int Cs[64];
6   unsigned laneid; asm("mov.u32 %0, %%laneid;" : "=r" (laneid)); //get laneid
7   wmma::fragment<wmma::matrix_a, 8, 8, 128, precision::b1, wmma::row_major> a_frag; //tile A
8   wmma::fragment<wmma::matrix_b, 8, 8, 128, precision::b1, wmma::col_major> b_frag; //tile B
9   wmma::fragment<wmma::accumulator, 8, 8, 128, int> c_frag; wmma::fill_fragment(c_frag, 0); //tile C
10  for (int i=0; i < (A_width/128); i++) {
11    load_matrix_sync(a_frag, A+bx*8-A_width/32+i*128/32, A_width); //fetch tile A
12    load_matrix_sync(b_frag, B+by*8-A_width/32+i*128/32, A_width); //fetch tile B
13    bmma_sync(c_frag, a_frag, b_frag, c_frag); //BMM
14    for (int i=0; i < c_frag.num_elements; i++) c_frag.x[i] = A_width-2-c_frag.x[i]; //fix for +1/-1 logic
15    store_matrix_sync(Cs, c_frag, B_width, wmma::mem_row_major); //store tile C
16    union{ unsigned data; uchar elements[4]; } p0, p1;
17    p0.data = __ballot(A_width-2-Cs[laneid] >= 0);
18    p1.data = __ballot(A_width-2-Cs[laneid+32] >= 0);
19    if (laneid < 4) { uchar Cb = (uchar)&Cs[0];
20      Cb[(bx*8+laneid)-(B_width/8)+FLIPBITS(by, 2)] = p0.elements[3-laneid];
21      Cb[(bx*8+4+laneid)-(B_width/8)+FLIPBITS(by, 2)] = p1.elements[3-laneid];
22    }
23  }
24  BMMb <<< dim3(A_height/16, B_width/8), dim3(32, 2) >>> (...); //invoke BMMb kernel

```

Listing 5: BMM in new format with binarized output

```

1 __global__ void BTC_Conv2d(const unsigned -__restrict__ input,
2   const unsigned -__restrict__ filter, int - output, const int in_channels, const int out_channels,
3   const int in_width, const int in_height, const int filter_width, const int filter_height,
4   const int batch, const int stride_vertical, const int stride_horizontal, const int out_width,
5   const int out_height, const int pad_h, const int pad_w) {
6   using namespace nvcuda::wmma::experimental;
7   wmma::fragment<wmma::matrix_a, 8, 8, 128, precision::b1, wmma::row_major> a_frag;
8   wmma::fragment<wmma::matrix_b, 8, 8, 128, precision::b1, wmma::col_major> b_frag;
9   wmma::fragment<wmma::accumulator, 8, 8, 128, int> c_frag;
10  unsigned laneid; asm("mov.u32 %0, %%laneid;" : "=r" (laneid)); //get laneid
11  const int bx = blockDim.x; //over Q: out_width
12  const int by = blockDim.y; //over P: out_height
13  const int bz = blockDim.z; //over O: out_channel/8 * batch/8
14  const int ins = (in_channels > 7); //number of steps in C: in_channels
15  const int bn = bz/(out_channels > 3); //batch
16  const int bo = bz/(out_channels > 3); //out_channel
17  //coord (ax, ay) in Input from bx, by in Output
18  const int ax0 = bx-stride_horizontal-pad_w; const int ay0 = by-stride_vertical-pad_h;
19  int exclude = 0; wmma::fill_fragment(c_frag, 0); //track the number of filter entries that are masked off
20  for (int r=0; r < filter_height; r++) { //load a window of data from input
21    for (int s=0; s < filter_width; s++) {
22      const int ay = ay0 + r; //y-coord in Input
23      const int ax = ax0 + s; //x-coord in Input
24      if ((ay >= 0) && (ay < in_height) && (ax >= 0) && (ax < in_width)) { //within Input frame
25        for (int c=0; c < ins; c++) { //per 128-bit in C: in_channels
26          //input: [H,W,N,C], filter: [K,K,O,C]
27          load_matrix_sync(a_frag, &input[(ay-in_width+ax)-batch-ins*4+bn-ins*32+c*4], in_channels);
28          load_matrix_sync(b_frag, &filter[(r-filter_width+s)-out_channels-ins*4+bo-ins*32+c*4], in_channels);
29          bmma_sync(c_frag, a_frag, b_frag, c_frag);
30        }
31        else exclude++; //accumulate for points not in frame
32      }
33    }
34    for (int i=0; i < c_frag.num_elements; i++)
35      c_frag.x[i] = in_channels-filter_height-filter_width - exclude-in_channels - (2-c_frag.x[i]);
36    //output: [P,Q,N,O] => [by,bx,bn,bo]
37    store_matrix_sync(&output[(by-out_width+bx)-batch-out_channels + bn*8-out_channels + bo*8],
38      c_frag, out_channels, wmma::mem_row_major);
39  }

```

Listing 6: BTC-based BConv design

uchar to a 32-bit unsigned, we define a union for packing and unpacking. As NVIDIA GPUs adopt little endian, we define `FLIPBIT()` for efficient byte-index translation.

5.3 BConv for Convolution Layer

The convolution operation here is to cross-correlate a 4D input tensor (*batch, input_height, input_width, input_channels*) with a 4D weight tensor (*weight_height, weight_width, input_channels, output_channels*). We use H to denote input_height, W to denote input_width, N to denote batch, C to denote input_channel, K to denote weight size and O to denote output_channel. *TensorFlow* thus uses NHWC for input and KKCO for filter. *PyTorch* uses NCHW for input and OCKK for filter. Traditionally, a 2D convolution can be transformed into GEMM through the *im2col()* process [28], [29], which can then be accelerated by the tensorcores. However, for BConv, directly converting to BMM is not feasible due to the challenge in padding [30]. Different from normal convolution where the padded zeros shall not affect the correctness, in BConv an element zero actually denotes -1. Therefore, after the *im2col()* process, we are unable to distinguish the padded 0s from the meaningful zeros representing -1, leading to inaccurate convolution results.

Thus, the objective here is how to design BConv so that the padding issue can be well-managed but at the same

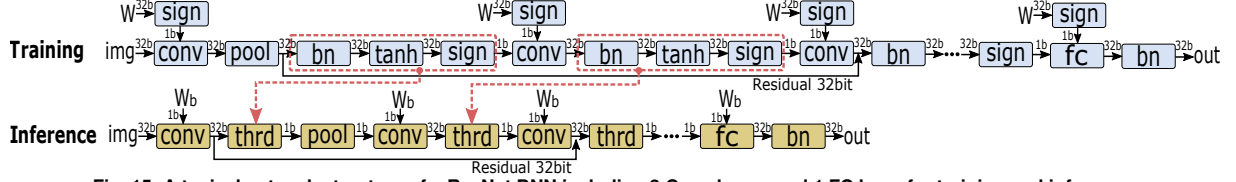


Fig. 15: A typical network structure of a ResNet BNN including 3 Conv layers and 1 FC layer for training and inference.

time can still be accelerated by the bit tensorcores of Turing GPUs. On one hand, motivated by existing work [26], if the entire filter window is processed sequentially by a single GPU thread, a status variable can be allocated to track how many entries of the filter window fall out of the frame of the input image, which can be used later to make an amendment accordingly for ensuring the correctness of bit-padding. On the other hand, if we ignore the image size and filter size for now but looking at a particular point $[i,j]$ of the input image, the batch of N images at that point cross-correlating with an entry of the filter window $[r,s]$ is essentially to calculate the following output point $[p,q]$:

$$Output_{[p,q]} = \sum_{k=1}^C input(N, k)_{[i,j]} \times filter(k, O)_{[r,s]} \quad (3)$$

This is just equivalent to multiplying a bit matrix in size (N, C) with another matrix in size (C, O) , which can be performed by the bit-tensorcores. Consequently, our idea is to change the input tensor to $HWNC$, the filter tensor to $KKCO$, and perform BMM along their last two dimensions.

Our first design is shown in Listing 6. We use each warp to traverse the input_channel space at Line 28 and perform the computation for 8 input_images over 8 output_channels (i.e., $(8, C) \times (C, 8)$) using the bit-tensorcores in Line 30-32. We use "exclude" to track the number of entries outside the filter frame at Line 33 and amendment the results at Line 36 for padding and the ± 1 logic (see Eq 2). We use c_frag for storing the partial results of convolution. Eventually, the 8×8 resulting matrix tile stored in c_frag is written back to the global memory in row-major at Line 38-39.

Our second BConv design leverages the new bit data format. We reform the last two dimensions of the input tensor (N, C) in a bit-tile of 128×8 bits in row-major, and the filter tensor (C, O) in a bit-tile of 128×8 bits in column-major. Then, we can adjust the ldm in Line 30-31 from "in_channels" to 128, later we will show the impact of this adjustment.

6 BNN DESIGN WITH BTC

6.1 BNN Network Structure

Figure 15 illustrates the network structure of an example ResNet. To avoid losing too much non-recoverable information at the beginning, if the input images are in full-precision (e.g., after preprocessing), the first layer of BNN is not binarized [2], [3], [7]. BWN is adopted here in which only the weight matrix is binarized. Consequently, we are unable to use BTC to accelerate the first layer. Also because the input channels of the first layer is usually very small (e.g., red, green, blue), to avoid alignment issue and fully leverage data locality, we binarized the weight matrix into a 4D bit tensor in $KKCO$ format and buffer the weight into the shared memory for reuse. Then, by extracting each bit of the weight, depending on whether it is 1 or 0, we add or subtract the corresponding element of the input matrix.

The output matrix is binarized and stored in particular bit-format as the input for the next layer.

Shown in Figure 15, regarding training, a BNN convolution layer typically comprises *binarization* (sign), *bit-convolution* (conv), *batch-normalization* (bn), *hard-tanh* (tanh), and *pooling* (pool). Binarization is the sign function following Eq 1. Batch-normalization [60] is to reduce the batch noise:

$$y_{i,j} = \left(\frac{x_{i,j} - \mathbb{E}[x_{*,j}]}{\sqrt{Var[x_{*,j}] + \epsilon}} \right) \cdot \gamma_j + \beta_j \quad (4)$$

Note that bn is essential for BNNs, as missing it will render the training unable to converge. Additionally, having bn brings two extra benefits: (1) bias is thus not necessary for the bit convolution or fully-connected layer, as bias can be integrated with β_j in Eq 4; (2) the scaling layer proposed in [3], [7] for BNN is also not necessary as it can be integrated with γ_j in Eq 4. Hard tanh is a piecewise linear function:

$$Htanh(x) = Clip(x, -1, 1) \quad (5)$$

Since tanh is immediately followed by the sign function, it has none effect on inference or the forward pass of training. The major purpose of tanh is to constrain the gradient of the sign function between -1 and +1 in the backward pass [1]. Otherwise, if the full-precision activation is too large, the gradient will be zeroed-out. Additionally, since the sign binarization function has already imposed non-linearity into the network, no other activation function such as *ReLU* [3] and *PReLU* [7] is actually needed for BNN. Conversely, extra activation functions might be harmful based on our tests.

Regarding the order of these unit functions, it should be $tanh \rightarrow sign \rightarrow bconv \rightarrow pool \rightarrow bn \rightarrow tanh \rightarrow sign$ for the training, as it has already been shown that placing pool before bn can lead to increased training accuracy [3], [30]. However, for inference it would be much faster if equivalently pool is located after bn and even the binarization of the next layer to convert a max pooling into a logic-OR operation [21], [26]. Additionally, for inference, bn and sign of the next layer can be aggregated as a simple threshold comparison operation (i.e., returns +1 if greater than a threshold τ and -1 otherwise) [21], [26], labeled as thrd in Figure 15. In this way, thrd can be further fused with bconv or bmm to reduce the volume of data access if the residual is not saved. Finally, tanh is not required for inference as discussed. Consequently, the ultimate function order becomes $thrd \rightarrow bconv \rightarrow thrd \rightarrow pool \rightarrow bconv$ for inference. Similar condition is also applied for the FC layers.

Traditionally, BNN's last layer is also in full-precision [1], [3]. However, Tang et al. [7] showed that binarizing the final layer with a learned scaling layer could significantly compact the model as FC layers comprises the most parameters. Our observation here is that such a scaling layer can be absorbed by adding a bn function for the last layer, which may provide even better performance due to more constraint output range for the following softmax function. Note, for the last layer, since the output is real-valued and

there is no future binarization, *bn* cannot be converted into a *thrd* function.

In terms of more advanced models such as ResNet, to avoid gradient diminishing or explosion, the cross-layer shortcut connections become vital. Here, the main performance concern is that these residuals are real-valued (bit-residual cannot convey gradient), which may incur substantial extra memory load & store compared with directly saving the bits after *thrd*. In addition, the residual may need a pooling layer before the injection. Furthermore, it is also possible that the number of channels needs to adjust. In those scenarios, we use the type-A shortcut of ResNet [61].

6.2 BTC based Implementation

Similar to [26], we have also fused all the layer functions into a single GPU kernel so the repeated kernel invocation & release overhead (as long as 20 μs per invocation [62]) can be eliminated. We implement each layer function as a GPU device function. These device functions are called from a global function where the BNN network model is defined. Due to data dependency across the layers, to ensure consistency, we rely on CUDA’s cooperative-groups for global synchronization among all SMs. There are two major challenges for the overall design here: (i) *Achieving high SM utilization*. Since *WMMA* is executed at the warp level, with 32 warps per SM for Turing GPUs and 68 SMs in RTX2080Ti for instance, the overall parallelism offered by the hardware is 2176 warps, implying 2176 BMMs sized $(8,128) \times (128,8)$ per round. Consequently, the task granularity per warp should be as small as possible [59] in order to use all the SM warp slots and achieve workload balance; (ii) *Adapting to WMMA format*. As BTC can only process BMM sized $(8,128) \times (128,8) = (8,8)$, we need to ensure the row of the FC input matrix, the column of the weight, the batch of the BConv image, and the output channel can all divide 8, while the column of the FC input matrix, the row of the weight, the input channel of BConv can all divide 128. Both requirements need to be consistent across all layers. Given the BNN model can be in arbitrary configuration and we internally use our own FSB format, the address translation and calculation become more complicated. There is another format change after the final Conv layer and ahead of the first FC layer to ensure correct format transition.

7 EVALUATION

7.1 Experiment Configuration

We use two NVIDIA Turing GPUs with CC-7.5 for evaluation. Their information is listed in Table 2. The RTX2080 GPU is in a Linux 3.10.0 system with Intel Xeon E5-2680 CPU @ 2.80 GHz, 128 GB DDR3 DRAM and gcc-4.8.5. The RTX2080Ti GPU is in a Linux 2.6.32 system with Intel Xeon E5-6230 CPU @ 2.10 GHz, 384 GB DDR4 and gcc-4.8.5. All the results reported are the average of 10 times’ execution.

7.2 BMM Evaluation

For BMM evaluation, we randomly generate square matrices with increased sizes from 128 until 16K. We use the well-optimized 16-bit HGEMM (accelerated by TCUs)

from *cuBLAS* as the baseline. We compare our three BTC-based BMM designs with the BMM approach from [3], the four BSTC BMM designs from [26], and the BTC uint-4 and BMM designs from *Cutlass* [31]. Note that both the *Cutlass* BMM and uint-4 designs are accelerated by TCUs. They are the only available reference designs on BMM and uint-4 MM upon TCUs when performing the evaluation. We conduct two types of testing: (1) **General BMM** where both the input matrices and the output matrix are floating-points. It includes binarization for A and B, but excludes the binarization for C. The tested schemes are listed in Table 3. (2) **BNN-specific BMM** where both the input and the output matrices are binarized. It thus includes binarization for C but excludes A and B. This test reflects how BMM behaves in a BNN FC layer. The schemes are listed in Table 4.

Figure 16, 17, 18 and 19 show the results of the two BMM tests on TU104 RTX2080 GPU and TU102 RTX2080Ti GPU, respectively. For general BMM in Figure 16 and 18, we have three major observations: (I) No single approach dominates the entire matrix range — For small matrices ($n \leq 1K$), the fine-grained 64bit BSTC is relatively better although the advantage is marginal. This might be due to more fine-grained thread-block tasks to leverage all SMs; For medium matrices ($1K < n \leq 4K$), Design-3 based on the proposed FSB-format obtains the best performance, particularly at 4K. For large matrices ($n > 4K$), the performance of all BTC based designs drop. This is due to the fierce competition in BTC and reduced data reuse in the L0/L1 cache [63]. Nevertheless, the size of FC layers of most BMMs fall in the medium range. (II) Comparing among Design-1, 2, and 3, while Design-2 is always better than Design-1 due to improved load efficiency and shared memory reuse, the new-format based Design-3 significantly outperforms Design-1/2 except on very large matrices. Overall, without this new FSB format, BTC may not deliver any performance advantage over existing BSTC software solutions. For BNN-specific BMM in Figure 17 and 19, the avoidance of binarizing A & B, and reduced memory store after binarizing C, dramatically amplify the supremacy of Design-3. The speedup is more than $12\times$ over the FP-16 *cuBLAS* at 4K on RTX2080. (III) Comparing between BMMs and uint-4 based GEMM over the same TCUs, we can observe that BMMs demonstrate obvious advantage. This is largely because (a) the smaller memory footprint (1-bit vs 4-bits) reduces the bandwidth and storage pressure over the data-path [64], [65] and registers [66]; (b) with the same bit-width for the ALUs in the TCUs, using 1-bit can compact $4\times$ more data elements than using int-4 or uint-4. Similar conditions apply to other types such as int-8 and FP16.

7.3 BConv Evaluation

For BConv, there are much more parameters than BMM: *input_height*, *input_width*, *weight_height*, *weight_width*, *batch*, *input_channels*, *output_channels*, *stride*, *pooling*, etc. We compare our two BTC-based designs (Note that we use *bmma* to denote Design-1 and *bmmafmt* to denote Design-2) with TCU-accelerated half-precision *cuDNN-base* (no workspace), *cuDNN-fast* (plenty workspace), and two BSTC (*bconv32* and *bconv64*) designs [26]. We use *cuDNN-base* as the baseline and perform the two types of test: (1) **General BConv** where the input, filter and output tensors are all floating-points; (2) **BNN-specific BConv** where all of them are binarized.

TABLE 2: Evaluation Platforms. "Reg" refers to the number of 4-byte registers. "Thds" refer to threads. "Dri/Rtm" refer to CUDA driver and runtime versions.

GPU	Arch/CC	Code	SMs	CTAs/SM	Warps/SM	Thds/CTA	Regs/SM	Shared/SM	TCUs/SM	Memory	Mem Bandwidth	Dri/Rtm
RTX-2080Ti	Turing-7.5	TU102	68	16	32	1024	64K	64K	8	11GB GDDR6	616 GB/s	10.1/10.0
RTX-2080	Turing-7.5	TU104	46	16	32	1024	64K	64K	8	8GB GDDR6	448 GB/s	10.0/10.0

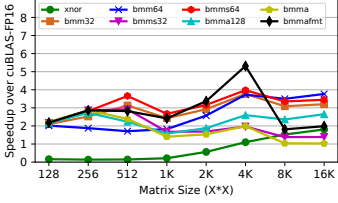


Fig. 16: General BMM on RTX2080

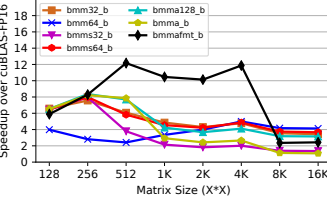


Fig. 17: Specific BMM on RTX2080

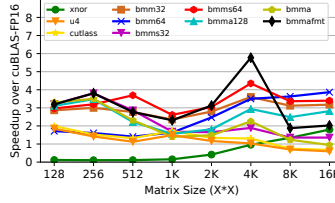


Fig. 18: General BMM on RTX2080Ti

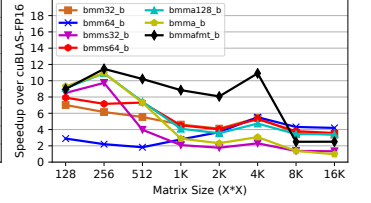


Fig. 19: Specific BMM on RTX2080Ti

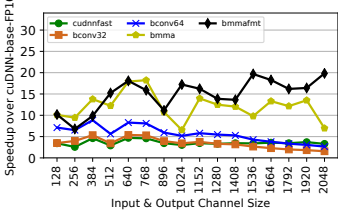


Fig. 20: General BConv on RTX2080

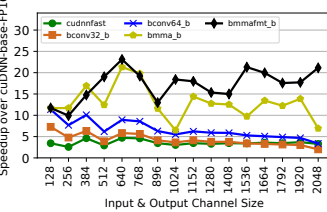


Fig. 21: Specific BConv on RTX2080

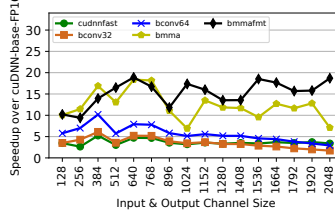


Fig. 22: General BConv on RTX2080Ti

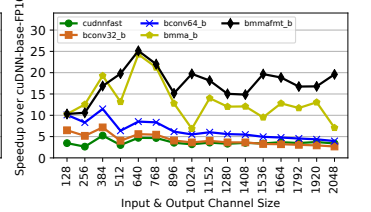


Fig. 23: Specific BConv on RTX2080Ti

TABLE 3: BMM full-precision output schemes.

Schemes	Description	Algorithm	Input	Output
cuBLAS	Simulating BMM via FP16 HGEMM	HGEMM	16bit	32bit
xnor	BMM design in [1]	BMM	32bit	32bit
bmm32	32bit BSTC BMM in [26]	BMM	32bit	32bit
bmm64	64bit BSTC BMM in [26]	BMM	32bit	32bit
bmm32	Fine-grained 32bit BSTC BMM in [26]	BMM	32bit	32bit
bmm64	Fine-grained 64bit BSTC BMM in [26]	BMM	32bit	32bit
cutlass	BMM on TCUs in Cutlass library [31]	BMM	1bit	32bit
u4	BMM via uint-4 MM on TCUs in Cutlass [31]	4bit-MM	4bit	32bit
bmma	Design-1: basic BTC implementation	BMM	32bit	32bit
bmma128	Design-2: 128bit load and shared memory	BMM	32bit	32bit
bmmafnt	Design-3: new format	BMM	32bit	32bit

TABLE 4: BMM bit output schemes.

Schemes	Description	Input	Output
bmm32_b	32bit BSTC BMM in [26] with bin output	1bit	1bit
bmm64_b	32bit BSTC BMM in [26] with bin output	1bit	1bit
bmm32_b	Fine-grained 32bit BSTC BMM in [26] with bin output	1bit	1bit
bmm64_b	Fine-grained 64bit BSTC BMM in [26] with bin output	1bit	1bit
bmma_b	Design-1: basic BTC implementation with bin output	1bit	1bit
bmma128_b	Design-2: 128bit load with bin output	1bit	1bit
bmmafnt_b	Design-3: new format with bin output	1bit	1bit

Figure 20, 21, 22 and 23 show the results of the two types of tests with $batch=16$, $input_size=64$, $weight_height=3$ and $stride=1$ on the two Turing GPUs. We increase both $input_channels$ (C) and $output_channels$ (O) from 128 to 2048. As is shown, our two BTC-based approaches exhibit considerable speedups over existing methods. Particularly, the FSB new format design achieves up to $25\times$ over the FP-16 cuDNN with $C=O=640$ on RTX2080Ti. Comparing between the two BTC designs, we can see that (i) when $C=O=128$, the two designs are just equivalent, so they show similar performance; (ii) When $C=O=384$, Design-1 is better possibly because $ldm=384$ is also a good choice for memory load (see Section 4). (iii) For the other points, Design-2 shows obvious advantages.

7.4 BNN Evaluation

Finally, we evaluate the overall BNN implementation. Table 5 lists the 6 models we used for evaluation. Table 6 and 7 list the latency and throughput we obtained for the six models on the two NVIDIA Turing GPUs, respectively. The latency is measured under a batch size of 8 since 8 is the smallest value to leverage the bit-tensorcores so essentially the latency is for the inference of 8 images. The throughput is measured under a batch of 1024 images for *MNIST* and

Cifar10, and 512 for *ImageNet*. We compare our performance with the four approaches from the latest SBNN work (from <http://github.com/uwdown/SBNN>.) [26]. Overall, compared with the best approach *SBNN-64-Fine* from SBNN, our BTC using the default format design achieves on average $2.10\times$ in latency and $1.65\times$ in throughput on RTX2080Ti, and $2.08\times$ in latency and $1.62\times$ in throughput on RTX2080 across the six models. Our proposed BTC new format achieves $2.33\times$ in latency and $1.81\times$ in throughput on RTX2080Ti, and $2.25\times$ in latency and $1.77\times$ in throughput on RTX2080. The best speedup has been achieved by the FSB-format based design on RTX2080Ti GPU for ResNet-14 on *Cifar10* — $3.79\times$ in latency and $2.84\times$ in throughput.

Regarding this result, we have three observations: (I) Our BTC design generally achieves more than $2\times$ over existing work except for *MNIST-MLP* and *ImageNet-Alexnet* where the throughput is actually a little bit worse. The reason is that for *MLP*, a batch of 1024 is still insufficient for fully leveraging the bit-tensorcores, as will be discussed later. For *Alexnet*, the delay of the first layer remains too large (77.4%) while the other convolution layers are relatively smaller than alternative networks, which cannot fully utilize the BTCs. (II) Although showing better performance, the speedup led by the new FSB format is not as good as in BMM and BConv, the major reason is that both the batch size and the channels are relatively small ($batch \leq 1K$, $channels \leq 512$) which is not the region that the FSB format can demonstrate its best speedups (Section 7.2 and 7.3).

Table 8 and 9 compare the single image raw latency and throughput of our BTC-based new format design with other existing BNN approaches for CPU, GPU, Xeon-Phi and FPGA using Alexnet and VGG-16 on ImageNet. As can be seen, our design achieves the best single-image raw latency and throughput on Alexnet, and more than $5\times$ throughput enhancement on VGG-16 over the existing works as listed.

7.5 Sensitivity Study

We perform several sensitivity studies in this subsection.

Latency Breakdown: Figure 24 illustrates the percentage breakdown of the latency (measured by the *clock()* instruc-

TABLE 5: BTC Evaluation. “1024FC” refers to a fully-connected layer with 1024 neurons. “2x128C3” refers to 2 convolution layer with 128 output channels and 3x3 filter. “P2” refers to a 2x2 pooling layer. “128C11/4” refers to a convolution layer with 128 output channels, 11x11 filter size and stride=4. “Input size” is of $input_height \times input_width \times input_channels$ format. “Ref” is short for references. “BNN” refers to state-of-the-art BNN training accuracy from existing work. “Our BNN” is the BNN training accuracy we obtained from our own BNN implementation. “Full-Precision” is the 32 bits full-precision training accuracy from existing works.

Dataset	Ref	Network	Ref	Network Structure	Input Size	Out	BNN	Our BNN	Full-Precision
MNIST	[67]	MLP	[1]	1024FC-1024FC-1024FC	28x28x1	10	98.6% [1]	97.6%	99.1% [1]
Cifar-10	[68]	VGG	[4]	(2x128C3)-MP2-(2x256C3)-MP2-(2x512C3)-MP2-(3x1024FC)	32x32x3	10	89.9% [1]	88.7%	90.9% [8]
Cifar-10	[68]	ResNet-14	[3]	128C3/2-4x128C3-4x256C3-4x512C3-(2x512FC)	32x32x3	10	N/A	91.6%	N/A
ImageNet	[69]	AlexNet	[70]	(128C11/4)-P2-(256C5)-P2-(3x256C3)-P2-(3x4096FC)	224x224x3	1000	75.7/46.1% [8]	74.2/44.7%	80.2/56.6% [8]
ImageNet	[69]	VGG-16	[71]	(2x64C3)-P2-(2x128C3)-P2-(3x256C3)-P2-2x(3x512C3)-P2-(3x4096FC)	224x224x3	1000	76.8%/NA [40]	77.7/53.4%	88.4%/NA [40]
ImageNet	[69]	ResNet-18	[3]	64C7/4-4x64C3-4x128C3-4x256C3-4x512C3-(2x512FC)	224x224x3	1000	73.2/51.2% [3]	72.7/48.6%	89.2/69.3% [3]

TABLE 6: BTC Inference Performance on NVIDIA Turing RTX2080 GPU.

	MNIST-MLP		Cifar10-VGG		Cifar10-ResNet14		ImageNet-AlexNet		ImageNet-VGG		ImageNet-ResNet18	
Schemes	8 Latency	Throughput	8 Latency	Throughput	8 Latency	Throughput	8 Latency	Throughput	8 Latency	Throughput	8 Latency	Throughput
SBNN-32	0.227ms	2.88×10^6 fps	1.891ms	1.06×10^4 fps	5.138ms	4.17×10^3 fps	4.494ms	3.18×10^3 fps	27.638ms	4.26×10^2 fps	6.550ms	2.60×10^3 fps
SBNN-32-Fine	0.082ms	1.97×10^6 fps	1.536ms	1.05×10^4 fps	4.382ms	3.97×10^3 fps	3.928ms	3.05×10^3 fps	27.009ms	4.25×10^2 fps	5.944ms	2.37×10^3 fps
SBNN-64	0.908ms	8.44×10^5 fps	2.816ms	1.06×10^4 fps	8.132ms	4.59×10^3 fps	17.258ms	1.95×10^3 fps	40.247ms	5.23×10^2 fps	8.108ms	3.01×10^3 fps
SBNN-64-Fine	0.074ms	5.51×10^6 fps	0.999ms	1.63×10^4 fps	2.550ms	6.52×10^3 fps	2.871ms	3.79×10^3 fps	16.68ms	6.65×10^2 fps	3.736ms	3.42×10^3 fps
BTC	0.061ms	3.37×10^6 fps	0.364ms	3.62×10^4 fps	0.827ms	1.58×10^4 fps	2.367ms	3.85×10^3 fps	7.449ms	1.24×10^3 fps	1.869ms	5.48×10^3 fps
BTC-FMT	0.055ms	5.48×10^6 fps	0.338ms	3.85×10^4 fps	0.724ms	1.71×10^4 fps	2.326ms	3.77×10^3 fps	7.021ms	1.34×10^3 fps	1.833ms	5.55×10^3 fps

TABLE 7: BTC Inference Performance on NVIDIA Turing RTX2080Ti GPU.

	MNIST-MLP		Cifar10-VGG		Cifar10-ResNet14		ImageNet-AlexNet		ImageNet-VGG		ImageNet-ResNet18	
Schemes	8 Latency	Throughput	8 Latency	Throughput	8 Latency	Throughput	8 Latency	Throughput	8 Latency	Throughput	8 Latency	Throughput
SBNN-32	0.252ms	2.99×10^6 fps	1.596ms	1.19×10^4 fps	4.909ms	4.68×10^3 fps	1.937ms	7.62×10^3 fps	23.788ms	5.13×10^2 fps	5.863ms	3.08×10^3 fps
SBNN-32-Fine	0.082ms	2.43×10^6 fps	1.548ms	1.19×10^4 fps	4.061ms	4.65×10^3 fps	1.733ms	7.16×10^3 fps	22.722ms	5.06×10^2 fps	5.145ms	3.10×10^3 fps
SBNN-64	0.952ms	1.03×10^6 fps	2.921ms	1.37×10^4 fps	8.633ms	5.95×10^3 fps	14.214ms	2.59×10^3 fps	31.561ms	7.08×10^2 fps	8.092ms	3.91×10^3 fps
SBNN-64-Fine	0.070ms	6.87×10^6 fps	0.926ms	2.09×10^4 fps	2.341ms	7.86×10^3 fps	2.017ms	4.99×10^3 fps	12.057ms	8.83×10^2 fps	3.233ms	4.52×10^3 fps
BTC	0.057ms	4.38×10^6 fps	0.317ms	4.69×10^4 fps	0.728ms	2.06×10^4 fps	1.878ms	4.87×10^3 fps	5.840ms	1.62×10^3 fps	1.538ms	7.23×10^3 fps
BTC-FMT	0.053ms	6.78×10^6 fps	0.276ms	5.06×10^4 fps	0.618ms	2.24×10^4 fps	1.862ms	4.87×10^3 fps	5.466ms	1.76×10^3 fps	1.438ms	7.34×10^3 fps

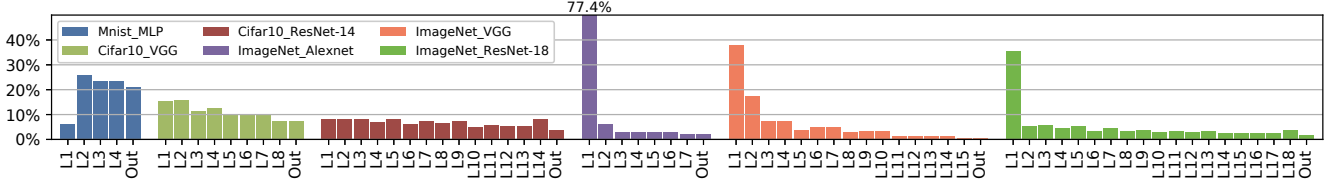


Fig. 24: Per-layer latency breakdown of our BTC new-format based BNN design on the 6 models.



Fig. 25: Normalized throughput with respect to increased batch size for the BTC new-format BNN design on the 6 models.

TABLE 8: Comparing with FPGA works using AlexNet on ImageNet.

AlexNet/ImageNet	Platform	Raw Latency	Throughput
RebNet [72]	Xilinx Virtex VCU108 FPGA	1902 μ s	521 img/s
FP-BNN [23]	Intel Stratix-V FPGA	1160 μ s	862 img/s
O3BNN [25]	Xilinx Zynq ZC706 FPGA	774 μ s	1292 img/s
SBNN [26]	NVIDIA Tesla V100 GPU	979 μ s	4400 img/s
BTC	NVIDIA RTX2080Ti GPU	559 μ s	4869 img/s

TABLE 9: Comparing with CPU, GPU and FPGA using VGG-16 on ImageNet.

Vgg-16/ImageNet	Platform	Raw Latency	Throughput
BitFlow [40]	NVIDIA GTX1080	12.87 ms	78 img/s
BitFlow [40]	Intel i7-7700 HQ	16.10 ms	62 img/s
BitFlow [40]	Intel Xeon-Phi 7210	11.82 ms	85 img/s
O3BNN [25]	Xilinx Zynq ZC706 FPGA	5.626 ms	178 img/s
SBNN [26]	NVIDIA Tesla V100 GPU	3.208 ms	312 img/s
BTC	NVIDIA RTX2080Ti GPU	3.570 ms	1760 img/s

TABLE 10: Layer-wise Synchronization Overhead.

Sync %	Mnist-MLP	Cifar10-vgg	Cifar10-ResNet14	Alexnet	VGG	ResNet18
	8.26%	14.10%	13.20%	1.36%	1.72%	5.67%

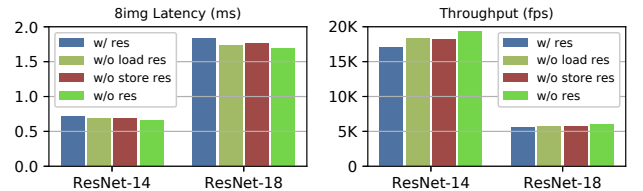


Fig. 26: Cifar-ResNet14 Latency: 9.7% speedup, Throughput: 14%, ImageNet-ResNet18 Latency: 9.0% speedup, Throughput: 8.3%

tion on GPU) for the inference of 8 images over the six models on the RTX-2080 GPU. Clearly, the first layer contributes the most delay for the three ImageNet models due significantly larger image size than the other two datasets. For AlexNet, the percentage can be as high as 77.4%. It is also over 35% for VGG-16 and ResNet-18. This is different from existing belief that the first layer is often not a big issue due to the least parameters and computation [2], [26]. The latency for other layers are roughly balanced.

Synchronization Overhead: As we enforce global synchronization through cooperative-groups per layer to ensure

data consistency, such global synchronizations can introduce extra overhead and idle waiting of SMs. Table 10 shows the percentage of this synchronization overhead, which is measured by removing all the synchronization primitives. As can be seen, this overhead is the most for the medium network models, e.g., the two on Cifar10 (14.1% and 13.2%).

Shortcut Overhead: We then focus on the two ResNet models and measure the overhead incurred by handling the cross-layer residual. Figure 26 show the latency and throughput of the two ResNet models on RTX-2080 regarding four scenarios: (a) with residual; (b) save the residual

TABLE 11: 8img Latency for ResNet with increased depth on RTX2080.

ResNet/ImageNet	ResNet-18	ResNet-50	ResNet-101	ResNet-152
BTC	1.538 ms	4.668 ms	8.873 ms	13.393 ms
BTC-FMT	1.438 ms	4.169 ms	8.521 ms	13.316 ms

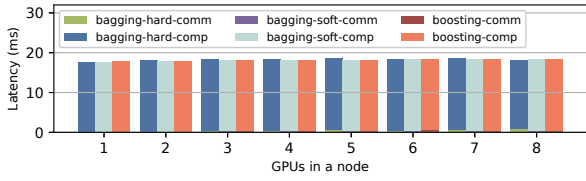


Fig. 27: Latency breakdown for BENN scaling-up with more GPUs in a node.

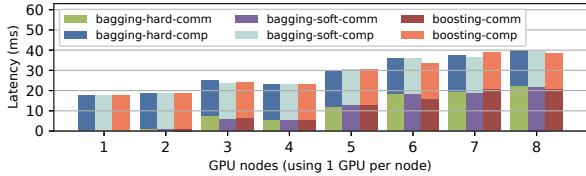


Fig. 28: Latency breakdown for BENN scaling-out with more GPU nodes.

without fetching them; (c) fetch the residual without saving them; and (d) without the residual at all. For ResNet-14 on Cifar10, if eliminating the residual-related operations, we can gain 9.7% speedup in latency and 14% in throughput. For ResNet-18 on ImageNet, we gain 9.0% and 8.3%.

Utilization: We investigate the impact of batch size over the throughput. If the batch size is too small, the hardware such as the bit-tensorcores might be under-utilized. Figure 25 shows the inference throughput of the six models with different batch sizes (normalized to the throughput with a batch of 1024 for MNIST and Cifar10, and 512 for ImageNet) on RTX2080. As can be seen, for ImageNet, a batch of 128 is sufficient to achieve the best throughput while for Cifar10, a batch of 512 is necessary. For MNIST, even with batch size arising from 16K to 32K, the throughput is still increasing. The best throughput is obtained at 32K with 7.62×10^6 fps.

Network Depth: Finally we look at the performance impact from increased network depth. Table 11 lists the raw latency for 8 image inference with ResNet-18, 50, 101 and 152 [61] on RTX2080. As can be seen, the latency increases almost in linear with more layers in the network. Even with very deep models, our BNN framework can still work well.

7.6 BTC-based BENN Scaling

To compensate potential accuracy loss of BNNs, Zhu et al. recently proposed BENNs [11], which assembled multiple BNNs through bagging and boosting to tackle the intrinsic instability of BNN training, thus achieving superior accuracy, e.g., top-1 54.3% for AlexNet and 61% for ResNet-18 on ImageNet). We implement the BTC-based BENN which executes each BENN’s BNN component on a single GPU concurrently and merges their output through collective communication over the inter-node network or intra-node GPU interconnects [73]. We evaluate our design on an HPC cluster with 8 nodes connected by InfiniBand (IB), and each node incorporates 8 NVIDIA RTX-2080Ti GPUs (see Table 2) connected by PCI-e [74].

We perform two types of evaluations: (i) *Scaling-up*: we use a single node, and increase the number of BNN components inside BENN, corresponding to adopting more GPUs in the execution. We use the *reduction* collective communication primitive from the NCCL library [75] for the bagging

and boosting operations of BENN. Figure 27 illustrates the latency breakdown of BENN inference using the *hard-bagging*, *soft-bagging* and *boosting* ensemble methodologies [11]. Each BENN component is a BTC-based ResNet-18 BNN using the new FSB format. The batch size is 128. As can be seen, due to the small amount of data transfer and the high efficiency of NCCL, the communication overhead is tiny for all the three ensemble techniques, which implies that by adopting BENN, we can greatly improve BNN accuracy but still gain the great performance advantage of BNN. (ii) *Scale-out*: in this test, we adopt all the 8 nodes, but use only a single GPU per node for the BENN inference. We use *MPI_reduce* primitive from *Intel-MPI-2019u4* for the bagging and boosting operations. As shown in Figure 27, different from the scaling-up, with increased BENN components, the latency surges when scaling-out. With 8 GPUs, the communication latency is even higher than the BNN inference itself. This suggests that communication is key to BENN design.

7.7 Discussion on BNN Accuracy and Usage

We further discuss the accuracy of BNN compared to DNN. So far, all the concerns regarding the accuracy loss of BNNs are based on two implicit assumptions: (a) BNN and DNN are using the same number of neurons and channels; (b) BNN and DNN are using the same models that were originally designed for full-precision DNN. For (a), if the number of neurons or channels for BNN can be expanded, e.g., through boosting, we can gain compatible or even better accuracy than DNN [11] with little overhead, as already shown. For (b), the network structure designed for DNN (e.g., VGG block) might not be the most suitable for BNNs. Recently, people started to look at BNN-oriented network structure, such as the *dense block + improvement block* structure in MeliusNet [13]. With such novel structures, BNN’s accuracy can be greatly improved. We anticipate BNN to be quite useful for (i) (Embedded) real-time system (e.g., [19]); (ii) Large-scale data preprocessing and vision (e.g., [14], [15], [16]). Finally, BNN is continuously a focused area in the ML community. More advanced BNN-specific models and training methods are under active development.

8 CONCLUSION

In this paper we investigate the new bit computation capability of the tensorcores in Turing GPUs. We found that the stride of memory access can significantly impact the performance of memory access. Based on this observation, we propose a new bit data format for efficient design of Bit-Matrix-Multiplication and Bit-Convolution. We built the full implementation for BNN inference. Evaluations using six network models (MLP, VGG-like, AlexNet, VGG-16, ResNet-14/18) on three datasets (MNIST, Cifar10 and ImageNet) over two latest Turing GPUs (RTX2080 and RTX2080Ti) show that our design can bring on average $2.33 \times$ (up to $3.79 \times$) in latency and $1.81 \times$ (up to $2.84 \times$) in throughput compared with state-of-the-art BNN design for GPUs, leading to super realtime performance. Future work include: (a) Exploiting BTC for alternative utilization such as Graph-BLAS computation; (b) Investigating a combination of FPGAs/ASICs and GPUs for BNN online training tasks; (c) Testing in Ampere GPUs.

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