Transactions Briefs

Design and Analysis of Isolated Noise-Tolerant (INT) Technique in Dynamic CMOS Circuits

I-Chyn Wey, You-Gang Chen, and An-Yeu Wu

***Abstract*—Along with the progress of advanced VLSI technology, noise issues in dynamic circuits have become an imperative design challenge. The *twin-transistor design* is the current state-of-the-art design to enhance the noise immunity in dynamic CMOS circuits. To achieve the high noise-tolerant capability, in this paper, we propose a new *isolated noise-tolerant (INT) technique* which is a mechanism to isolate noise tolerant circuits from noise interference. Simulation results show that the proposed 8-bit *INT* Manchester adder can achieve 1.66× *average noise threshold energy (ANTE)* improvement. In addition, it can save 34% *power delay product (PDP)* in low *signal-to-noise ratio (SNR)* environments as compared with the 8-bit *twin-transistor* Manchester adder under TSMC 0.18-μm process.**

***Index Terms*—Dynamic CMOS circuit, isolated noise-tolerant (INT) technique, noise-tolerant design.**

I. Introduction

With the progress of advanced VLSI technology, the scaling down of supply and threshold voltage reduces the noise margin. Moreover, under low signal-to-noise ratio (SNR) noisy environment, the power spent on solving noise issues dominates the overall power consumption in computing systems [1]–[3]. Therefore, the efficient noise-tolerant circuit design becomes an urgent challenge in the advanced VLSI design. Dynamic CMOS circuit is one of most popular logic families adopted in the high-performance applications due to its high-speed characteristics. However, a dynamic circuit is inherently susceptible to noise due to floating nodes that may occur in the evaluation phase. Noise interference in static circuits only leads to glitch while the circuits are still functional. Once the noise interference occurs in dynamic circuits, the leakage charge cannot be recovered and leads to malfunction. Hence, we will focus on the design of noise-tolerant dynamic circuits in this paper.

Several techniques have been proposed to increase the noise immunity of dynamic circuits in [3]–[8]. The existing noise tolerant design techniques can be divided into two main categories: One is to prevent the dynamic node from floating [4], [6]. The other is to raise the source voltage of transistor to prevent the input gate from noise injection [3], [7], [8]. The latter techniques can more effectively improve the noise tolerance and have become a popular solution to enhance noise immunity in dynamic circuits. However, all existing techniques must still suffer from expensive design penalty in terms of speed, power, and area to achieve the goal of noise tolerance. Especially, while the requirement of noise tolerance is increased along with the progress of VLSI technology, the design overhead is further increased dramatically.

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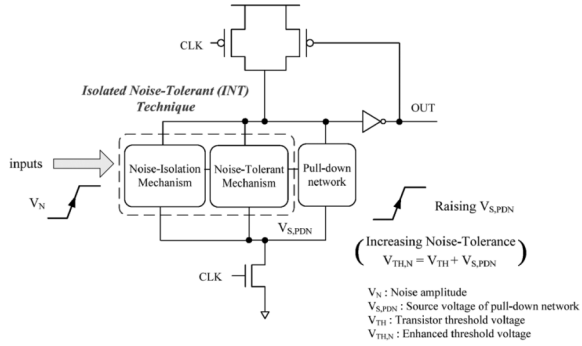

Fig. 1. Proposed INT technique in dynamic CMOS circuits.

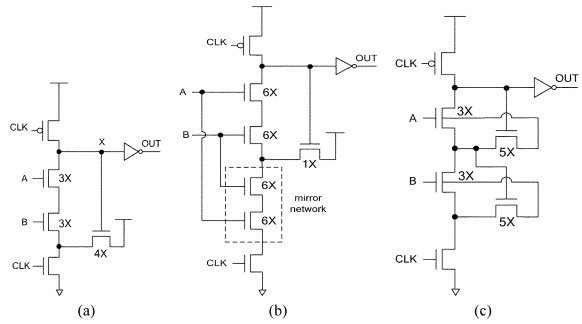

Fig. 2. Raise source voltage by using: (a) nMOS pull-up transistor with feedback control [7]; (b) mirror technique [8]; (c) twin-transistor technique [3].

In this paper, we develop a new noise-tolerant technique, called isolated noise-tolerant (INT) technique, to enhance the noise tolerance of dynamic circuits. As shown in Fig. 1, the *noise-tolerant mechanism* can raise the source voltage of pull-down network, $V_{S,\mathrm{PDN}}$, to enhance the noise immunity of dynamic circuits from V_{TH} to $V_{\mathrm{TH},N}$ ($V_{\mathrm{TH},N} = V_{\mathrm{TH}} + V_{S,\mathrm{PDN}}$). Besides, the INT technique adds the *noise-isolation mechanism* to protect noise-tolerant mechanism from noise interference. This *noise-isolation mechanism* is the major difference between the proposed INT technique and conventional noise-tolerant techniques. By this way, we can further improve the noise-tolerance of dynamic circuits and bring dynamic circuits to operate under low SNR environments. Moreover, in the proposed INT design, the performance overhead for enhancing the noise-tolerance can be greatly reduced.

II. Review of Existing Noise Tolerant Dynamic Circuit Designs

While the noise voltage in the transistor gate is greater than the sum of source voltage and transistor threshold voltage, it will cause malfunction in the dynamic CMOS circuits. Raising the source voltage of pull-down network is the most popular way to improve the noise-tolerance in dynamic circuits. In Fig. 2(a) [7], an nMOS pull-up transistor with feedback control is employed to pull-up the source voltage, and this nMOS is turned off as the dynamic output X goes low. However, the response speed in node X is slower than the noise injection speed. Consequently, the noise-tolerant mechanism is easily destroyed by the

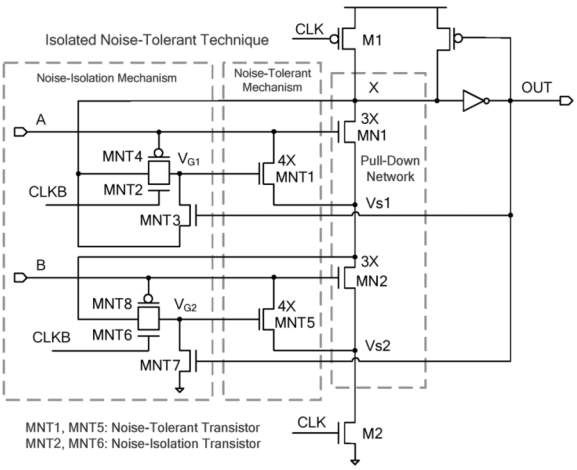

Fig. 3. Proposed INT AND gate circuit.

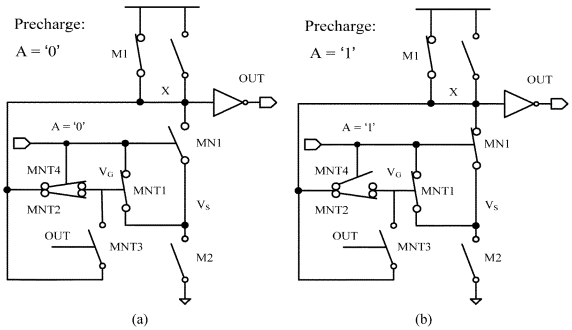

Fig. 4. Operation of the proposed INT circuit in precharge phase: (a) as input signal is "0". (b) as input signal is "1".

input noise. Moreover, dc power consumption and non-full-swing of output signal are serious problems in the nMOS pull-up technique.

Fig. 2(b) [8] illustrates the *mirror* technique, which can solve both dc power consumption and non-full-swing of output signal problems while raising the source voltage. The mirror technique uses the principle of Schmitt trigger to increase the dynamic switching threshold by using a mirror nMOS pull-down network. However, the stacked nMOS transistor will seriously increase the propagation delay.

Recently, the *twin-transistor* technique was proposed to pull up the source voltage in a noise-dependent manner [3]. As illustrated in Fig. 2(c) [3], the twin-transistor technique employs an extra transistor for every pull-down transistor. The drain nodes of the additional nMOS transistors are connected to the inputs. The charge injected by noise can be drained away through the additional nMOS transistors. Then the source voltage of pull-down network is raised to enhance the noise tolerant capability of dynamic circuits. Nevertheless, the noise-tolerant mechanism may still possibly be destroyed by the input noise.

All these existing techniques can enhance the noise tolerance of dynamic CMOS circuits. However, none of these noise-tolerant mechanisms are under protection, and they may possibly be destroyed by serious noise interference. *Therefore, all these existing techniques need to pay expensive design penalty in terms of speed, power, and area to achieve the noise tolerance goal. Especially, as the requirement of noise tolerance is increased along with the progress of process technology, the design overhead will further increase dramatically*.

III. Proposed INT Technique

A. Proposed INT Circuits

The proposed INT circuit is illustrated in Fig. 3. We take an INT AND gate as an example circuit. The INT technique *consists of noise-tolerant mechanism* and *noise-isolation mechanism*. The *noise-tolerant mechanism* can raise the source voltage of pull-down network to enhance the noise immunity of dynamic circuits. The *noise-isolation mechanism* can isolate the noise-tolerant mechanism from noise interference and essentially maintain the noise-tolerant capability. As illustrated in Fig. 3, the added $MNT1$ transistor provides a path to transmit noise from A to $Vs1$. By this way, the noise charge can be transmitted away and the source voltage $Vs1$ can be raised to enhance the noise immunity of dynamic circuits. Therefore, we call the transistor $MNT1$ as *noise-tolerant transistor* (*NT-transistor*). The $MNT2$ transistor is turned off in the evaluation phase to isolate the gate of $MNT1$ from noise interference. Therefore, we call $MNT2$ as *noise-isolation transistor*. The $MNT3$ transistor provides a discharge path for maintaining function correctness and the $MNT4$ transistor is utilized to prevent the occurrence of clock feed through. The weak feedback keeper prevents the dynamic node from floating. Transistors $MNT5 \sim MNT8$ perform the similar function as $MNT1 \sim MNT4$ in the INT AND circuit.

In our INT circuit, we enhance the noise-tolerance ability by pulling up the source voltage in a noise-dependent manner, which follows the *twin-transistor* design [3]. The main difference of our proposed INT technique is that the noise-tolerant mechanism can be protected from being destroyed even if the noise input is large. Therefore, the noise-tolerant ability can be greatly improved and the performance sacrifice for enhancing the noise-tolerance can be greatly reduced.

B. Operations of the INT Technique

The operations of the INT technique can be divided into three cases: *operation in precharge phase, normal operation in evaluation phase, and operation in evaluation phase with noise interference*. To simplify the explanation of INT operation, we take the INT buffer as example. The same operation principle can be extended to all other INT dynamic circuits.

1) ***Precharge Phase***: In the precharge phase, the clock signal CLK is low and the inverse clock signal $CLKB$ is high. The dynamic node X is charged to logic high and the node OUT to logic low. In this phase, $MNT2$ is turn-on by $CLKB$ and $MNT3$ is turn-off by OUT, as illustrated in Fig. 4. Then node V_G is precharged to high to turn on $MNT1$. To enhance the noise-tolerance, the conduction of $MNT1$ is essential for raising the source voltage of $MN1$.
2) ***Evaluation Phase (Normal Operation)***: In the evaluation phase, CLK and $CLKB$ are switched to high and low, respectively. The dynamic node X is floating because $M1$ is turn-off by CLK. As the input A is at logic "0", the isolated noise-tolerant mechanism is activated. As illustrated in Fig. 5(a), $MNT2$ is turned off as $CLKB$ switches to low and $MNT3$ is also off since the input A is at logic "0". As a result, node V_G is isolated and latched in logic high to maintain the conduction of $MNT1$. However, the clock feed through effect caused by $CLKB$ can lower the voltage in node V_G. We use $MNT4$ to provide a conduction path to charge the node V_G to V_{DD}. By this mean, the clock feed through effect can be suppressed and the noise-tolerant ability can be enhanced. As the input A is at logic "1," the node X is pull-down to logic low and OUT is at logic high. The charge in the node V_G can be discharged through $MNT3$ to turn off $MNT1$ to ensure the correctness of function in normal mode, as illustrated in Fig. 5(b).
3) ***Evaluation Phase (Operation Under Noise Interference)***: As noise interrupts the circuit illustrated in Fig. 5(c), the noise charge

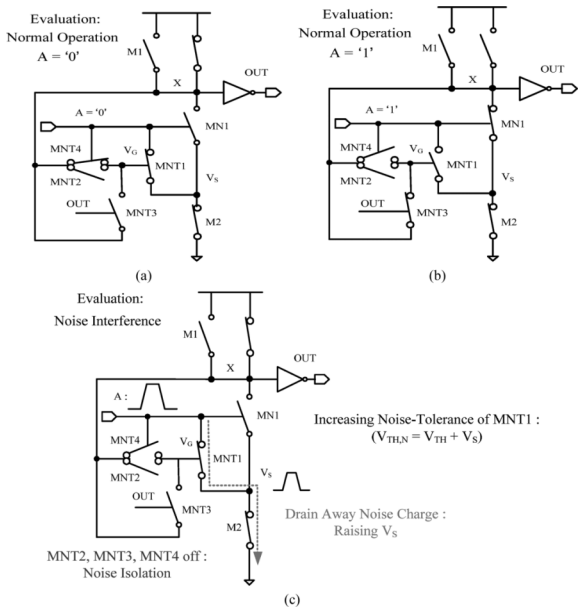

Fig. 5. Operation of the proposed INT circuit in evaluation phase: (a) operate in normal operation as input signal is "0"; (b) operate in normal operation as input signal is "1"; and (c) operate in evaluation phase with noise interference.

can be drained away immediately through $MNT1$ to the source node. As the source voltage raises, noise tolerant ability is also enhanced. Thus, it is important to maintain the conduction of $MNT1$. While input A is logic "0," $MNT2$ and $MNT3$ are off to isolate the connection of node V_G. As the noise signal raises, the $MNT4$ transistor are also be turned off to isolate the node V_G in logic high. As a result, the noise-tolerant mechanism can be protected and the noise-tolerant ability will not degrade even under the presence of high noise interference.

C. Experimental Results

To demonstrate the noise-isolation property in the proposed INT technique, we perform simulation experiments by HSPICE. We first demonstrate that the drain current in the NT-transistor is dominated by its gate voltage. Then we show that the INT technique can hold the gate voltage of NT-transistor high. Finally, we illustrate that the source voltage of NT-transistor can be hold high in the proposed INT design to achieve high noise-tolerance.

1) Noise-Tolerance Capability of the NT-Transistor: The gate voltage of *NT-transistor* dominates the capability of noise-tolerance. As illustrated in Fig. 6, the drain current in the NT-transistor, $I_{D,NT}$, is determined by its gate voltage, $V_{G,NT}$. The degradation of gate voltage results in the reduction of noise-tolerance. Preventing the degradation of gate voltage can protect the noise-tolerant mechanism not being destroyed.

We compare the gate voltage of NT-transistor associated with the injected noise in various noise-tolerant techniques in Fig. 7. The $V_G(a) \sim V_G(d)$ represents the gate voltages of NT-transistor in the nMOS pull-up design [7], the *mirror technique* [8], the *twin-transistor design* [3], and the *proposed INT design*, respectively. The gate voltage $V_G(a) \sim V_G(c)$ degrades fast as the injected noise is high enough to turn on the pull-down nMOS transistor. In the proposed INT circuits, the gate voltage of NT-transistor $MNT1$ can be isolated from noise interference. Therefore, the gate voltage $V_G(\mathrm{d})$ in the INT circuit does not degrade, even if the injected noise is large.

2) Increase of Source Voltage in Noise-Tolerant Dynamic CMOS Circuits: As illustrated in Fig. 8, we compare the enhancement of

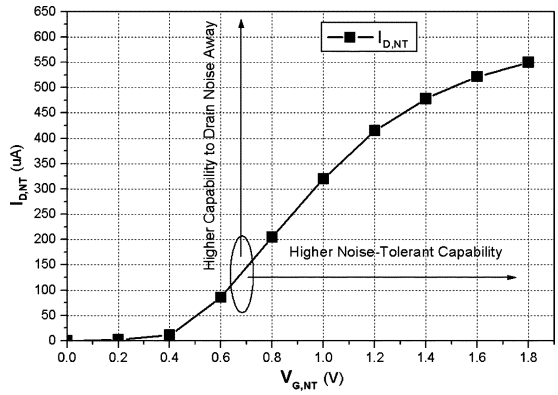

Fig. 6. Drain current in the NT-transistor as a function of its gate voltage.

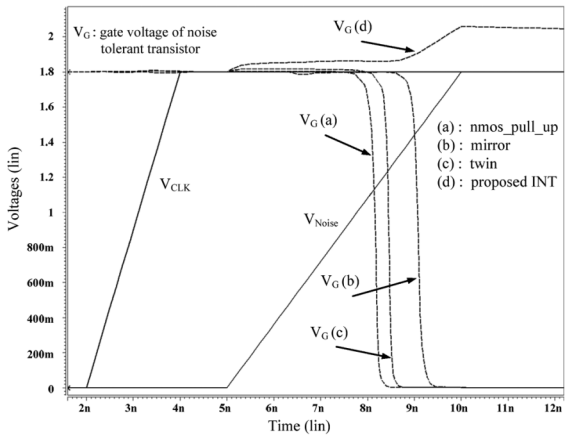

Fig. 7. Gate voltage of *NT-transistor* associated with the injected noise.

noise-tolerance by observing the source voltage in various noise tolerant techniques. In the conventional passive mode noise-tolerant techniques, as illustrated in $V_S(a)$ [7], the source voltage of the pull-down network is precharged to high. However, the source voltage will be pulled down to low as the dynamic output is hold in logic high in the evaluation phase. The dynamic output is destroyed as $V_{\mathrm{noise}} - V_S > V_{\mathrm{TH}}$. The *mirror technique* [8] is *the prior art design of the passive mode noise-tolerant techniques*. The noise-tolerant ability can be improved; however, it is still a passive mode noise-tolerant design, the source voltage $V_S(b)$ is still pulled down as V_{noise} increases. As for the *active mode* noise-tolerant techniques, the *twin-transistor* technique [3] is *the prior art design*. As illustrated in Fig. 8, it can raise the source voltage $V_S(c)$ depending on the degree of V_{noise}. Enhancing the noise-tolerance in an active manner can mitigate the performance penalty, which will be discussed later in Section IV-A. However, the noise-tolerant mechanism is destroyed as the noise signal is large and the source voltage $V_S(d)$ is pulled down.

The *proposed INT technique* is also an *active mode* noise-tolerant technique. Furthermore, the gate voltage of NT-transistor can be maintained to V_{DD} in a *noise-isolated manner*. Eventually, the source voltage $V_S(d)$ of the pull-down network can be further raised and the noise-tolerant ability can be improved. The performance comparison results will be illustrated later in Section IV-A.

IV. Application of Noise-Tolerant Techniques to Dynamic Manchester Adder Circuits

To compare the performance of noise-tolerance in the presence of noise, we apply various noise-tolerant techniques in the *8-bit Manchester adder*. The proposed INT technique is applied in the

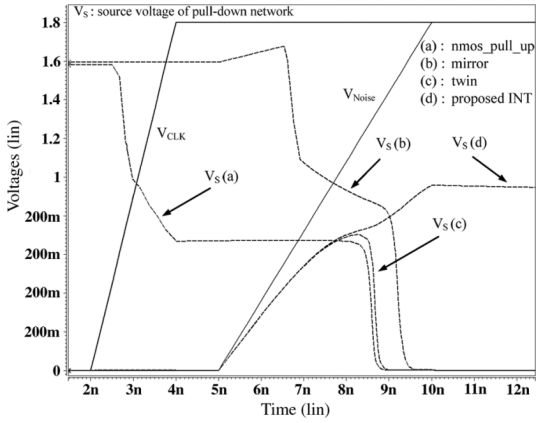

Fig. 8. Source voltage of *NT-transistor* associated with the injected noise.

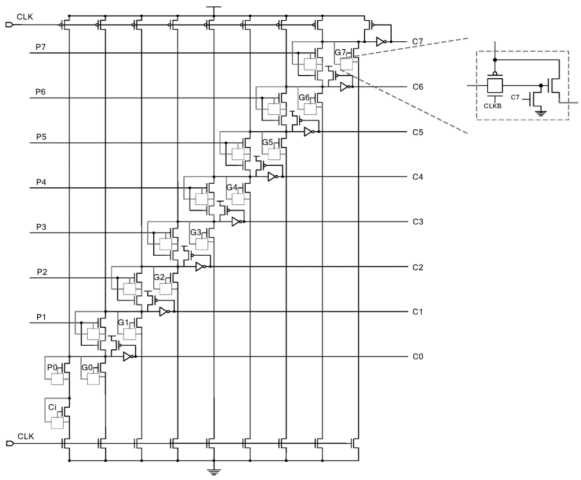

Fig. 9. Proposed noise-tolerant technique is applied in the carry generation chain of *8-bit Manchester adder*.

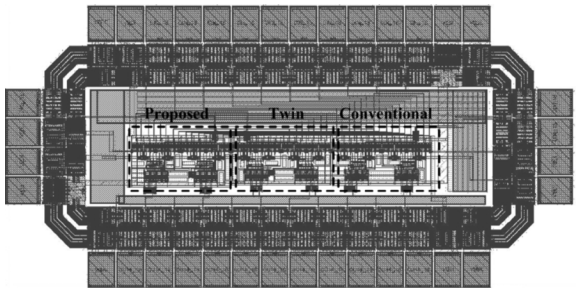

Fig. 10. Chip layout of *8-bit Manchester adder*.

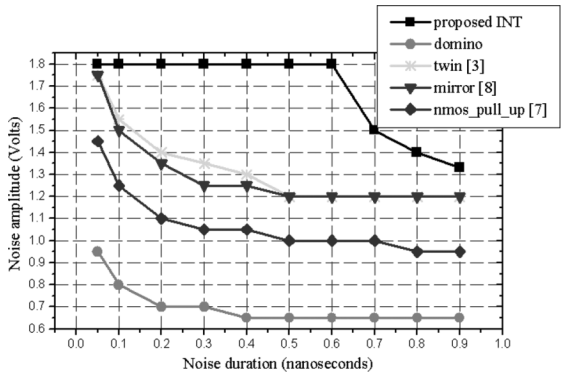

Fig. 11. NICs.

8-bit Manchester adder as illustrated in Fig. 9. In the carry generation circuit, the proposed INT mechanism is constructed by the red block and transistors in blue color are used to solve the direct conducting path problem. Also, we apply the twin-transistor design [3] and the mirror technique [8] in the 8-bit Manchester adder for performance comparison. Fig. 10 is the chip layout of the proposed *INT 8-bit Manchester adder*, the twin-transistor 8-bit Manchester adder, and the conventional Manchester adder. We also layout the mirror 8-bit Manchester adder, but not put in the chip because of pad limitation. Performance comparisons are based on the post-layout simulation performed by HSPICE under TSMC 0.18-μm process with 1.8-V supply voltage.

A. Simulation Comparisons of Noise-Tolerance Performance

1) Noise Immunity Curves and Average Noise Threshold Energy: We can use the *noise immunity curves* (*NICs*) [8], [9] to compare the noise-tolerant capability of various noise-tolerant techniques applied in the 8-bit Manchester adder. This curve is the locus of noise amplitude $(V_{\rm noise})$ and width $(T_{\rm noise})$ combinations that cause the gate output to switch [8]. The NIC method can meet the basic criteria of noise margin and also take the duration of noise into consideration [9].

To have a fair comparison, we set the transistor size of all compared noise-tolerant techniques to have the same minimal carry prorogation delay (190 ps). In Fig. 11, we draw the NIC of various noise-tolerant dynamic circuit designs. The upper NIC curve represents the better noise immunity. As illustrated in Fig. 11, the tolerable noise amplitude in conventional domino circuits is 0.65 V, which is only slightly higher than the transistor threshold voltage. In the nMOS pull-up design, the tolerable noise amplitude is higher than 0.95 V. In the twin-transistor and the mirror noise-tolerant design, the tolerable noise amplitude is enhanced to be higher than 1.2 V. In the proposed INT design, the noise tolerant mechanism is under protection; therefore, the corresponding NIC lies in the most top curve and the tolerable noise amplitude is further enhanced to be higher than 1.3 V. From Fig. 11, it shows that the proposed INT design outperforms all other noise-tolerant designs in terms of NIC index.

2) Tradeoff Between Noise-Tolerance Capability and Operation Speed: The NICs can vary with different NT-size. By increasing the NT-size, the NICs can be raised up to perform better noise immunity. However, the design overhead also increases; especially the delay time of dynamic circuits is increased. We compare the delay time with various SNR as applying different noise-tolerant techniques in Fig. 12. As illustrated in Fig. 12, the mirror technique spends expensive design overhead, 39× NT-size, to operate accurately under 3.2-dB SNR. The design penalty in the mirror design increases abruptly when the SNR is lower than 4.8 dB. This is because that the passive style noise-tolerant design can not effectively take the advantage of NT-transistor in a noise dependent manner.

As for the twin-transistor design, the design overhead under low SNR can be reduced because it takes the advantage of NT-transistor in a noise dependent manner. However, if the noise peak is high, the gate voltage of NT-transistor falls down. The twin-transistor design still need to pay expensive design cost to achieve high noise immunity. As illustrated in Fig. 12, the twin-transistor design still need to pay 23× design overhead of NT-size and 75% speed penalty under 3.2-dB SNR.

In the proposed INT technique, we also enhance the noise-tolerance in an active mode. Furthermore, the gate voltage of noise-tolerant transistor can be maintained to $V_{\rm DD}$. The noise-tolerant ability can be

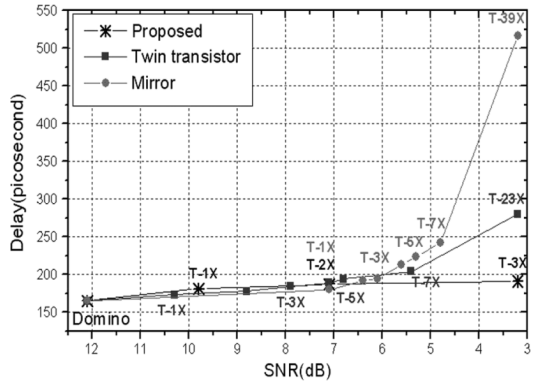

Fig. 12. Tradeoff of the *noise tolerance* against *delay*.

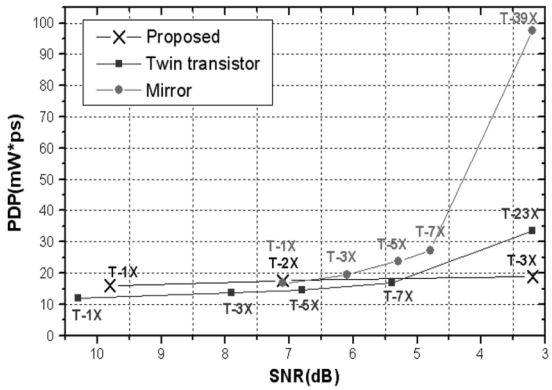

Fig. 13. Tradeoff of the *noise tolerance* against *PDP*.

achieved in a more effective way that the performance sacrifice for enhancing the noise-tolerance is greatly reduced. As illustrated in Fig. 12, the proposed design can provide noise immunity under 3.2-dB SNR with only 3× NT-size and 12.5% speed penalty. In other words, under the same performance sacrifice of speed, the proposed design has better noise tolerant capability.

3) Tradeoff Between Noise-Tolerance Capability and Power Delay Product: In Fig. 13, we further compare the performance penalty in terms of *power-delay-product* for enhancing the noise tolerance. Under 3.2-dB SNR, the PDP in the mirror technique and twin-transistor technique is 97.6 and 33.5 mW·ps, respectively. Under 3.2-dB SNR, the PDP in the proposed INT design is only 18.9 mW·ps. It can save 43.6% performance penalty of PDP as compared to the twin-transistor design. Namely, under the same performance sacrifice of PDP, the INT design has better noise tolerant capability.

B. Performance Summary

We summarize the performance comparisons of various noise-tolerant techniques applied in the *8-bit Manchester adder* in Table I. As illustrated in Table I, the transistor count in the conventional domino Manchester adder is 1128. The transistor count in the INT design is 1206 and the transistor overhead is within 7%. The implementation area in the conventional Manchester adder is 0.102 mm^2. The implementation area in the twin-transistor design, the mirror design and the proposed INT design are 0.157, 0.218, and 0.183 mm^2, respectively. Because the routing complexity is increased in the twin-transistor design, the mirror design and the proposed INT design, the area overhead increases by 54%, 114%, and 79%, respectively.

TABLE I
PERFORMANCE SUMMARY

Implementation Process	TSMC 0.18*um*			
Supply Voltage	1.8*V*			
Clock Frequency	100*MHz*			
Design Type	Domino	Mirror [8]	Twin [3]	INT
Transistor Count	1128	1206	1170	1206
Circuit Area (mm^2)	0.102	0.218	0.157	0.183
ANTE (V^2-*ns*)	0.200	0.687	0.704	1.117
ANTE Improvement	5.85X	1.66X	1.70X	
Delay @SNR=3.2*dB*		517*ps*	280*ps*	191*ps*
Delay @SNR=5*dB*		230*ps*	220*ps*	180*ps*
PDP @SNR=3.2*dB*(*mw***ps*)		97.6	33.5	18.9
PDP @SNR=5*dB*(*mw***ps*)		25	27.3	18
NT-Size @SNR=3.2*dB*		39X	23X	3X
NT-Size @SNR=5*dB*		6X	8X	2.5X

In the aspect of noise-tolerant performance, *average noise threshold energy* (*ANTE*) [8] is a convenient index that can be directly derived from the NIC by averaging the energy of noise pulses that cause the function error. The higher ANTE represents the higher noise energy the circuit can sustain with; in another word, the higher noise immunity the circuit performs. As illustrated in Table I, in the proposed INT technique, the ANTE can be enhanced by 5.85× and 1.66× as compared to the conventional domino design and the twin-transistor design, respectively.

Comparing with different noise-tolerant techniques, the proposed design has a lower delay time and PDP because of noise isolation property. As compared to the twin-transistor design, INT technique can reduce the delay time with 31.8% and 18.2% improvement under 3.2- and 5-dB SNR, respectively. The PDP in INT design can also be improved by 43.6% and 34.1% as compared to the twin-transistor design under 3.2- and 5-dB SNR, respectively.

V. CONCLUSION

In this paper, we develop a new INT technique to enhance noise-tolerance in dynamic circuits. The INT design can maintain the high noise-tolerant capability even under severe SNR environments. The *8-bit INT Manchester adder* circuit can provide 5.85× and 1.66× *ANTE* as compared with the domino circuit and twin-transistor design, respectively. In the seriously noisy environment with 3.2-dB SNR, the proposed design can speed up by 18.2% and save 34.1% performance penalty of PDP as compared to the twin-transistor technique.

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