

Design of a Tri-modal Multi-Threshold CMOS Switch with Application to Data Retentive Power Gating

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Abstract—A tri-modal Multi-Threshold CMOS (MTCMOS) switch design is presented. Similar to the conventional MTCMOS switches, the tri-modal switch comes in two flavors: header and footer. The tri-modal switch provides three different power modes for the underlying circuit, active, drowsy, and sleep. The ability of data retention in the drowsy mode makes the proposed tri-modal switch an excellent candidate for implementing data-retentive power gating designs. We will see that three different low-power design schemes, namely data-retentive power gating, multi-drowsy mode structures, and on-chip dynamic voltage scaling, are implemented using the proposed tri-modal switch. We show that our proposal introduces superior low-power solutions across various circuit operating modes using a single circuitry.

I. INTRODUCTION

POWER reduction is one of the most significant challenges in designing today's advanced VLSI circuits. Low power designs are desirable for various reasons including competent energy and temperature characteristics, higher battery time for portable devices, and lower packaging and maintenance costs.

MTCMOS, aka power gating, technology provides a simple and effective power gating structure by utilizing high speed, low V_t (LVT) transistors for logic cells and low leakage, high V_t (HVT) devices as sleep transistors [1]. MTCMOS circuits suffer from some drawbacks such as long wakeup latency, large amount of rush-thru current, and wasteful energy usage during mode transition [7]. In addition, due to data loss in the sleep mode, MTCMOS circuits usually use a data retention strategy to restore the pre-sleep state which they cannot afford to lose. In particular, regular flip-flops are replaced by retention flip-flops, preserving the pre-sleep state. Retention flip-flops that are larger cells in terms of area, introduce a significant amount of area overhead in designs that require substantial amount of data retention.

In this paper, we present a power gating scheme that implements data retention without requiring retention flip-flops. The proposed technique benefits from a new tri-modal MTCMOS switch design, in the form of header or footer, which can operate in three different modes: active, drowsy, and sleep. We will show that the drowsy mode, an intermediate power saving mode, reduces the leakage current while preserving the content of the cell. We will also see that the proposed power gating circuitry can be used to reduce dynamic power consumption in the active mode by implementing voltage scaling. This improves the *Total Power Saving Factor (TPSF)*—a metric that measures the overall quality of a low power technique and will be defined later in this paper (cf. Section IV.D).

There have been a number of studies on implementing intermediate modes for standby power-saving. In [4], the authors propose a power gating structure to support a drowsy mode and the traditional sleep mode. The idea is to add a clamping PMOS transistor in parallel with each NMOS sleep transistor. By applying zero voltage to the gate of the clamping PMOS and NMOS sleep

transistors, the circuit can be put in the intermediate power saving mode whereby leakage reduction and data retention are both realized. The circuit structure proposed in [4] enables only one additional drowsy mode where the voltage gap across logic circuit is reduced from VDD to $VDD - |V_{tp}|$ and V_{tp} denotes the threshold voltage of the PMOS transistor connected in parallel to the NMOS sleep transistor. In contrast we will see that our proposed switch enables a continuous range of virtual ground voltages, V_x , depending on sizing of various transistors in our design. This gives us the ability to set the voltage drop across logic circuit, $VDD - V_x$, to any value.

The work in [5] describes multiple power modes for the circuit, but it needs multiple supply voltages (stable reference voltages to drive the gate terminal of the sleep transistor which operates in different points of the subthreshold conduction region during the sleep mode). This is a costly proposition due to using multiple supply voltages. In [6], the authors propose a drowsy circuit scheme that automatically controls the degree of the drowsiness of the circuit by using a negative feedback implemented with a sleep inverter. This configuration thereby clamps the voltage level of the virtual ground node using the negative feedback loop. The problem with using this technique is that the circuit will either work in the active or drowsy mode, and the sleep mode is lost. This technique works fine for small standby periods when the circuit switches back and forth between standby and active periods frequently. However, for medium to long standby periods, the technique in [6] fails to be effective due to the large amount of leakage consumption.

II. TRI-MODAL SWITCH

In this section we present the circuit configuration and functionality of the header and footer tri-modal switches. Readers interested in more detailed discussions on different issues about tri-modal switch including data retention capability and transistor sizing are referred to [2].

A. Circuit Configuration and Switch Functionality

Figure 1 shows the proposed footer type tri-modal switch. We use thick lines to draw the gate plate of HVT transistors. As seen in Figure 1, the proposed tri-modal switch has two input signals called SLEEP and DROWSY. This switch enables three different circuit operation modes: sleep, drowsy, or active, depending on the value of the two control signals (cf. TABLE I). When SLEEP = '0', MS1 is ON and the voltage level at GS is VDD. Thus, independent of the value of the DROWSY input, the MS transistor is ON and the circuit is in the active mode. When SLEEP = '1', the tri-modal switch operates in the sleep or drowsy mode depending on the value of the DROWSY signal. In particular, if DROWSY = '0', MS2 and MD2 will both be ON, MS is OFF, and the tri-modal switch cell will operate in sleep mode. If SLEEP = DROWSY = '1', MS2 and MD1 will be ON, creating a negative feedback between VVSS and GS nodes which puts the circuit block into the drowsy mode (see TABLE I.)

In the sleep mode, the sub-threshold leakage of the circuit block is

limited by OFF HVT devices MS and MD1 that lie on the two parallel paths from VVSS to Ground. Thus the leakage current is negligible. However, in this case, there also exists a *sneak path* from VDD to the ground through MS1, MS2, and MD2. Since MD2 is ON, if needed, one may replace MS1 and MS2 with HVT devices to limit the leakage current through this sneak path. In the drowsy mode, since MD2 is OFF, there is no sneak path through MD2, and the total leakage current from VVSS to Ground is equal to leakage through partially OFF HVT transistor MS.

Defined for a circuit operating in sleep or drowsy modes, the wakeup and ready latencies (shown by t_w and t_r) measure the delay between the time when the SLEEP signal crosses the 50% VDD level as it makes a transition to low state and the time when the VVSS node reaches 5% of the VDD level as it is discharged to zero.

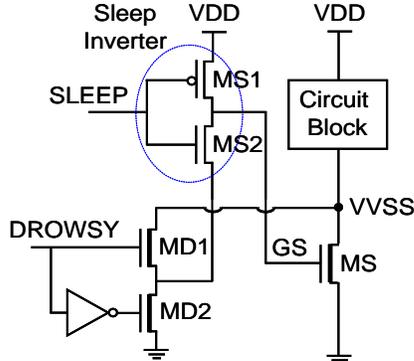


Figure 1. Implementation of the tri-mode footer cell.

TABLE I: TRI-MODE SWITCH FUNCTIONALITY

SLEEP	DROWSY	Switch Function (Block Mode)
0	X	Active
1	0	Sleep
1	1	Drowsy

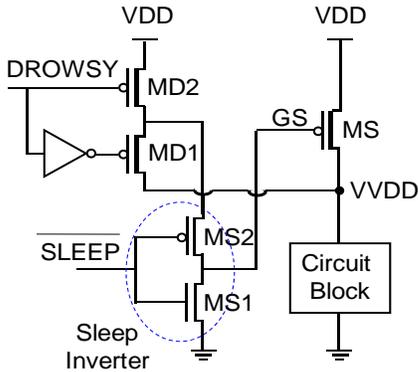


Figure 2. Implementation of the tri-mode header cell.

Notice that since the drowsy signal changes only during sleep to drowsy or drowsy to sleep transitions, it need not be fast. Therefore, the always-on inverter that receives the DROWSY input in Figure 1 may be implemented with HVT devices for leakage saving. The transistor count overhead of the tri-modal switch is only four (MD1, MD2, and the two transistors inside the inverter that feeds into gate terminal of MD2) compared to a regular bimodal MTCMOS switch. This is because the two transistors inside the sleep inverter, MS1 and MS2, are already used in (conventional) bimodal power gating structures. In [2] we explain that, independent of the circuit block or the sleep transistor size, all additional transistors may be chosen to have minimum size; therefore, the actual area overhead of the proposed switch is quite small. The circuit configuration and functionality of the tri-modal header is similar to the footer and are

provided in Figure 2 and TABLE I.

III. TRI-MODAL SWITCH APPLICATIONS

In this section we present some applications of the tri-modal switch.

A. Data-Retentive Power Gating

By controlling the SLEEP and DROWSY signals for different tri-modal switches in the circuit, we can selectively put various circuit elements in different modes. Consider a K-stage pipeline structure with K-1 pipeline registers as shown in Figure 3. We perform power gating for this structure by using the proposed tri-modal switches, where we have two types of switches: ones disconnecting VVSS net of the flip-flops in pipeline registers from the ground rail and those disconnecting VVSS net of the combinational logic cells in the design from VSS. This implies having two different VVSS nets: one for the flip-flops and another for the rest of the logic cells. Suppose the design is to be implemented in a standard cell layout style. Cells fit in one of two groups: (i) pipeline registers (FF's), and (ii) combinational logic cells. If the pre-standby stored data in the pipeline registers is to be retained when going to sleep, the pipeline registers must be put into the data-retentive drowsy mode while the rest of the cells in the circuit are put in the sleep mode to reduce standby leakage. Depending on the state of each switch type, the circuit can be in one of the four modes, Active (when both switches are active), Drowsy (when both switches are drowsy), Data Retentive (when logic switch is in sleep and FF switch in drowsy), and Deep-Sleep (when both switches are in sleep).

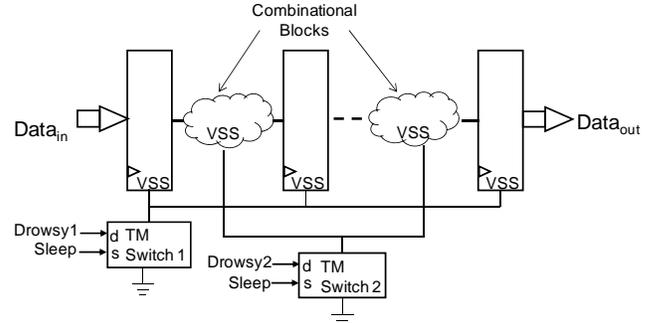


Figure 3. Application of tri-modal switch in designing multimodal pipeline structures.

To realize this architecture, placement of the cells in the design has to be in such a way that the VVSS rail used for pipeline FF's is separated from the VVSS rail used for combinational logic cells. This is possible by disconnecting the VVSS rail every time a FF is placed next to a logic cell. This can cause a large number of breaks and reconnections in the VVSS rail. To solve this problem, we modify the original placement by moving the cells such that in each row, there are at most a few contiguous sections of FF's and a few contiguous sections of logic cells.

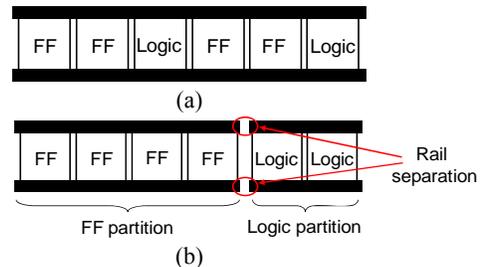


Figure 4. Examples of (a) illegal and (b) legal placements.

Figure 4 shows a legal and an illegal placement. In this particular example, all the FF cells have been placed in one section. It is possible, however, that we have multiple FF and logic sections in

each row. Whenever we have a legal placement with a number of sections in the same row, e.g. Figure 4.(b), the virtual ground rail has to be disconnected at the point where two adjacent sections meet. Interested readers are referred to [2] for detailed explanations of how to remove placement conflicts in a row such that total overhead due to removing illegal placements is minimized.

B. Multi-Drowsy Mode Circuits

The VVSS voltage value in drowsy mode depends on the threshold voltage and the width of MS. Larger width and lower threshold voltage values for MS results in lower VVSS drowsy voltage value. Figure 5 shows a multimodal switch that is designed by using multiple sleep transistors and using different SLEEP signals to turn them ON or OFF. Suppose that all the sleep transistors in Figure 5, i.e., MS1-MS_n, are HVT. In the active mode, all the sleep signals have logic “0”. In the sleep mode, however, the DROWSY signal has logic “0” value and all the sleep signals are “1”. In the drowsy mode, DROWSY=“1”, and turning on less number of sleep transistors, i.e., a larger effective sleep transistor size, results in higher VVSS voltage value and thus, lower leakage current in the drowsy mode. Similarly, we can use different threshold voltage values for MS1-MS_n to achieve multi-drowsy mode implementation.

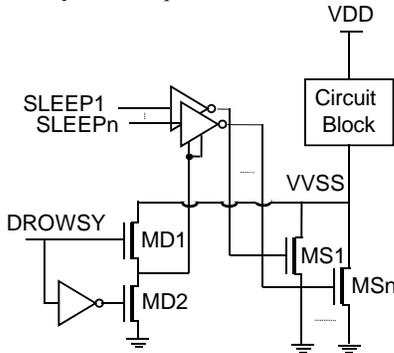


Figure 5. Implementations of multimodal footer switch for multi-drowsy mode circuits.

One of the advantages of using the proposed multimodal switch is preventing huge amount of rush-thru current at the edge of sleep to active transition. The proposed multimodal switch can be used in a similar fashion as in mother-daughter MTCMOS switches (cf. [8]) to avoid large rush-thru currents by correctly sizing the sleep transistors (MS_i's) and appropriately timing them.

C. Voltage-Scaling Using Multimodal Headers

DC-DC converters are used to supply power in most digital systems. They are typically classified in two types: linear and switching voltage regulators [9]. Switching voltage regulators usually achieve better power efficiency compared to linear regulators; however, linear regulators are much cheaper and generate less noise. Linear regulators are also faster and can be implemented on-chip.

In this section we present an application of the proposed multimodal switch in designing a special type of linear regulator that can be used in enabling on-chip Dynamic Voltage Scaling (DVS) for VLSI circuits. Consider the circuit shown in Figure 6 which is a circuit block with multimodal header switch. Suppose that the circuit is in drowsy mode, that is DROWSY=“1” and at least one of the sleep signals (SLEEP_i's) is “1”.

Similar to what we discussed in Section B, we can provide different voltage levels at VVDD node in the drowsy mode by changing the effective size (or threshold voltage) of the sleep transistor. This is done by turning ON or OFF different number of sleep transistors in the multimodal switch (MS_i's in Figure 6).

The capacitor, C_{VVDD}, in Figure 6 is to stabilize the VVDD voltage

when there are switching activities inside the circuit block. Even though more sophisticated techniques can potentially result in improved I-V characteristics, they are out of the scope of this paper, and we only consider a simple capacitor as the voltage stabilizer as shown in Figure 6.

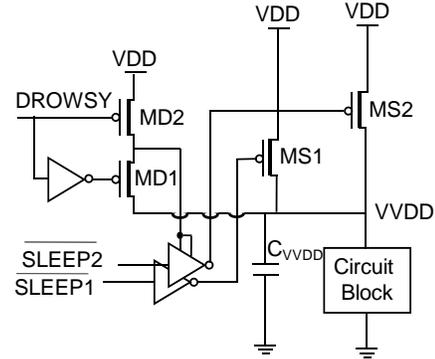


Figure 6. Using multimodal header to perform voltage scaling.

The presented approach for VDD scaling is specifically suitable for implementing local DVS where global DVS is less effective. For example, in the existence of latency imbalances of pipeline stages, the effectiveness of global DVS decreases leaving some power saving opportunities for local DVS, where different scaling factors are used for different stages [10]. In other words, instead of constraining pipeline voltage to single global voltage (as it is done in global DVS) and changing that global value, local DVS supplies separate voltage values for different pipeline stages using locally adjustable voltages. Therefore, the energy demand for each pipeline stage is minimized individually. Local DVS shows better energy saving compared to global DVS, but the downside is that now each stage has to have its own voltage regulator. Level converters are also required between two stages. Our presented DVS scheme can be used to implement local DVS for different stages of a pipeline using their power gating circuitry. This reduces implementation cost of the local DVS by eliminating voltage regulators of different stages.

IV. SIMULATION RESULTS

In this section we present the simulation results for different tri-modal switch applications discussed in this paper. For this purpose we designed and implemented a 16×16 pipelined Carry Save Multiplier (CSM). The circuit is divided into two pipeline stages. The 46-bit output of the first stage is latched into the pipeline registers (46 FF's). The first 16 bits out of these 46 bits, which make the least significant bits of the product, are directly passed to the output. The last 30 bits are passed to the second stage to make the most significant bits of the product.

We implemented the 16×16 pipelined CSM in structural Verilog and synthesized the design using the Synopsys Design Compiler with a standard cell library in IBM90nm, V_{DD}=1.2V. Timing analysis resulted on the worst-case stage delay of 2.3ns (clock frequency of 435 MHz). Cadence System on Chip (SoC) Encounter was used to place and route the design. The tri-modal switch cells were manually inserted into the design. Finally, we extracted the netlist and performed HSPICE simulations. Note that we used these rather old CMOS technologies since we do not have access to physical views of the cell libraries in more current CMOS technology nodes (say 35nm). These libraries are needed to implement the CSM.

A. Data-Retentive Power Gating: Results

We compare the leakage current, ground bounce and wakeup/ready latencies for four different cases: a) CMOS, b) MTCMOS: deep-sleep, c) MTCMOS: drowsy, and d) MTCMOS: data-retentive.

No power gating is used for the CMOS circuit and there is no constraint for placement of the FF's. During the active mode, all tri-modal switches are in the active state (SLEEP="0", DROWSY="X") in all versions of MTCMOS circuit. In the standby mode, however, tri-modal switches are put in different states: in deep-sleep MTCMOS, all tri-modal switches are in the sleep mode (SLEEP="1", DROWSY="0"), in drowsy MTCMOS all tri-modal switches are in the drowsy mode (SLEEP="1", DROWSY="1"), while in data-retentive MTCMOS, tri-modal switches used for combinational logic cells are in the sleep mode and tri-modal switches used for FF's are in drowsy mode. We use different metrics to compare the four versions of the 16×16 pipelined CSM.

The results are shown in TABLE II. The second, third, and fourth columns show the standby leakage current, the peak ground bounce (GB) value, and the wakeup/ready (w/r) latencies for all circuit configurations explained above, respectively. The peak ground bounce value is measured as the maximum voltage jump at the VVSS rail in the turn-on event. As it is shown in the table, the deep-sleep MTCMOS circuit has the lowest leakage among all configurations, making it the most appropriate choice for long standby periods. We note that the leakage of the drowsy MTCMOS is 77% lower than that of the CMOS circuit and higher than that of the deep-sleep. The ground bounce for deep-sleep circuit is much higher than that for drowsy circuit. Therefore, the drowsy circuit provides a reasonably low-leakage solution with very small wakeup latency and ground bounce.

TABLE II: LEAKAGE, GROUND BOUNCE, AND W/R LATENCY COMPARISONS IN 90NM TECHNOLOGY WITH VDD=1.2V

Circuit Type	Leakage (μA)	Ground-Bounce (mV)	Wakeup/Ready Latency (ns)
CMOS	150	-	-
Drowsy	35	111	2.1
Data-Retentive	2.35	296	9.3
Deep-Sleep	0.6	362	9.3

Although, we do not consider the gate leakage in this paper directly, it is generally understood and agreed that reducing the voltage drop across the VDD and VVSS (or VVDD and VSS) will not only reduce the sub-threshold leakage, but also combats the gate leakage since this current component is dependent on the voltage applied to the devices [4].

Now assume that the maximum tolerable ground bounce is 100mV ($\approx 0.08 \times V_{DD}$). This constraint automatically limits the peak rush-thru current. To ensure that the actual ground bounce is lower than this limit, one way is to resort to a multi-cycle turn-on strategy similar to the one presented in [3], where we turn on only a portion of tri-modal switches at each clock cycle. In particular, 4/30, 6/30, 9/30, and 11/30 fractions of the tri-modal switches are turned on during the first, second, third, and fourth consecutive clock cycles, respectively. Using this turn-on strategy, we need 4 clock cycles to wake up the deep-sleep circuit while it only takes one clock cycle for the drowsy circuit to wake up. This is because we can turn on all the tri-modal switches in the drowsy circuit simultaneously without violating the given constraint of the maximum tolerable ground bounce. Now assume this multiplier is used in the execution stage of a five-stage pipelined processor, and has been put into the deep-sleep mode by the power-management unit due to low recent activity. A new instruction in the IF stage requesting to use this multiplier will stall the processor for three clock cycles until the multiplier is ready for operation. However, if the multiplier was in drowsy mode, and a new instruction in IF stage was requesting the multiplier, the processor could perform its regular operation without being stalled at all. The cycle penalty will increase as the size of the circuit increases.

Despite having a faster wakeup, the drowsy circuit suffers from

higher leakage compared to the deep-sleep circuit. Therefore, for longer standby periods when the leakage energy dissipation becomes an issue, we may want to pay the wakeup cycle penalty to achieve low leakage dissipation. In that case, deep-sleep or data-retentive modes are more preferable than the drowsy mode.

B. Multi-Drowsy Mode Circuits

Based on the discussion that we had in Section III.B, multimodal headers can be used in implementing circuits with multiple drowsy modes. This part of the experimental results demonstrates the implementation of this idea for some benchmark circuits.

For each circuit we use a multimodal header with two sleep transistors of equal size and different threshold voltages. Therefore, there are two different drowsy modes for each circuit. Considering active and sleep modes, this adds up to four different available power modes for each circuit. In the active mode both sleep transistors are ON providing the maximum current capacity for the circuit in case of any switching event.

TABLE III: READY LATENCIES FOR MULTI-DROWSY ISCAS85 CIRCUITS IN 90NM TECHNOLOGY WITH VDD=1.2V

Circuit	Ready/Wakeup Latency (ns)			Ready to Wakeup Increase (%)	
	Drowsy1	Drowsy2	Sleep	Drowsy1	Drowsy2
9sym	1.72	2.14	2.74	59	28
C432	2.16	2.79	2.87	33	3
C880	1.76	2.10	2.53	43	21
C1355	1.61	1.92	2.44	51	27
C3540	1.59	1.88	2.20	38	17
Avg.	-	-	-	45	19

TABLE III shows the ready latency values measured for the two drowsy modes for different benchmark circuits in 90nm technology. TABLE V shows leakage current values and leakage savings for different modes for the same circuits as in TABLE III. Leakage current in TABLE V is averaged over 1000 different input cases, where a random input vector is applied to the underlying circuit in each case. It can be seen that an average of 50%, 71%, and 91% leakage saving is achieved for Drowsy1, Drowsy2, and Sleep circuits, respectively. By comparing results shown in TABLE III and TABLE V, we realize that Drowsy1 provides relatively smaller leakage saving, but a much faster ready latency compared to Drowsy2 making it more convenient for smaller idle periods. Having different power modes with different characteristics available gives designer the opportunity of coming up with solutions that consume less amount of power and show faster response time.

C. Voltage Scaling

TABLE IV:

ACHIEVING DIFFERENT SCALED SUPPLY VOLTAGE VALUES FOR CSM

Transistor/mode	Scaled VDD Achieved (V)	Dynamic Power (mW)
MS1/Drowsy	0.91	2.24
MS2/Drowsy	1.0	2.71
MS1+MS2/Active	1.2	3.96

TABLE IV shows different scaled voltage levels achieved by using a multimodal switch with two parallel sleep transistors, MS1 and MS2, for the CSM circuit in 90nm technology and VDD=1.2V. The two HVT sleep transistors used have widths of $W_{MS1}=130\mu\text{m}$ and $W_{MS2}=1300\mu\text{m}$. The value of the off-chip capacitor is $C_{VVDD}=10\text{pF}$. The first column shows the sleep transistors involved in achieving the scaled VDD and their operation mode while the second column presents the value of the scaled VDD itself. The third column represents the average power consumption for 1,000 random transitions applied to the CSM inputs. Note that the clock frequency

is kept fixed and the circuit is functional in all cases.

D. Total Power Saving Factor Measure by Way of an Example

We define the *Total Power Saving Factor* (TPSF) for a circuit, c , that uses a power saving technique, lp , as follows:

$$TPSF(c, lp) = \sum_i \alpha_i(c, lp) \tau_i(c)$$

where $\tau_i(c)$ is the fraction of time that circuit c is spending in mode i ($\sum_i \tau_i(c) = 1$), $\alpha_i(c, lp)$ is the amount of power saving achieved by applying lp to c in mode i ($0 \leq \alpha_i < 1$), and the summation is taken over all possible modes in which circuit c operates. This coefficient can be used to compare the overall quality of different power saving techniques. In this section we use the TPSF measure to evaluate different power saving schemes.

Suppose that we use the CSM discussed in Section IV.C in three operating voltage values, namely 1.2V, 1.0V and 0.91V. Furthermore, assume that 35% of the time the CSM block works at full performance (VDD=1.2V), 30% of the time at medium performance (VDD=1.0V), 15% of the time with low performance (VDD=0.91V), and for the remaining 20% of the time, it is idle (i.e., it is in the Sleep mode). Moreover, suppose that the CSM activity factor remains unchanged under different active modes, and that the clock frequency is scaled by the same factor as the supply voltage. The TSPF for the CSM is calculated as follows (mm stands for multimodal):

$$TPSF(CSM, mm) = \sum_{i=1}^4 \alpha_i(CSM, mm) \tau_i(CSM)$$

Substituting the abovementioned information, we will have:

$$TPSF(CSM, mm) = 0 \times 0.35 + 0.43 \times 0.30 + 0.57 \times 0.15 + 1 \times 0.2 = 0.4145$$

where we have assumed that because of power gating, the amount of leakage in the sleep mode is negligible. Now consider the case that the CSM employs only DVFS using conventional approaches. In this case, the multiplier will operate at VDD=0.91V (lowest power state) during its idle period, and we have:

$$TPSF(CSM, dvfs) = 0 \times 0.35 + 0.43 \times 0.30 + 0.57 \times 0.35 = 0.3285$$

Finally consider the case where we use conventional (bi-modal) MTCMOS. In this case, the CSM always works at the maximum supply (VDD=1.2V) and the power saving is only due to leakage reduction in the sleep mode. The TPSF is calculated as:

$$TPSF(CSM, mtcmos) = 1 \times 0.2 = 0.2$$

It is seen that the multimodal CSM performs much better than others, i.e., $(CSM, mm) > TPSF(CSM, dvs) > TPSF(CSM, mtcmos)$. This is because we are able to reduce power consumption of the circuit in different modes using the same structure.

V. CONCLUSION

We presented a tri-modal MTCMOS switch design enabling three different modes: active, drowsy, and sleep. Header and footer style designs of the tri-modal switch were provided and three applications of the proposed tri-modal switch were presented: data-retentive power gating, multi-drowsy mode circuits, and on-chip DVS. The presented results prove a wide range of applications for the proposed tri-modal switch. We showed that the tri-modal switch makes it possible to achieve superior power-saving capabilities using the same circuit structure in different modes; thus, increasing the TPSF.

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TABLE V: LEAKAGE CURRENT FOR VARIOUS MODES IN MULTI-DROWSY IMPLEMENTATION OF ISCAS85 CIRCUITS IN 90NM TECHNOLOGY WITH $V_{DD}=1.2V$

Circuit	# of Cells in Design	Total Sleep TX Width (μm)	Leakage Current (μA)				Leakage Saving (%)		
			Standby	Drowsy1	Drowsy2	Sleep	Drowsy1	Drowsy2	Sleep
9sym	276	99	3.9	2.5	1.5	0.7	37	61	83
C432	204	73.4	7.1	3.2	1.9	0.5	55	73	93
C880	432	155.5	14.9	6.8	4.1	1.0	54	73	93
C1355	526	189.4	17.9	7.8	4.0	1.3	57	78	93
C3540	1295	466.2	45.6	23.5	13.9	2.9	49	70	94
Average	-	-	-	-	-	-	50	71	91