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An Information Theory Perspective for the Binary STT-MRAM Cell Operation Channel

Jianxiao YANG[1], BenoitGELLER[1], Meng LI[2], and Tong ZHANG[3]

***Abstract*—Spin-torque transfer magnetic random access memory (STT-MRAM) has emerged as a promising non-volatile memory technology, with advantages such asscalability, speed, endurance and power consumption. This paper presents a STT-MRAM cell operation channel model with write and read operations for information theorists and error correction code designers. This model takes into account the effects of process variations and thermal fluctuations and considers all principle flaws during the fabrication and operation processes.With this model, evaluations are not only made for the write channel, the read channel, but alsothe write and read channel with metricssuch as operation failure rate, bit error rate, channel ergodiccapacity and channel outage probability at certain outage capacity. Moreover, it is proved that the distributions of written-in bit states are not uniformly distributed andare proportional to their respective write success probabilities. Finally, simulation results show that practical code rates and code block lengths can guarantee reliable performances only if the operation success rate difference between state '1' and state '0'is small enough.**

***Index Terms*—Spin-Torque Transfer Magnetic Random Access Memory (STT-MRAM), Non-Volatile Memory (NVM), Error Correction Code (ECC), Write Operation, Read Operation, Channel Model, Operation Failure Rate, Bit ErrorRate (BER), Channel Ergodic Capacity, Channel Outage Capacity, Channel Outage Probability.**

I. INTRODUCTION

SPIN-TRANSFERtorque magnetic random access memory (STT-MRAM) has become one of the most promising candidate for nextgeneration memory in terms of high-speed, nonvolatility and ultra low-power consumption. All these features make STT-MRAMextremely attractive to become general memories (cache, main memory, disk) for mobile devices.

However, STT-MRAM suffers from process variations such as MOS transistor device variations, magnetic tunneling junction (MTJ) geometry variations, and resistance variations, which become even more critical as the technology scales down. Moreover, as many electronic devices, STT-MRAM suffers from random thermal fluctuations which are independent of the device process variations.Therefore, complementary to making a difficult cell optimization among different technical parameters mutually correlated, it is possible to reduce the design complexity and tolerate a certain level of device imperfection by introducing another degree-of-freedom, *i.e.*,error correction codes (ECC) [1],[2].

In order to design asatisfying ECC, the STT-MRAM cell channel needs to be carefully modeled and investigatedby obtaining metrics such asoperation failure rate, bit error rate (BER), channel ergodiccapacity and channel outage probability at certain outage capacity. This model is extremely important for the efficient selection ofboth the code rate and the code lengthin order to meet the practical performance requirements.The scientific canvas for this design is information theory; STT-MRAM is then considered as a device having an input (*i.e.*, the original information) and an output (*i.e.*, a resistance corresponding to the written/read out information), the output being statistically linked to the input through the physical properties of the media. For more distorted channels, more redundancy should be added by the ECC, *i.e.* the code rate between the real informationand the coded bits (information and added redundancy) should be lower and Shannon postulated that an asymptotically small error can be achieved if the code rate is less than the channel capacity[3]. However, there are very few works correlating the ECC design with the cell channel.[4] modeled the STT-MRAM operation channel as an asymmetrical resistance variation channel; both the influence ofthe write and read failures, and the process variations are considered as factors enlarging the standard deviations of resistance distributions which is over-simplifying as the write and read failures are nonlinear processes.Moreover, [5]proposed an asymmetric write channel model taking into account process variations and thermal fluctuations. However, in a STT-MRAM memory system, the write and the readoperations are both important and each of these functions must be modeled carefully; actually the optimization on either the write or the read operation generally does not lead to a global optimization and technical parameters are usually selected to balanceboth write and read performances to reach a global optimum performance.Taking the transistor width as an example, the selection of the transistor width generally determinesthe current drive capacity;on one side,the write operation needs a large current to target the magnetization as

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quickly as possible, andthe read operationrequires a sufficient current to drive the sense amplifier as fast as possible;on the other side,the read current should be kept small enough to avoid flipping the cell content.Differently from [4][5], [6] proposed an optimization technique to minimize both read and write failures and developed a mixed-mode framework to optimize the bit-cell level reliability. This framework captured the transport physics by using the non-equilibrium Green's function method, solved the MTJ magnetization dynamics with the Landau-Lifshitz-Gilbert (LLG) equation, and performed bit-level optimization with HSPICE. [7]dealt with the reliability issues by analyzing the impact of the nonpermanent "soft-errors"introduced by various operations,as well as thepermanent "hard-errors" caused by permanent device damages.[6]and[7]concentrate on hardware design in order to optimize the memory performance.However, such a performance level can also be reached by using an additional degree-of-freedom - a properly designed ECC[1],[8]-[13]; the hardware design complexity can thus tolerate a certain level of unreliability that will be improved by ECC.

Differently fromthe previous works[4]-[7], this paper intends to propose a channel model to simulatethe reliability of the basic STT-MRAM cells write and read operationsby taking into account both the process variations and thermal fluctuations(without considering the impact of "hard-errors");also differently from the compact models [14]-[18], this model targets to bridge the gap between the information theory community and the physical device community by taking into account various process variations and thermal fluctuations without solving any complex equations.Moreover, aiming at an efficient ECC design, operation failure rates, bit error rates and channel capacitiesareevaluated.Comments are also made for the highly asymmetrical characteristics of the STT-MRAM channel. Finally, suggestions are made for the selection of both the code rate and the code block length.

The rest of the paper is organized as follows. The basics of STT-MRAM cell operations, various process variations, thermal fluctuations and capacity definitions arebriefly reviewed in Section II. The proposed channel model including both write and read operations isdetailed in Section III. Simulation and numerical results are given in Section IVwith comments on ECC design. Finally, conclusions are made in Section V.

II. STT-MRAM CellOperations

A. STT-MRAM Cell Basics

A datum in a STT-MRAM cell is represented as the resistance state ofa magnetic tunneling junction (MTJ) device, which can be switched by applying programming currents with different polarizations[19],[20]. A widely used STT-MRAM cell structure is displayed in Fig.1 and the so-called "1T-1MTJ" structure consists of one transistor and one magnetic tunneling junction, where a tunneling oxide layer (see the grey bars in Fig.1) is sandwiched between two ferromagnetic layers; one of these layer is called reference layer (RL) and has a fixed magnetization and the other layer is called free layer (RL) with two possible magnetizations to represent a bit.

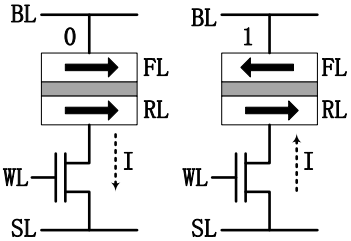


Fig.1. STT-MRAM 1T-1MTJ cell structure: (a) bit "0".(b) bit "1".

Writing a "0" or writing a "1" to a cell is achieved by applying reversed direction currents.When writing "0" (MTJ in parallel state), the word line (WL) and bit line (BL) are connected to the supply voltage V_{DD}, and the source line (SL) is connected to the ground (see Fig.1.(a)). The NMOS transistor is either working in its saturation regionfor a small transistor width or in its linear region for a large transistor width. When writing "1" (MTJ in anti-parallel state), WL and SL are connected to V_{DD}, while BL is connected to the ground (see Fig.1.(b)). The transistor is then working in its saturation region.

There are two ways to read a cell, the so-called parallel (P) direction read with the same direction as writing "0", and the anti-parallel (AP) read with the same direction as writing "1". Inthe parallel direction reading, a low voltage is applied between BL and SL. After activating WL, a current flows from BL to SL.In the anti-parallel direction reading, the voltage polarity applied to BL and SL is switched and a current flows in the reversed direction - from SL to BL.

B. CMOS Process Variations

The CMOS process variations contribute to the variability of the driving strength of the NMOS transistor due to random dopantfluctuations, line-edge roughness, shallow trench isolationstress, and geometry variations of the transistor channel length/width[21]. All these process variations have a direct impact over the transistor's threshold voltage V_{TH} and its equivalent resistance.

C. MTJ Process Variations

The MTJ process variationsare independent from the CMOS process variations and lead to the variability of the MTJ. Thesevariationsstem from the MTJ shaping variations, from the oxide thickness variation, and from the localized fluctuation of magnetic anisotropy[22]. The first two factors cause thevariations of the MTJ resistance and of the MTJ switching current by changing the bias conditions of the NMOS transistor, whereas the third factor is an intrinsic variation of the magnetic material that both affects the MTJ'scritical switching current density J_{C0} and the magnetization stability barrier height.

D. Random Thermal Fluctuations

In general, the magnetization dynamics of the MTJ switching affected by thermal fluctuations can be modeled by the famous

Landau-Lifshitz-Gilbert (LLG)equationby considering thethermal agitation fluctuating field[23].Due to the random thermal fluctuations, the MTJ switching time becomes unrepeatable and is independent of the process variations.

It has been found that switching modes in MTJ are categorized as a function of the switch current duration and can be classified into three distinct modes[24]: thermal activation, dynamic reversal and precessional switching.

For a long current pulse(longer than 10 ns), the magnetization switching is a thermally activated process. In this regime, the magnetization switching is independent of the initial conditions and is only determined by thermal agitation during the switching process.

For a very short switch current duration(shorter than 3 ns), the magnetization switching is precessional switching and is mainly dependent on the initial thermal distribution. In this regime, both the magnetization switching distribution and the switching probability are independent of the thermal agitation during the switching process.

For an intermediate current pulseduration (between 3 ns and 10 ns), the magnetization switching is dynamic reversal[24]and is determined by the initial thermal distribution and bythe thermal agitation during the switching process.

E. Write Variations

During the write operation, two kinds of failures can occur :

1) The cell fails to be flipped from 0 to 1 and keeps the 0 state while anti-parallel writing is performed;

2) The cell fails to be flipped from 1 to 0 and stays at the 1 state when parallel writing is performed.

These failures come from two factors that can lead to the variation of the MTJ switching current and thus result ona switching time uncertainty [25]: one factor is the CMOS transistor and MTJ process variations, which causea driving ability variation of the transistor; the other factor is therandomthermal fluctuations, inducing a stochastic MTJ magnetization switching process[23].

Moreover, these two factors leadto a high asymmetry between the two writing state transitions $0 \to 1$ and $1 \to 0$. The bias difference condition [26]of the transistor causes that the $0 \to 1$ transition requires a longer time to perform the transition compared to the $1 \to 0$ transition, and the standard deviation(STD) of the transition $0 \to 1$ is much broader thanthe one of the transition $1 \to 0$ [27]. Therefore the write operation $0 \to 1$ contributes prominently to writing failure events [26]and is considered as an "unfavorable" switching direction.

F. Read Variations

One must achievea compromise on setting a proper read current[6],[7],[28] for the read operation: on one side, the read current requiresto be high enough to generate a sufficient sense voltage margin to drive the sense amplifier and to ensure a fast read access time; on the other side, the read current must be kept low enough so as to avoid flipping the stored state to the reversed one.

Therefore, three types of errors can occur during the read operation:

1) The cell stores a 0 but is read out as a 1;

2) The cell stores a 1 but is read out as a 0;

3)The cell stores a 0 (*resp.* 1) but is flipped to 1 (*resp.*0) during an anti-parallel (*resp.*parallel) read operation.

The first two error types come from the process variations of the cell MTJs and transistors, when compared to a reference resistance which is assumed to be ideal with neither process variations nor thermal fluctuations; the third error type stems from too large read current flipping the MTJ cell state.

G. Channel Capacity

In order to design an efficient ECC with reliable performance for STT-MRAM systems, not only should the operation failure ratesbe measured, but also the operational channel capacity, *i.e.*, the maximum ratio that can be reliably written into and read out from 1T-1MTJ cells, needs to be evaluated.

For the STT-MRAM write and read channel, the capacity can be written as:

$$C = \max_{\{p(x)\}} \{ I(X;Y) \}, \tag{1}$$

where $X = \{0,1\}$ is the input of the channel, and Y is a continuous output resistance value.

Since the a priori information about the input bit X is highly content dependent, it is reasonable to assume an equiprobable distribution for X , *i.e.*, $p(x=0) = p(x=1) = 0.5$. Therefore, the channel capacity is equal to the mutual information $I(X;Y)$, given by:

$$\begin{aligned} C &= I(X;Y) \\ &= H(Y) - H(Y \mid X), \end{aligned} \tag{2}$$

where $H(Y)$ is the entropy of the channel output:

$$H(Y) = -\int p(y) \log_2 (p(y))\, dy \tag{3}$$

and the probability density function $p(y)$ is:

$$p(y) = \sum_{x=0}^{1} p(x)\, p(y \mid x)\,; \tag{4}$$

moreover, $H(Y \mid X)$ is the conditional entropy of the channel output Y given the channel input X , defined as:

$$H(Y \mid X) = -\sum_{x=0}^{1} \int p(y \mid x)\, p(x) \log_2 (p(y \mid x))\, dy \tag{5}$$

Note that (2) can be applied to the capacity evaluation of the write channel, the read channel, the write and read channel in order to balance write and read operations.

The capacity (2), also called ergodic capacity, is obtained by averaging overall possible channel realizations (*i.e.*, an infinite number of 1T-1MTJ cells). This implies that the ergodic capacitycan be achieved only by a theoreticinfinite length ECC.

However, in practice, for a finite code length, the channel capacity varies from one block to another due to the limited number of channel realizations. The outage probability ε_o [29]ismore useful in this case; ε_o is defined as the probability that a capacity C_N measured over a finite sample of size N is lower than a given capacity threshold C_o, where C_N represents the actual data rate and C_o represents a target data rate that is able to be correctlymemorized and delivered. When theactual

block-wise channel capacity C_N is smaller than the required data rate C_o, no ECC exists to guarantee a zero errorevent and a decoding failure isthus declared. In other words, if a design target with a block code of length N bits and a decoding failure rate ε_o are set, the maximum useful information bit number is NC_N and the minimum redundant bit numberintroduced by the ECC should be $N(1-C_N)$. Mathematically, the definition of the outage probability is given by:

$$\Pr(C_N < C_o) \triangleq \varepsilon_o, \tag{6}$$

where the terms C_N, $H(X_N)$ and $H(X_N \mid y_n)$ can be computed as follows:

$$C_N = \frac{1}{N}\sum_{n=1}^{N}\left(H(X_n) - H(X_n \mid y_n)\right), \tag{7}$$

$$H(X_n) = -\sum_{x_n=0}^{1} p(x_n)\log_2\left(p(x_n)\right), \tag{8}$$

$$H(X_n \mid y_n) = -\sum_{x_n=0}^{1} p(x_n \mid y_n)\log_2\left(p(x_n \mid y_n)\right), \tag{9}$$

$$p(x_n \mid y_n) = \frac{p(x_n)\,p(y_n \mid x_n)}{\sum_{x=0}^{1} p(x)\,p(y_n \mid x)}. \tag{10}$$

It is noted that y_n is just onerealizationof Y anda finite block of N realizations cannotcover the whole distribution of Y.

III. STT-MRAM Cell Operation Channel

In this section, a complete STT-MRAM cell operation channel model with both write and read operations is proposed. This model considerstransistor and MTJ process variations, random thermal fluctuations, writing failures, reading flipping errors and resistance variations.

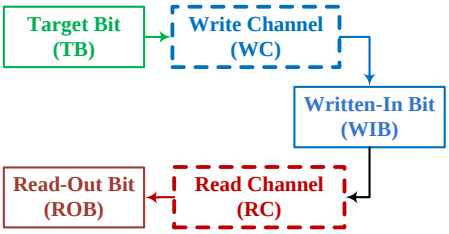


Fig.2. Block diagram of STT-MRAM operation channel model.

The proposed complete cell channel model is shown in Fig.2 and includestwo operationsand three states. The two operations - write channel and read channel are further elaborated inFig.3 and Fig.6, respectively.The three states - target bit (TB), written-in bit (WIB) and read-out bit (ROB) represent the three different livingstates where a bit message resides respectively before writing, after writing (or before reading), and after reading.

A. WriteOperation Channel

The write operation channel model is divided into 5 consecutivesteps:

1) Generate the mean write current value $\bar{I}_w^{PV}$ for the target bit $w = \{0,1\}$;
2) Add a random variation to the mean write current $\bar{I}_w^{PV}$ to generatetheaffectedwritecurrent I_w^{PV} processvariation;
3) Map theprocess variation affected switching current I_w^{PV} to a flipping time T_w^{PV};
4) Generate thefinal switching time T_w^{FST} by further introducing a random thermal-induced deviation ΔT_w^{TF} to the previous flipping time T_w^{PV}:
$$T_w^{FST} = T_w^{PV} + \Delta T_w^{TF}; \tag{11}$$
5) Finally, a writing operation success/failure decision is made by comparing the given write pulse duration (WPD) T_w^{WPD} with the required final switchingtime T_w^{FST}. If $T_w^{WPD} \geq T_w^{FST}$, the written-in bit z is successfully updated asthe target bit w; otherwise, the write operation fails and the WIB z keeps the previous state z^- before this write operation, *i.e.*,
$$z = \begin{cases} w, & \text{if } T_w^{WPD} \geq T_w^{FST} \\ z^-, & \text{else} \end{cases}. \tag{12}$$
Moreover, the soft WIB state z, *i.e.*, the MTJ resistance value R_z [22],[25], is such that:
$$R_z \propto \exp(t_{ox}) / A_{MTJ}, \tag{13}$$
where t_{ox} and A_{MTJ} are the MTJ's tunneling oxide thickness and shape area.

The previous steps of the write operation channel model aredisplayed in Fig.3 and will be further detailed in the rest of this subsection.

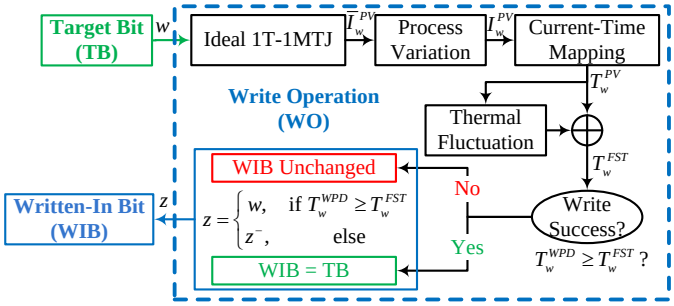


Fig.3. Block diagram of thewrite operation channel.

Thewriting switching current I_w^{PV} impacted by the transistor and MTJ process variations can be modeled as a dual-exponential distribution[5]:

$$p_{PV,w}\left(I_w^{PV}\right) = \sigma_w^{PV} \exp\left(-\frac{\left|I_w^{PV} - \bar{I}_w^{PV}\right|}{\sigma_w^{PV}}\right), \tag{14}$$

where $w = 0$ (*resp.* 1)isthe write switching current directionin the P(*resp.* AP)direction; $\bar{I}_w^{PV}$ and σ_w^{PV} are respectively the mean nominal switching current value and the standard deviation of the corresponding switching currentlisted in TABLE.I.

TABLE.I 1T-1MTJ Write Current Distribution Under Transistor and MTJ Process Variations [25]

Transistor Width (nm)	$\bar{I}_1^{PV}$ (μA)	σ_1^{PV} (μA)	$\bar{I}_0^{PV}$ (μA)	σ_0^{PV} (μA)
180	148.28	14.35	186.00	14.02
270	194.75	18.11	263.03	15.64
360	230.18	20.68	323.27	15.34
450	258.18	22.76	362.77	17.15

540	280.79	24.51	387.48	19.82
630	299.91	26.15	404.43	21.96
720	315.41	27.31	416.69	23.49

The mapping of step 3) froma mean of the MTJ switching current I_w^{PV} toa switching frequency f_w^{PV} (reciprocal of the switching time T_w^{PV})for both transitions $0 \to 1$ and $1 \to 0$ isgiven inFig.4[25].

The ratio σ_w^{TF}/T_w^{PV} between the standard deviation (STD) σ_w^{TF} and the mean of the MTJ switching time T_w^{PV} versus switching frequency f_w^{PV} is shown in Fig.5 for both transitions $0 \to 1$ and $1 \to 0$ [25].

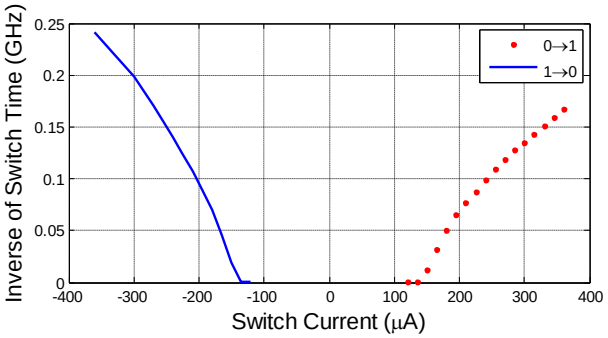


Fig.4. Switching current to switching frequency mapping.

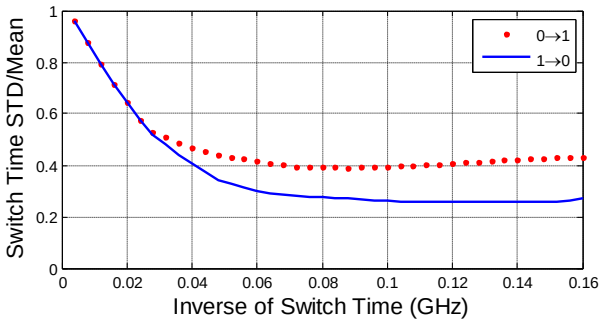


Fig.5. Inverse of switching time to switching time STD/Mean mapping.

As recalled in Section II.D, there are different kinds of thermal fluctuations according to the current switching time at step 4. For a long mean switching time $T_w^{PV} \geq 10$ ns , thethermal-induced MTJ switching time T_w^{FST} follows approximately theexponential distribution[30], for which the STD and the mean are theoretically always equal. However, for $T_w^{PV} \geq 10$ ns , it can be observed from Fig.5 that $\sigma_w^{TF}/T_w^{PV} < 1$ (see below 0.1 GHz). In order to solve this theoretical problem, the random thermal-induced deviation ΔT_w^{TF} is calibrated as:

$$\Delta T_w^{TF} = \sigma_w^{TF}(\delta_E - 1), \tag{15}$$

wherethe probability density function (PDF) of δ_E is given by:

$$p_{\text{Exponential}}(\delta_E) = \exp(-\delta_E). \tag{16}$$

With this calibration, both the mean and STD of T_w^{FST} satisfy with Fig.4 and Fig.5.

For a very short switching time $T_w^{PV} \leq 3$ ns , the thermal-induced switching time variation T_w^{FST} followsthe Gaussian distribution[30]:

$$\Delta T_w^{TF} = \sigma_w^{TF}\delta_G, \tag{17}$$

where :

$$p_{\text{Gaussian}}(\delta_G) = \frac{1}{\sqrt{2\pi}}\exp\left(-\frac{(\delta_G)^2}{2}\right). \tag{18}$$

For an intermediate switch time $3 \text{ ns} < T_w^{PV} < 10$ ns , the thermal-induced switching time T_w^{FSW} is a mixture of the two previous distributions[30]:

$$\Delta T_w^{TF} = \frac{\sigma_w^{TF}}{\sqrt{7}}\left(\sqrt{10 - T_w^{PV}}\,\delta_G + \sqrt{T_w^{PV} - 3}\,(\delta_E - T_w^{PV})\right). \tag{19}$$

Therefore, the final switching time T_w^{FSW} follows the distribution characterized by the process variation induced by both the switching time T_w^{PV} and the STD.

The write operation failure rate of the STT-MRAM cell at step 5 can be defined as the probability that the write access to the STT-MRAM cell cannot becompleted within a givenwrite pulse duration (WPD) T_w^{WPD} , *i.e.*, the probability that the given WPD T_w^{WPD} is shorter than the final switching time T_w^{FST} .

Both, the MTJ's tunneling oxide thickness t_{ox} and the shape area A_{MTJ} follow Gaussian distributions[25]:

$$p(t_{ox}) = \frac{1}{\sqrt{2\pi}\sigma_{tox}}\exp\left(-\frac{(t_{ox} - u_{tox})^2}{2(\sigma_{tox})^2}\right), \tag{20}$$

$$p(A_{MTJ}) = \frac{1}{\sqrt{2\pi}\sigma_{AMTJ}}\exp\left(-\frac{(A_{MTJ} - u_{AMTJ})^2}{2(\sigma_{AMTJ})^2}\right), \tag{21}$$

where u_{tox} and σ_{tox} are the mean and STD of the tunneling oxide thickness, while u_{AMTJ} and σ_{AMTJ} are the mean and STD of the shape area.

Taking into account(13), the equivalent resistance of the MTJ with technical variations can be approximatedas:

$$\begin{aligned} R_Z^{PV} &= \frac{\exp(t_{ox})/A_{MTJ}}{\exp(u_{tox})/u_{AMTJ}}R_Z \\ &= \left(\frac{u_{AMTJ}}{A_{MTJ}}\right)\exp(t_{ox} - u_{tox})R_Z. \end{aligned} \tag{22}$$

The technical parameters σ_{tox} and σ_{AMTJ} in (20)-(22)are obtained from[22]. The other parameters u_{tox} and u_{AMTJ} are taken from [25]in which an elliptical shaped 45nm × 90nm in-plane MTJ under a Predictive Technology Model (PTM) 45nm model [31]was proposed. These parameters were calibrated with the measurement data from a leading magnetic recording company and are recalled in TABLE.II.

TABLE.IIMTJ and Transistor Technical Parameters

Device	Parameter	Mean	STD
Transi-stor	Channel Length L_T (nm)	45	
	Channel Width W_T (nm)	180 to 720	
	Threshold voltage V_{th} (V)	0.466	
MTJ	Shape Area A_{MTJ} (nm^2)	$45 \times 90\pi/4$	5% of mean
	MgO Thickness t_{ox} (nm)	1.5	2% of mean
	Low Resistance R_p (Ohm)	1000	
	High Resistance R_{AP} (Ohm)	2000	
	Reference Resistance R_{REF} (Ohm)	1500	

The STD $\sigma_{V_{th}}$ of the threshold voltage V_{th} (seeTABLE.II)is approximately computed as[25]:

$$\sigma_{V_{th}} = 0.3\frac{45^2}{W_T L_T} = \frac{607.5}{W_T L_T}, \tag{23}$$

where W_T and L_T are respectively the transistor width and length in nm.

Let us turn now to the evaluation of the write channel capacity. Given the equiprobableassumption made over the input TB w, the capacity of the write channel can be written as:

$$\begin{aligned} I(w;R_z) &= H(R_z) - H(R_z \mid w) \\ &= -\int p(R_z)\log_2\big(p(R_z)\big)dR_z \\ &\quad + \sum_{w=0}^{1}\int p(R_z \mid w)\,p(w)\log_2\big(p(R_z \mid w)\big)dR_z, \end{aligned} \tag{24}$$

wherethe key terms $p(R_z)$ and $p(R_z \mid w)$ are given by:

$$p(R_z) = \sum_{w=0}^{1} p(w)\,p(R_z \mid w), \tag{25}$$

$$p(R_z \mid w) = \sum_{z^- =0}^{1} p(z^-)\,p(R_z \mid w, z^-); \tag{26}$$

$p(z)$, according to the previous state distribution $p(z^-)$ can be computed as:

$$p(z) = \sum_{w=0}^{1} p(w)\sum_{z^-=0}^{1} p(z^-)\,p(z \mid w, z^-); \tag{27}$$

From Section II.A and step 5of Section III.A, the transition probability $p(z \mid w, z^-)$ can be expressed in terms of write success and fail probabilities, *i.e.* :

$$\begin{cases} p(z=0 \mid w=0, z^-=0) = p(z=1 \mid w=1, z^-=1) = 1 \\ p(z=1 \mid w=0, z^-=0) = p(z=0 \mid w=1, z^-=1) = 0 \\ p(z=0 \mid w=0, z^-=1) = p(\text{P write success}) \\ p(z=1 \mid w=1, z^-=0) = p(\text{AP write success}) \\ p(z=1 \mid w=0, z^-=1) = p(\text{P write fail}) \\ p(z=0 \mid w=1, z^-=0) = p(\text{AP write fail}) \end{cases} \tag{28}$$

Substituting (28)into (27), $p(z=0)$ and $p(z=1)$ can be further written as:

$$\begin{aligned} p(z=0) &= p(w=0)\,p(z^-=0) \\ &\quad + p(w=0)\,p(z^-=1)\,p(\text{P write success}) \\ &\quad + p(w=1)\,p(z^-=0)\,p(\text{AP write fail}), \end{aligned} \tag{29}$$

$$\begin{aligned} p(z=1) &= p(w=1)\,p(z^-=1) \\ &\quad + p(w=0)\,p(z^-=1)\,p(\text{P write fail}) \\ &\quad + p(w=1)\,p(z^-=0)\,p(\text{AP write success}) \end{aligned}. \tag{30}$$

Since the previous state z^- has asymptotically the same distribution as z, (29) can be reformulated as:

$$\begin{aligned} & p(w=0)\,p(z^-=1)\,p(\text{P write success}) \\ &= p(z=0) - p(w=0)\,p(z^-=0) - \\ &\quad p(w=1)\,p(z^-=0)\,p(\text{AP write fail}) \\ &= p(w=1)\,p(z^-=0) - p(w=1)\,p(z^-=0)\,p(\text{AP write fail}) \\ &= p(w=1)\,p(z^-=0)\big[1 - p(\text{AP write fail})\big] \\ &= p(w=1)\,p(z^-=0)\,p(\text{AP write success}). \end{aligned} \tag{31}$$

Since $p(w=0) = p(w=1) = 0.5$, the ratio of $p(z^-=1)$ and $p(z^-=0)$ can readily be obtained as:

$$\frac{p(z^-=1)}{p(z^-=0)} = \frac{p(\text{AP write success})}{p(\text{P write success})}. \tag{32}$$

(32)simplymeans thatthe WIB z distribution depends only on the write operation success rate and that the state distribution ratio is exactly equal to the ratio of the anti-parallel and parallelwrite success probabilities.In other words, with no a priori information onthe TB, the distribution of the WIB converges to the distribution given by(32). Therefore, theequiprobable assumption does not hold anymore for theWIB z.

Thuscomputing the capacity(24)involvesto obtain $p(\text{write success})$ and thePDF $p(R_z \mid w, z^-)$, which can be achieved by Monte-Carlo simulations of the proposed write channel model.

B. Read Channel Model

Due to the unbalanced driving ability of the transistor,the failure probability of anti-parallel ($0 \to 1$) writing is much higher than that of parallel ($1 \to 0$) writing. However, the higher write operation failure probability gives a favor of lower flipping probability to the read operation. Therefore, differently from the write channel, the AP direction is preferable to the P directionfor read operation.

The read operation channel model can also be divided into 5 consecutive steps:

1) Generate the mean read current value $\bar{I}_{AP}^{PV}$;
2) Add a random variation to the mean read current $\bar{I}_{AP}^{PV}$ so as to generate the process variation affected read current I_{AP}^{PV};
3) Map the process variation affected read current I_{AP}^{PV} to a flipping time T_{AP}^{PV};
4) Generate the overallswitching time T_{AP}^{FST} by further introducing a random thermal-induced deviation ΔT_{AP}^{TF} to the previous switching time T_{AP}^{PV}:
$$T_{AP}^{FST} = T_{AP}^{PV} + \Delta T_{AP}^{TF}; \tag{33}$$
5) Finally, a readflipping error is decided by comparing the given read pulse duration (RPD) T_{AP}^{RPD} with the required flipping time T_{AP}^{FST}. If $T_{AP}^{RPD} \geq T_{AP}^{FST}$, the written-in bit z is flipped to 1 and the read-out bit state $r=1$; otherwise, no flipping error occurs and the ROB r is updated as the WIB z:
$$r = \begin{cases} 1, & \text{if } T_{AP}^{RPD} \geq T_{AP}^{FST} \\ z, & \text{else} \end{cases}. \tag{34}$$
Moreover, the decidedbit (DB) $\hat{r}$ is obtained by comparing the actual sensing current $I(\hat{r})$ with an ideal sense current I_{REF}:

$$\hat{r} = \begin{cases} 0 & \text{if } I(\hat{r}) > I_{REF} \\ 1 & \text{else} \end{cases}, \tag{35}$$

where $I(\hat{r})$ and I_{REF} are:

$$I_{\hat{r}} = \frac{V_{sense} - V_{th}}{R_r}, \tag{36}$$

$$I_{REF} = \frac{V_{sense} - \bar{V}_{th}}{R_{REF}}; \tag{37}$$

V_{sense} = 0.58 V is the sense voltage for reading, $\bar{V}_{th}$ = 0.466 V (see TABLE.II) is the mean threshold voltage, V_{th} is the actual threshold voltage depending of process variation, R_r is the actual resistance value corresponding to ROB state r and R_{REF} = 1500 Ohm (see TABLE.II).Due to the V_{th} variation, the nominal resistance value for the bit decision is:

$$R_{\hat{r}} = \frac{V_{sense} - 0.466}{V_{sense} - V_{th}} R_r. \tag{38}$$

It should be mentioned that there are many kinds of sense amplifiers [32]-[35] and none of them has really become a "standard" cell. Because of this, the sense amplifier in the read channel is assumed to be an ideal current sense amplifier with a reference current value simply being the mean of the current values of the low and high resistance states; in other words, this sense amplifier does neither take into account the process variations, nor the thermal fluctuations.

Apart from thecurrent direction and the current strength, the read operation is analogous to the write operation (see Fig.6). In this way, most of the technical parameters and all the distribution models already used for the write channel can be used again for the read channel.and the reference resistance is assumed to be ideal with neither process variations nor thermal fluctuations.

For the AP read operation over the 1T-1M cell, there are three types of reading errors:

1) The cell stores a 0 but is read out as a 1;
2) The cell stores a 1 but is read out as a 0;
3) The cell stores a 0 but is flipped to 1.

The capacity of the read channel can be written as:

$$\begin{aligned} I(z;R_{\hat{r}}) &= H(R_{\hat{r}}) - H(R_{\hat{r}} \mid z) \\ &= -\int p(R_{\hat{r}}) \log_2 \left(p(R_{\hat{r}}) \right) dR_{\hat{r}} \\ &\quad + \sum_{z=0}^{1} \int p(R_{\hat{r}} \mid z)\, p(z) \log_2 \left(p(R_{\hat{r}} \mid z) \right) dR_{\hat{r}}, \end{aligned} \tag{39}$$

where the resistance distribution $p(R_{\hat{r}})$ of the nominal resistance value in (38) can be written as:

$$p(R_{\hat{r}}) = \sum_{z=0}^{1} p(z)\, p(R_{\hat{r}} \mid z), \tag{40}$$

and $p(z)$ is obtained from (32) by computing $p(\text{write success})$. Therefore, in order to evaluate the PDF $p(R_{\hat{r}} \mid z)$ and to compute (39), one has to simulate both the write and read operations.

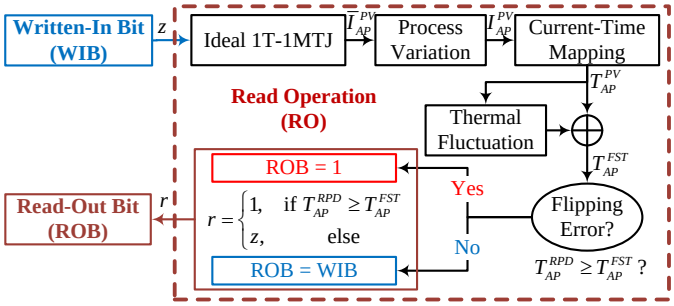


Fig.6. Block diagram of the read operation channel.

C. *Write and Read Channel Capacity*

The combinedwrite and read channel capacity can be written as:

$$\begin{aligned} I(w;R_{\hat{r}}) &= H(R_{\hat{r}}) - H(R_{\hat{r}} \mid w) \\ &= -\int p(R_{\hat{r}}) \log_2 \left(p(R_{\hat{r}}) \right) dR_{\hat{r}} \\ &\quad + \sum_{w=0}^{1} \int p(R_{\hat{r}} \mid w)\, p(w) \log_2 \left(p(R_{\hat{r}} \mid w) \right) dR_{\hat{r}}, \end{aligned} \tag{41}$$

where $p(R_{\hat{r}})$ and $p(R_{\hat{r}} \mid w)$ are:

$$p(R_{\hat{r}}) = \sum_{w=0}^{1} p(w)\, p(R_{\hat{r}} \mid w), \tag{42}$$

$$\begin{aligned} p(R_{\hat{r}} \mid w) &= \sum_{z^- = 0}^{1} p(z^-)\, p(R_{\hat{r}} \mid w, z^-) \\ &= \sum_{z^- = 0}^{1} p(z^-) \sum_{z=0}^{1} p(R_{\hat{r}}, z \mid w, z^-) \\ &= \sum_{z^- = 0}^{1} p(z^-) \sum_{z=0}^{1} p(z \mid w, z^-)\, p(R_{\hat{r}} \mid z). \end{aligned} \tag{43}$$

Similarly to SectionIII.A andSection III. B, $p(z \mid w, z^-)$ and $p(R_{\hat{r}} \mid z)$ are computed by simulating the write channel and the read channel respectively.

IV. Simulations and Results

In this section, the proposed channel model is first validated by comparing simulation results to the experimental results published in[25]. After validation,the reliability of the 1T-1MTJ operation channel is evaluated in terms of probability density function, operation failure rate, bit error rate and channel capacity.All the process variations and thermal fluctuations mentioned in SectionIII are included in these simulations.

A. *Model Validation*

In this subsection, all the curves with "REF" represent the original experimental results published in [25], whereas the curves with "SIMU" represent the recreated results via the proposed channel model.

Fig.7 and Fig.8 (see Fig. 7 (a) in [25]) show our simulation results of the write error rates (WERs) with awriting pulse duration (WPD) equal to 10 ns and 20 ns. It can be observed that the recreated results obtained by the proposed STT-MRAM operation model follow closely the already published corresponding results.

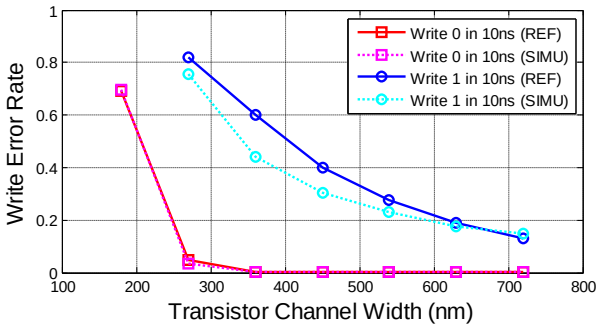


Fig.7. Write error rate for a 10 ns writing pulse width.

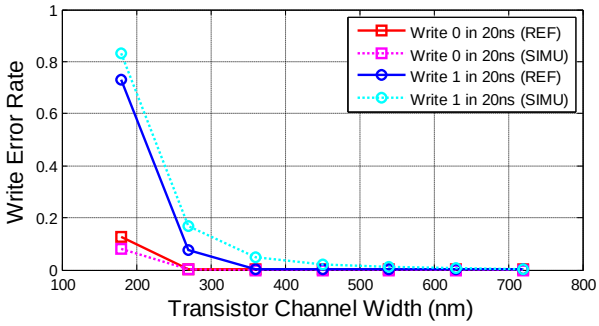


Fig.8. Write error rate for a 20 ns writing pulse width.

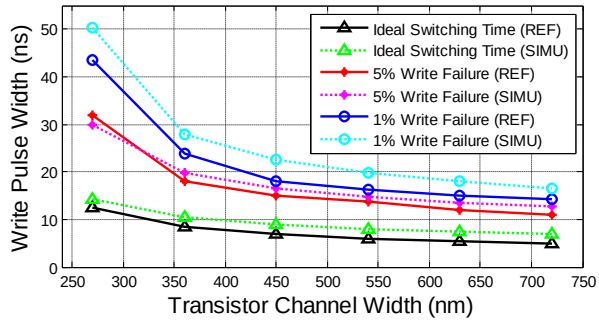


Fig.9. Comparison of writing "1" error rates between our model and Fig. 7 (b) of [25].

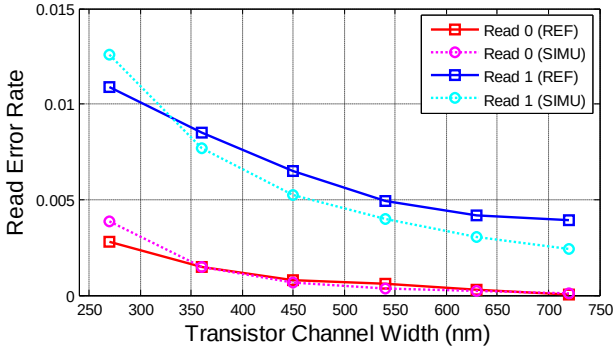


Fig.10. Reading failure rate for different transistor widths.

Fig.9 (see Fig. 7 (b) in [25]) displays the required WPDs for different NMOS transistor widths. In this figure, the ideal switching time represents the results based on the mean device parameters without considering any process variations and thermal fluctuations. It can be observed that the recreated 1% and 5% WER switching time also follow closely the corresponding already published curves. The limited differences between the 1% (resp. 5%) WER switching time curves are mainly due to the small difference between the recreated ideal switching time and the corresponding published ideal switching time.

Fig.10 (see Fig. 3 in [25]) gives the read error rates (RERs) for different transistor widths. As [25] uses a practical sense amplifier, the recreated results with an ideal sense amplifier lead to slightly better results in most cases.

B. Write Operation Channel

In this subsection, the write channel is evaluated according tothe model illustrated by Fig.3in SectionIII.A.The TBs are assumed to be equiprobable. We recall that the switching current parameters for the write operations are listed in TABLE.I, the conversion from switching current to switching time is displayed inFig.4 and the thermal-induced switching timeis generated by using (15)-(19).

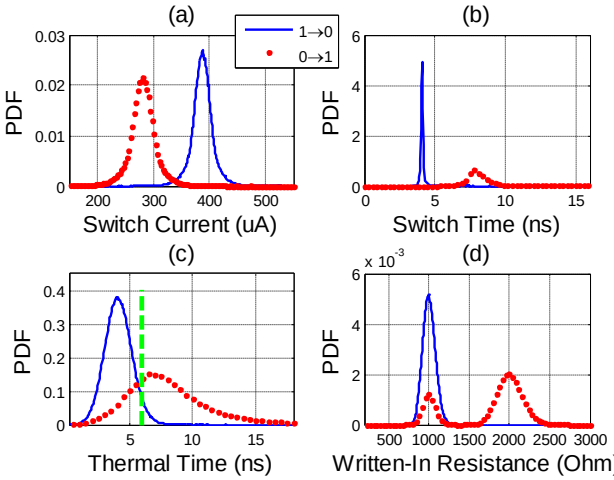


Fig.11. STT-MRAM write operational channel (transistor size = 540 nm, WPD = 10 ns).

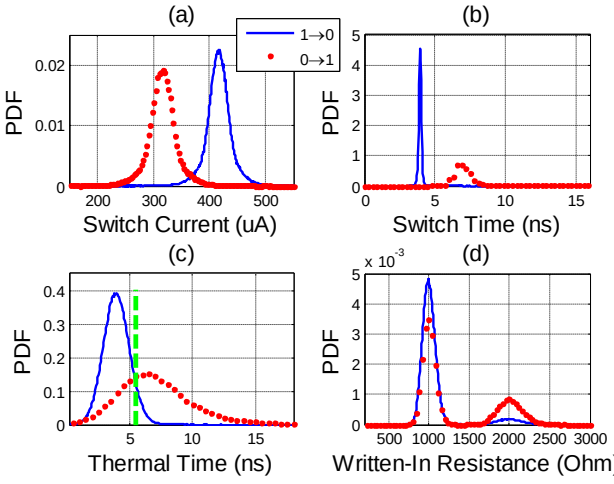


Fig.12. STT-MRAM write operational channel (transistor size = 720nm, WPD = 5.5 ns).

Fig.11 displays the whole process of the write operation channel with a 540 nm transistor size; Fig.11 (a) presents the distributions of write currents I_w^{PV} under the impact of process variations, (see (14)). Fig.11 (b) illustrates the distribution of switch time T_w^{PV} mapped from switching current I_w^{PV} (see Fig.4 and step 3 in Section III.A), where the larger deviation for the AP direction ($0 \to 1$) can be easily observed. Fig.11 (c)

highlights even larger expansions of the final switching time T_w^{FST} of (11) affected by thermal fluctuations; a large difference can be noticed between Fig.11 (b) and Fig.11 (c) with and without thermal fluctuations, respectively. Moreover, in Fig.11 (c), a green dash line indicates a given WPD = 10ns serving as the boundary between a write operation success (left-hand side) region with required cell flipping time inferior to this given WPD and a write operation failure (right-hand side) region. Fig.11 (d) gives the written-in resistance distributions generated from (22) for a WPD = 10ns. The write failure for the $0 \to 1$ transition, *i.e.*, the small red peak around the low resistance state (around 1000 Ohm) can be clearly observed, and this peak stems from the large tail existing at the right-hand side of the green 10 ns dash line in Fig.11 (c) for too long switching durations. Therefore, for WPD=10 ns, the high write operation failure rate can be predicted.

Fig.12 display the whole process of the write operation channel with even more critical parameters (720 nm transistor size and WPD = 5.5 ns). Differently from Fig.11, due to the insufficient WPD, the reliability of writing "0" is also affected and a write operation failurefor both transitions can be observed in the lower subfigures (c) and (d).

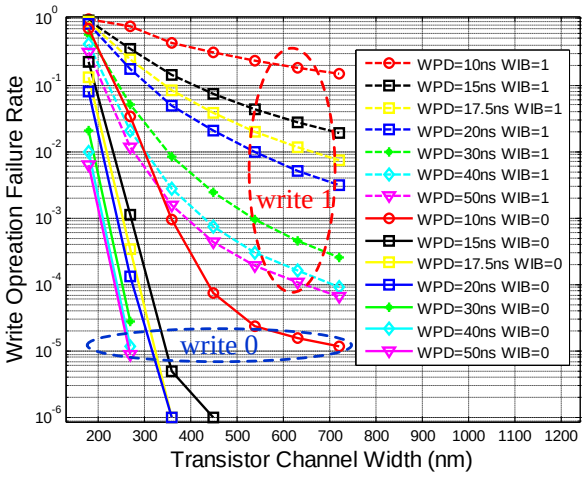


Fig.13. STT-MRAM writeoperation failure rates with different transistor widths and different WPDs.

Fig.13 shows the write operation failure rates for different transistor widths and different WPDs. It is easy to notice that the write failure rate for the $0 \to 1$ transition is several orders of magnitude higher than the failure rate for the $1 \to 0$ transition. The larger the transistor, the larger the drive current strength so that the required switching time is shorter and thus the write operation failure rate tends to be lower. Similarly to increasing the transistor width, the same improvement for the write operation failure can be easily observed by increasing the WPD. Since the operation failure rate involves only $0 \to 1$ and $1 \to 0$ transitions, the performance is not influenced by the original cell state before writing operation.Differently from Fig.13, Fig.14 measures the written-in bit error rate and the corresponding simulations logically involves the original cell state before the writing operation. Therefore, the fact that the TB can be successfully written into the STT-MRAM cell depends also of the original cell state. To simplify the simulations, we assume that there are originally as much "0"s as "1"s.

Fig.15 displays the write channel capacity (see (24)) for various transistor widths and various WPD. Similarly to Fig.14, since Fig.15 is related with the bit reliability, the capacity simulations also involve the original cell state. From Fig.15for a WPD = 10 ns, a target channel code rate equal to 0.85 cannot meet the capacity requirement due to the too high write failure rate of the AP direction; moreover, solutions with transistor widths inferior to 200 nm can neither satisfy the system requirements. As the target code rate slightly increases to 0.9, solutions can only be selected among the designs with transistor width being superior to 360 nm.

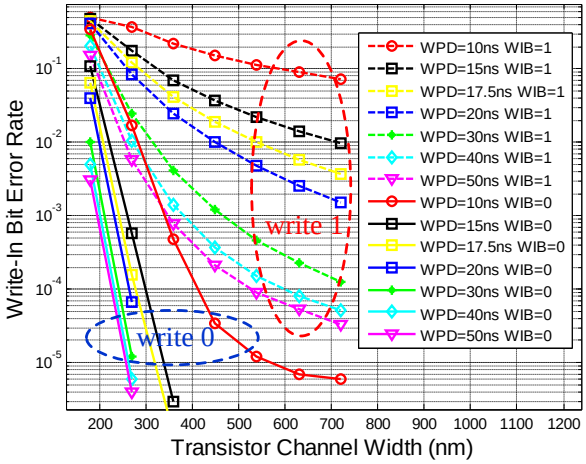


Fig.14. STT-MRAM write-in bit error rates with different transistor widths and different WPDs.

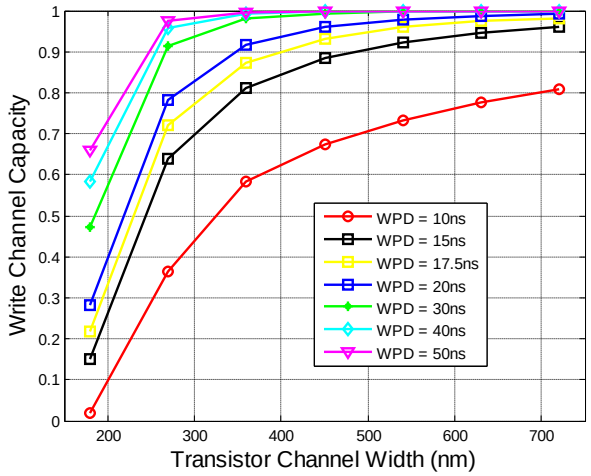


Fig.15. STT-MRAM write channel capacities with different transistor widths and different WPDs

Fig.16 illustrates the result given by(32). It shows that the distribution of the WIB is not equiprobable in general and that writing '0' is always easier than writing '1'. Moreover, solutions with WPD = 10 ns and solutions with a transistor width smaller than 270 nm cause large differences between $p(z=0)$ and $p(z=1)$. By comparing the results ofFig.13 with Fig.16, it can be further observed that the WIB approaches to the equiprobability as the write operation failure rate decreases. It

can then be concluded by comparing with Fig.15 that the hypothesis that WIBs areequiprobableholds for reliable write channels with write channel capacity being superior to 0.9 bit/cell.

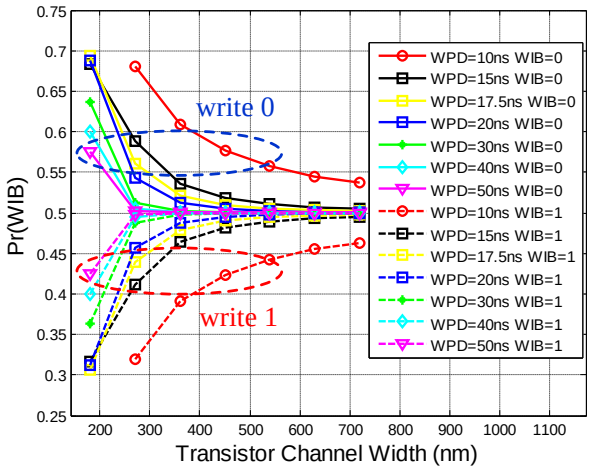


Fig.16. STT-MRAM written-in bits (WIBs) distributions with different transistor widths and different WPDs.

C. *Read Operation Channel*

In this subsection, the read channel is evaluated according to the model illustrated by Fig.6in SectionIII.B. The WIBsare assumed to be uniformly distributed to eliminate any write channel influence. Theparameters for the read operation are listed inTABLE.IIand are applied to(20)-(23).

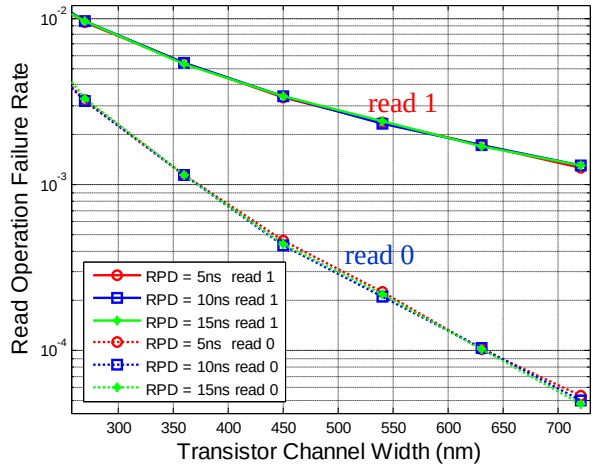


Fig.17. STT-MRAM read operation failure rates with different transistor widths and different RPDs.

Fig.17 and Fig.18 present the read operational failure rate and the read channel capacity for different transistor widths and for different read pulse durations (RPDs). Because of the lowvalues taken by read currents, the flipping error *i.e.*, the third type of read error nearly never happens even with RPD=15ns and operational failures are mainly due to process variations of the MTJ resistanceand to the threshold voltage variations. As the threshold voltage STD decreaseswhenthe transistor width increases, the operation failure rate for a large transistor width is better than the rate for a small transistor width. Since the MTJ resistance distribution is independent of thetransistor width, the read failure rate is no affected by the short RPDs. Moreover, because of the larger resistance variations of state '1', thefailure rate to read a '1' is higher than that to read a '0'.Theread channel capacity ofFig.18 is much higher than the write channel capacity of Fig.15; this is due to the small current values used for read operations, and consequently the flipping error rate is near zero.

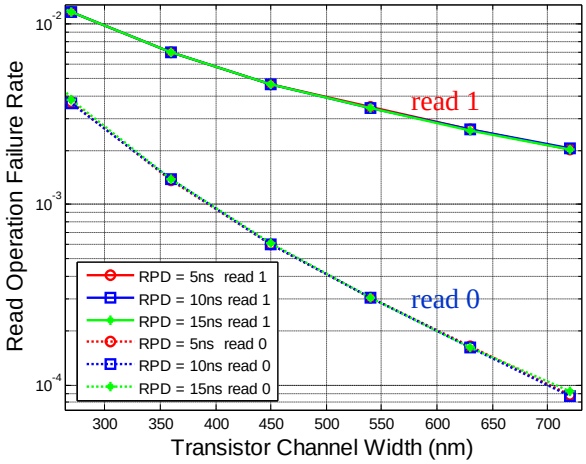


Fig.18. STT-MRAM read channel capacitywith different transistor widths and different RPDs.

D. *Combined Write and Read Channel*

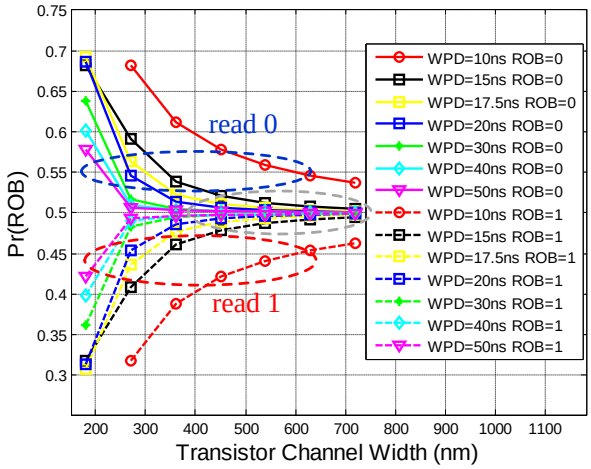


Fig.19. STT-MRAM read-out bits (ROBs) distributions with different transistor widths and different WPDs (RPD = 5ns).

Fig.19 gives the read-out bit (ROB) distributions after that the cell write and read operations are both completed. It can be seen that the ROB distributions are similar to the WIB distributions in Fig.16. However, as the channel width increases, the ROB distribution difference is slightly larger than the WIB distribution difference (compare the curves within the grey dashed circle in Fig.19 with the corresponding curves in Fig.16). This fact comes from the difference of MTJ resistance deviations for state '0' and state '1' due to process variations of the MTJ's shape surface and tunnel oxide thickness. However, the equiprobable assumption still approximately holds for the cases of a transistor size larger than 270 nm and a WPD longer than 10 ns.

Fig.20 and Fig.21respectively present the operation failure rate and the BER of the combined write and read operation channel. Due to the process variations of the MTJ resistance,

there exists error floorsfor both parallel and anti-parallel directions. Note that the intrinsic resistance variations cannot be removed by changing extrinsic parameters such as the transistor size orthe WPD; thereforeusing an ECC becomesabsolutely compulsorywhen the BER does not meet the target requirement.

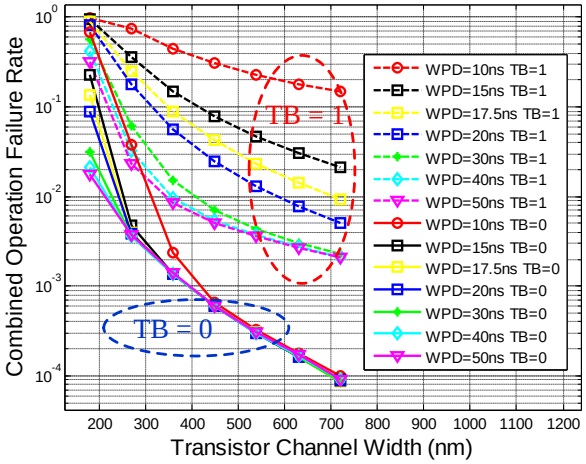


Fig.20. STT-MRAM written-in bits (WIBs) distributions with different transistor widths and different WPDs (RPD = 5ns).

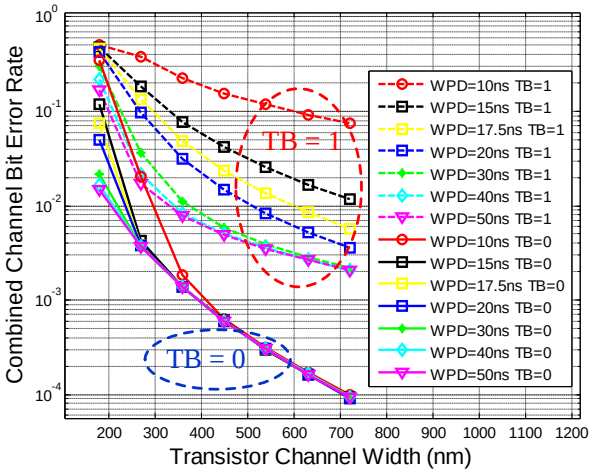


Fig.21. STT-MRAM written-in bits (WIBs) distributions with different transistor widths and different WPDs (RPD = 5ns).

Fig.22 gives the combined channel capacities, *i.e.*, the maximum bit number that can be reliably written in and read out in one cell. This metric gives the upper bound for the channel coding rate with infinite code length. Note that as the transistor drive capacity increases, the reduced operation failure rate and the increased channel capacity indicate that an ECC can have less redundancy (i.e., higher efficiency) to protect messages. If the target code rate is 0.7, the transistor width needs to be larger than 270 nm and the WPD has to be kept longer than 17.5 ns. If the target code rate is 0.9, the minimum transistor width is 350 nm for a minimum WPD equal to 20 ns.

Finally, Fig.23 gives the outage probability for an outage capacity C_o = 0.9 bit/cell with different transistor widths, different block lengths (BLK) and different WPDs. The ergodic curves of different WPDs and different transistor sizes serve as limits. The lowest outage probabilities simulated for different WPDs and all transistor sizes reach at least the level of 10^{-7}. In other words, if a point is not plotted, it simply means that the performance is below 10^{-7}.

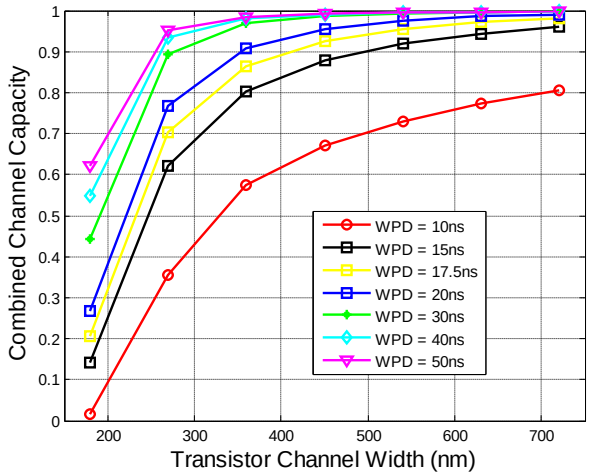


Fig.22. STT-MRAM written-in bits (WIBs) distributions with different transistor widths and different WPDs (RPD = 5ns).

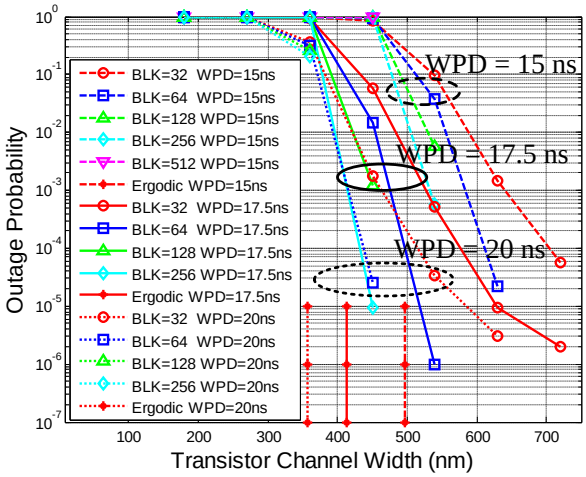


Fig.23. STT-MRAM outage probability as outage capacity C_o = 0.9 bit/cell with different transistor widths (including infinite block length) and different WPDs (RPD = 5ns).

It can be observed that the outage probability can be improved as the block length increases; this is simply due to the fact that an increased block length has more channel realizations and thus leads the block capacity to approach the ergodic capacity limit. Moreover, as the transistor width or the WPD increases, the decreased outage probability should be attributed to both improved operation channel quality and lower write operation failure rate. Note that for large outage probabilities the gain obtained with an increased block length is usually smaller than the gain obtained with improved technical parameters; this is because the former only induces that the block capacity approaches the ergodic capacity while channel conditions are not improved, however, improving technical (*i.e.*, physical) parameters directly increases the channel capacity.

Obviously, there is a price for improved technical parameters. For example, increasing the transistor width does improve the channel capacity and thus allows the use of higher code rate ECCs; however, both the memory area and power consumptionthenincrease.Therefore, for a specific application,

the optimum solution will be selected by balancing the various requirements among latency, throughput, size, andpower constrain.

V. Conclusion

This paper proposed a complete channel model to simulate write and read operations of the 1T-1MTJ STT-MRAM cells. This model considered both process variations and thermal fluctuations. Based on the proposed cell operation channel, reliabilities including operation failure rate, bit error rate (BER), channel ergodic capacity and channel outage probabilitywere evaluated from an information theory perspective. Moreover, it is proved that the distributions of the WIB states are not equiprobable and that their ratio isdetermined by their respective write success probabilities. Finally, simulation results show that practical code rates and code block lengths can guarantee reliable performances only if the difference between state '1' and state '0' operation success rates is small enough.

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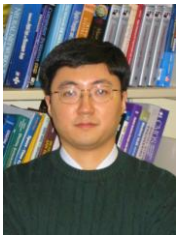
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