Analysis and Design of Cost-Effective, High-Throughput LDPC Decoders

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Abstract—This paper introduces a new approach to costeffective, high-throughput hardware designs for Low Density Parity Check (LDPC) decoders. The proposed approach, called Non-Surjective Finite Alphabet Iterative Decoders (NS-FAIDs), exploits the robustness of message-passing LDPC decoders to inaccuracies in the calculation of exchanged messages, and it is shown to provide a unified framework for several designs previously proposed in the literature. NS-FAIDs are optimized by density evolution for regular and irregular LDPC codes, and are shown to provide different trade-offs between hardware complexity and decoding performance. Two hardware architectures targeting high-throughput applications are also proposed, integrating both Min-Sum (MS) and NS-FAID decoding kernels. ASIC post synthesis implementation results on 65nm CMOS technology show that NS-FAIDs yield significant improvements in the throughput to area ratio, by up to 58.75% with respect to the MS decoder, with even better or only slightly degraded error correction performance.

Index Terms—Error correction, LDPC codes, NS-FAID, low cost, high-throughput.

I. INTRODUCTION

THE increasing demand of massive data rates in wireless communication systems will require significantly higher processing speed of the baseband signal, as compared to conventional solutions. This is especially challenging for Forward Error Correction (FEC) mechanisms, since FEC decoding is one of the most computationally intensive baseband processing tasks, consuming a large amount of hardware resources and energy. The use of very large bandwidths will also result in stringent, application-specific, requirements in terms of both throughput and latency. The conventional approach to increase throughput is to use massively parallel architectures. In this context, Low-Density Parity-Check (LDPC) codes are recognized as the foremost solution, due to the intrinsic capacity of their decoders to accommodate various degrees of parallelism. They have found extensive applications in modern communication systems, due to their excellent decoding performance, high throughput capabilities [1]–[4], and power efficiency [5], [6], and have been adopted in several recent communication standards.

This paper targets the design of cost-effective, highthroughput LDPC decoders. One important characteristic of LDPC decoders is that the memory and interconnect blocks dominate the overall area/delay/power performance of the hardware design [7]. To address this issue, we build upon the concept of Finite Alphabet Iterative Decoders (FAIDs), introduced in [8]–[10]. While FAIDs have been previously investigated for variable-node regular LDPC codes over the binary symmetric channel, this paper extends their use to any channel model, and to both regular and irregular LDPC codes.

The approach considered in this paper, referred to as *Non-Surjective FAIDs* (NS-FAIDs), is to allow storing the exchanged messages using a lower precision (smaller number of bits) than that used by the processing units. The basic idea is to reduce the size of the exchanged messages, once they have been updated by the processing units. Hence, to some extent, the proposed approach is akin to the use of *imprecise storage*, which is seen as an enabler for cost and throughput optimizations. Moreover, NS-FAIDs are shown to provide a unified framework for several designs previously proposed in the literature, including the normalized and offset Min-Sum (MS) decoders [11], [12], the partially offset MS decoder [13], the MS-based decoders proposed in [14], [15], or the recently introduced dual-quantization domain MS decoder [16].

This paper refines and extends some of the concepts we previously introduced in [17], [18]. In particular, the definition of NS-FAIDs [17] is extended such as to cover a larger class of decoders, which is shown to significantly improve the decoding performance in case that the exchanged messages are quantized on a small number of bits (e.g., 2 bits per exchanged message). We show that NS-FAIDs can be optimized by using the Density Evolution (DE) technique, so as to obtain the best possible decoding performance for given hardware constraints, expressed in terms of memory size reduction. The DE optimization is illustrated for both regular and irregular LDPC codes, for which we propose a number of NS-FAIDs with different trade-offs between hardware complexity and decoding performance.

To assess the benefits of the NS-FAID approach, we further extend the hardware architectures proposed in [18] to cover the case of irregular codes, and provide implementation results targeting an ASIC technology, which is more likely to reflect the benefits of the proposed NS-FAID approach in terms of throughput/area trade-off. The proposed architectures target high-throughput and efficient use of the hardware resources. Both architectures implement layered decoding with fully parallel processing units. The first architecture is pipelined, so as to increase throughput and ensure an efficient use of the

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hardware resources, which in turn imposes specific constraints on the decoding layers¹, in order to ensure proper execution of the layered decoding process. The second architecture does not make use of pipelining, but allows maximum parallelism to be exploited through the use of full decoding layers², thus resulting in significant increase in throughput. Both MS and NS-FAID decoding kernels are integrated into each of the two proposed architectures, and compared in terms of area and throughput. ASIC post synthesis implementation results on 65nm CMOS technology show a throughput to area ratio improvement by up to 58.75%, when the NS-FAID kernel is used, with even better or only slightly degraded error correction performance.

The rest of the paper is organized as follows. NS-FAIDs are introduced in Section II, which also discusses their expected implementation benefits and the DE analysis. The optimization of regular and irregular NS-FAIDs is presented in Section III. The proposed hardware architectures, with both MS and NS-FAID decoding kernels, are discussed in Section IV. Numerical results are provided in Section V, and Section VI concludes the paper.

II. NON-SURJECTIVE FINITE ALPHABET ITERATIVE DECODERS

A. Preliminaries

LDPC codes are defined by sparse bipartite graphs, comprising a set of variable-nodes (VNs), corresponding to coded bits, and a set of check-nodes (CNs), corresponding to paritycheck equations. Finite Alphabet Iterative Decoders (FAIDs) are message-passing LDPC decoders that have been introduced in [8]–[10]. We state below the definition of a subclass of FAID decoders, which is less general than the one proposed in [10]. Let Q be a positive integer. A (2Q + 1)-level FAID is a 4-tuple $(\mathcal{M}, \Gamma, \Phi_v, \Phi_c)$, where:

- $\mathcal{M} = \{-Q, \ldots, -1, 0, +1, \ldots, +Q\}$ is the alphabet of the exchanged messages, and is also referred to as the *decoder alphabet*,
- Γ ⊆ M is the input alphabet of the decoder, *i.e.*, the set of all possible values of the quantized soft information supplied to the decoder,
- Φ_v and Φ_c denote the update rules for VNs and CNs, respectively.

We shall use $\mathfrak{m} \in \mathcal{M}$ and $\gamma \in \Gamma$ to denote elements of \mathcal{M} and Γ , respectively. The CN-update function Φ_c is the same for any FAID decoder, and is equal to the update function used by the MS decoder. Precisely, for a CN of degree d_c , the update function $\Phi_c : \mathcal{M}^{d_c-1} \to \mathcal{M}$ is given by:

$$\Phi_c(\mathfrak{m}_1,\ldots,\mathfrak{m}_{d_c-1}) = \left(\prod_{i=1}^{d_c-1} \operatorname{sgn}(\mathfrak{m}_i)\right) \min_{i=1,\ldots,d_c-1} |\mathfrak{m}_i| \quad (1)$$

¹A decoding layer may consist of one or several rows of the base matrix of the QC-LDPC code, assuming that they do not overlap.

²A decoding layer is said to be full if each column of the base matrix has one non-negative entry in one of the rows composing the layer.

The VN-update function $\Phi_v : \Gamma \times \mathcal{M}^{d_v - 1} \to \mathcal{M}$, for a VN of degree d_v , is defined as:

$$\Phi_{v}\left(\gamma,\mathfrak{m}_{1},\ldots,\mathfrak{m}_{d_{v}-1}\right)=F\left(\gamma+\sum_{j=1}^{d_{v}-1}\mathfrak{m}_{j}\right) \qquad (2)$$

where the function $F : \mathbb{Z} \to \mathcal{M}$ is defined based on a set of threshold values $\mathcal{T} = \{T_0, T_1, \dots, T_{Q+1}\} \subset \mathbb{R}_+$, with $T_0 = 0$, $T_{Q+1} = +\infty$, and $T_i < T_j$ for any i < j:

$$F(x) = \operatorname{sgn}(x)\mathfrak{m}$$
, where \mathfrak{m} is s.t. $T_{\mathfrak{m}} \le |x| < T_{\mathfrak{m}+1}$ (3)

In Eq. (2), the variable γ represents the *channel contribution*, *i.e.*, the quantized soft information that has been supplied to the decoder for the corresponding variable-node. The quantization method and its impact on FAIDs' decoding performance will be discussed in Section II-E. It is also worth noting that in [10], FAIDs are introduced with a more general VN-update function Φ_v , but the simpler definition (2) that we use has many hardware implementation benefits, which will be described in later sections. Moreover, it can be easily seen that any non-decreasing odd function satisfies Eq. (3). Precisely, the following proposition holds.

Proposition 1: For any function $F : \mathbb{Z} \to \mathcal{M}$, there exists a threshold set \mathcal{T} such that F is given by Eq. (3), if and only if F satisfies the following two properties:

(i) F is an odd function, *i.e.*, $F(-x) = -F(x), \forall x \in \mathbb{Z}$

(ii) F is non-decreasing, *i.e.*, $F(x) \leq F(y)$ for any x < y. We note that the above proposition also implies that F(0) = 0and $F(x) \geq 0, \forall x > 0$. In this paper, we further extend the definition of FAIDs by allowing F(0) to take on non-zero values. To ensure symmetry of the decoder, we shall write $F(0) = \pm \lambda$, with $\lambda \geq 0$, meaning that F(0) takes on either $-\lambda$ or $+\lambda$ with equal probability. In the following, F will be referred to as *framing function*.

As the focus of this work is on practical implementations, we will further assume that the sum $\gamma + \sum_{j=1}^{d_v-1} \mathfrak{m}_j$ in Eq. (2) is saturated to \mathcal{M} , prior to applying F on it. Consequently, in the sequel we shall only consider framing functions $F : \mathcal{M} \to \mathcal{M}$, and the VN-update function Φ_v from Eq. (2) is redefined as:

$$\Phi_{v}\left(\gamma,\mathfrak{m}_{1},\ldots,\mathfrak{m}_{d_{v}-1}\right)=F\left(s_{\mathcal{M}}\left(\gamma+\sum_{j=1}^{d_{v}-1}\mathfrak{m}_{j}\right)\right) \quad (4)$$

where $s_{\mathcal{M}} : \mathbb{Z} \to \mathcal{M}, s_{\mathcal{M}}(x) = \operatorname{sgn}(x) \min(|x|, Q)$, is the saturation function. Since $F(-\mathfrak{m}) = -F(\mathfrak{m}), \forall \mathfrak{m} \in \mathcal{M}, F$ is completely determined by the vector [|F(0)|, F(1), ..., F(Q)], further referred to as the *Look-Up Table (LUT)* of *F*, which satisfies the following inequalities (Proposition 1):

$$0 \le |F(0)| \le F(1) \le \dots \le F(Q) \le Q$$
 (5)

Summarizing, the subclass of FAIDs considered in this paper is defined by Eq. (4), where F is a framing function satisfying Eq. (5). Furthermore, for any integer q > 0, the expression *q*-bit FAID is used to refer to a (2Q + 1)-level FAID, with $Q = 2^{q-1} - 1$. It follows that messages exchanged within the FAID decoder are *q*-bit messages (including 1 bit for the sign). Finally, the message-passing iterative decoding process for a FAID with framing function F is depicted in Algorithm 1.

Algorithm 1 FAID decoding with framing function F

for all m = 1, ..., M and $n \in H(m)$ do \triangleright CN-processing $\beta_{m,n} = \Phi_c (\alpha_{m,n'} | n' \in H(m) \setminus n);$

▷ AP-update

for all
$$n = 1, \dots, N$$
 do
 $\tilde{\gamma}_n = \gamma_n + \sum_{m \in H(n)} \beta_{m,n};$

for all n = 1, ..., N do $\hat{x}_n = \operatorname{sign}(\tilde{\gamma}_n)$; \triangleright hard decision if $\underline{\hat{x}}$ is a codeword then exit the iteration loop \triangleright syndrome check End Iteration Loop

B. Non-Surjective FAIDs

The finite alphabet MS decoder is a particular example of FAID, with framing function $F : \mathcal{M} \to \mathcal{M}$ being the identity function. Using Eq. (5) it can be easily verified that this is the only FAID for which the framing function F is *surjective* (or equivalently *bijective*, since \mathcal{M} is finite). For any other framing function F, there exists at least one element of \mathcal{M} , which is not in the image of F. The class of FAIDs defined by non-surjective framing functions³ is investigated in this section.

Definition 2: The weight of a framing function $F : \mathcal{M} \to \mathcal{M}$, denoted by W, is the number of distinct entries in the vector [|F(0)|, F(1), ..., F(Q)]. It follows that $1 \le W \le Q + 1$. By a slight abuse of terminology, we shall also refer to W as the weight of the NS-FAID. We further define the *framing bit-length* as $w = \lceil \log_2(W) \rceil + 1$.

Definition 3: A non-surjective FAID (NS-FAID) is a FAID of weight W < Q + 1. Hence the framing function F is non-surjective, meaning that the image set of F is a strict subset of \mathcal{M} .

Table I provides two examples of q = 4-bit NS-FAIDs (hence Q = 7), both of which are of weight W = 4, hence framing bit-length $w = \lceil \log_2 4 \rceil + 1 = 3$. Note that F_1 maps 0 to 0, while F_2 maps 0 to ± 1 . The image sets of F_1 and F_2 are Im $(F_1) = \{0, \pm 1, \pm 3, \pm 7\}$ and Im $(F_2) = \{\pm 1, \pm 3, \pm 4, \pm 7\}$.

The main motivation for the introduction of NS-FAIDs is that they allow reducing the size of the memory required to store the exchanged messages. Clearly, for a NS-FAID with framing bit-length w, the exchanged messages can be represented using only w instead of q bits (including 1 bit

Table I Examples of 4-bit framing functions of weight W=4

m	0	1	2	3	4	5	6	7
$F_1(\mathfrak{m})$	0	1	1	3	3	3	7	7
$F_2(\mathfrak{m})$	±1	1	1	3	3	4	4	7

for the sign). Moreover, as a consequence of the message size reduction, the size of the interconnect network that carries the messages from the memory to the processing units is also reduced.

Proposition 4: The number of (2Q+1)-level NS-FAIDs of weight W is given by:

$$N_{\text{NS-FAID}}(Q,W) = \binom{Q}{W-1}\binom{Q+1}{W}$$
(6)

where $\binom{y}{x}$ denotes the binomial coefficient.

C. Examples of NS-FAIDs

As mentioned above, if the framing function F is the identity function, then the corresponding FAID is equivalent to the MS decoder with finite alphabet \mathcal{M} . Some examples of NS-FAIDs are provided below.

Example 1. Let $F : \mathcal{M} \to \mathcal{M}$ be defined by:

$$F(\mathfrak{m}) = \operatorname{sgn}(\mathfrak{m}) \max(|\mathfrak{m}| - \theta, 0) \tag{7}$$

where $\theta \in \{1, ..., Q-1\}$. Then, the corresponding NS-FAID is the Offset Min-Sum (OMS) decoder with offset factor θ .

Example 2. Let $F : \mathcal{M} \to \mathcal{M}$ be defined by:

$$F(\mathfrak{m}) = \begin{cases} \mathfrak{m}, & \text{if } |\mathfrak{m}| \text{ is even} \\ \operatorname{sgn}(\mathfrak{m})(|\mathfrak{m}| - 1), & \text{if } |\mathfrak{m}| \text{ is odd} \end{cases}$$
(8)

Then, the corresponding NS-FAID is the Partially OMS (POMS) decoder from [13].

Moreover, it can be seen that the MS-based decoders proposed in [14], [15] and the dual-quantization domain decoder proposed in [16] are particular realizations of NS-FAIDs.

While the main reason behind the NS-FAIDs definition consists in their ability to reduce memory and interconnect requirements, we can also argue that they may allow improving the error correction performance (with respect to MS). This is the case of both OMS and POMS decoders mentioned above. Given a target message bit-length w (e.g., corresponding to some specific memory constraint), one may try to find the framing function F of corresponding weight W, which yields the best error correction performance. The optimization of the framing function can be done by using the DE technique, which will be discussed in Section II-E.

Since F is a non-decreasing function, it can be shown that the framing function F can alternatively be applied at the CNprocessing step (instead of VN-processing), while resulting in an equivalent decoding algorithm. Whether F is applied at the VN-processing or the CN-processing step is rather a matter of implementation. When F is applied at the VN-processing step, both VN- and CN-messages belong to a strict subset of the alphabet \mathcal{M} , namely $\mathcal{M}' = \text{Im}(F) \subset \mathcal{M}$. When F is applied at the CN-processing step, only CN-messages belong to \mathcal{M}' . However, it is worth noting that many hardware

Notation: H – bipartite graph of the LDPC code, with N VNs and M CNs; H(n) – set of CNs connected to VN n; H(m) – set of VNs connected to CN m; $\alpha_{m,n}$ – message from VN n to CN m; $\beta_{m,n}$ – message from CN m to VN n; γ_n and $\tilde{\gamma}_n$ – a priori and a posteriori LLR of VN n; quant – quantization map (see also Section II-E).

³Although we restrict the study in this paper to non-surjective framing functions $F : \mathcal{M} \to \mathcal{M}$, it can be readily extended to non-surjective framing functions $F : \mathbb{Z} \to \mathcal{M}$. While such an extension would widen the class of NS-FAIDs, our preliminary investigations have shown that the best NS-FAIDs are actually those within the subclass of NS-FAIDs defined by $F : \mathcal{M} \to \mathcal{M}$, investigated in this paper.

implementations of Quasi-Cyclic (QC) LDPC decoders rely on a layered architecture, which only requires storing the checknode messages [7].

D. Irregular NS-FAIDs

In case of irregular LDPC codes, *irregular NS-FAIDs* are NS-FAIDs using different framing functions F_{d_v} for VNs of different degrees d_v . Framing functions F_{d_v} may have different weights W_{d_v} . In this case, messages outgoing from degree- d_v VNs can be represented by using only $w_{d_v} = \lceil \log_2(W_{d_v}) \rceil + 1$ bits. However, the message size reduction does not necessarily apply to CN-messages, due to the fact that a CN may be connected to VNs of different degrees. Let $\mathcal{M}'_{d_v} = \text{Im}(F_{d_v})$. Then, messages outgoing from a CN c can be represented by using:

$$\left[\log_2\left(\left|\cup_{d_v\in\mathcal{D}_c}\mathcal{M}'_{d_v}\right|\right)\right] \text{ bits,} \tag{9}$$

where \mathcal{D}_c is the set of degrees of VNs connected to c, and $|\cdot|$ is used to denote the number of elements of a set.

Alternatively, it is also possible to define CN-irregular NS-FAIDs in a similar manner. However, in this work we only deal with VN-irregular NS-FAIDs, since most of the practical irregular LDPC codes are irregular on VNs, while almost regular (or semi-regular) on CNs. In order to reduce the size of the CN-messages, in Section III-B we will further impose certain conditions on the framing functions F_{d_v} , by requiring their images being included in one another.

E. Density Evolution Analysis

For the sake of simplicity, we only consider transmission over *binary-input* memoryless noisy channels. We assume that the channel input alphabet is $\mathcal{X} = \{-1, +1\}$, with the usual convention that +1 corresponds to the 0-bit and -1 corresponds to the 1-bit, and denote by \mathcal{Y} the output alphabet of the channel. We denote by $x \in \mathcal{X}$ and $y \in \mathcal{Y}$ the transmitted and received symbols, respectively.

We further consider a function $\varphi : \mathcal{Y} \to \Gamma$ that maps the output alphabet of the channel to the input alphabet of the decoder, and set $\gamma = \varphi(y)$. Hence, φ encompasses both the computation of the soft (unquantized) log-likelihood ratio (LLR) value and its quantization. We shall refer to φ as *quantization map* and to γ as the *input LLR* of the decoder.

For transmission over the binary-input Additive White Gaussian Noise (AWGN) channel, we shall consider that the decoder's input information as well as the exchanged messages are quantized on the same number of bits; therefore $\Gamma = \mathcal{M}$ unless otherwise stated. In this case, y = x + z, where z is the white Gaussian noise with variance σ^2 , and the quantization map $\varphi : \mathcal{Y} \to \mathcal{M}$ is defined by:

$$\varphi(y) = [\mu \cdot y]_{\mathcal{M}} \tag{10}$$

where $\mu > 0$ is a constant referred to as *gain factor*, and $[x]_{\mathcal{M}}$ denotes the closest integer to x that belongs to \mathcal{M} (see also [19] and the gain factor quantizer defined therein).

The objective of the DE technique is to recursively compute the probability mass function (pmf) of the exchanged messages, through the iterative decoding process. This is done under the assumption that exchanged messages are independent, which holds in the asymptotic limit of the code length. In this case, the decoding performance converges to the cycle free case. DE equations for the NS-FAID decoder can be derived in a similar way as for the finite-alphabet MS decoder [19]. Similar to [19], the DE is used to compute the asymptotic error probability, defined as:

$$p_e^{(+\infty)} = \lim_{\ell \to +\infty} p_e^{(\ell)} \tag{11}$$

where $p_e^{(\ell)}$ is the bit error probability at iteration ℓ .

For a target bit error probability $\eta > 0$, the η -threshold is defined as the worst channel condition for which decoding error probability is less than η . Assuming the binary-input AWGN channel model, the η -threshold corresponds to the maximum noise variance σ^2 (or equivalently minimum SNR), such that the asymptotic error probability is less than η :

$$\sigma_{\text{thres}}^2(\eta) = \sup\left\{\sigma^2 \mid p_e^{(+\infty)} \le \eta\right\}$$
(12)

In case that $\eta = 0$, the η -threshold is simply referred to as DE threshold [20]. However, the asymptotic decoding performance of finite-precision MS-based decoders is known to exhibit an error floor phenomenon at high SNR [19]. This makes the η -threshold definition more appropriate in practical cases, when the target bit error rate can be fixed to a practical non-zero value.

Finally, it is worth noting that the $\sigma_{\text{thres}}^2(\eta)$ value depends on: (i) the irregularity of the LDPC code, parametrized as usual by the degree distribution polynomials $\lambda(x)$ and $\rho(x)$ [20], (ii) the NS-FAID, *i.e.*, the size of the decoder alphabet and the framing function F, (iii) the channel quantizer φ , or equivalently the gain factor μ used in Eq. (10). Therefore, assuming that the degree distribution polynomials $\lambda(x)$ and $\rho(x)$ and the size of the decoder alphabet are fixed, we use the DE technique to jointly optimize the framing function Fand channel quantizer.

III. DENSITY EVOLUTION OPTIMIZATION OF NS-FAIDS

Throughout this section, we consider q = 4-bit NS-FAIDs (hence, Q = 7). To illustrate the trade-off between hardware complexity and decoding performance, we consider the optimization of both regular and irregular NS-FAIDs.

A. Optimization of Regular NS-FAIDs

In this section, we consider the optimization of regular NS-FAIDs for $(d_v = 3, d_c = 6)$ -regular LDPC codes. We consider q = 4-bit NS-FAIDs, with framing bit-length parameter $w \in \{2,3\}$. According to Proposition 4, the number of NS-FAIDs is given by $N_{\text{NS-FAID}}(q = 4, w = 3) = N_{\text{NS-FAID}}(Q = 7, W = 4) = {7 \choose 3} {8 \choose 4} = 2450$, and $N_{\text{NS-FAID}}(q = 4, w = 2) = N_{\text{NS-FAID}}(Q = 7, W = 2) = {7 \choose 1} {8 \choose 2} = 196$.

All regular NS-FAIDs have been evaluated by using the DE technique from Section II-E. Table II summarizes the best NS-FAIDs according to w and F(0) values⁴, for $0 \le |F(0)| \le 3$;

⁴NS-FAIDs with |F(0)| > 3 have worse DE thresholds, thus they have not been included in the table.

 Table II

 BEST NS-FAIDS FOR (3, 6)-REGULAR LDPC CODES

		F	SNR-thres (dB)
w = 4	MS	$\left[0,1,2,3,4,5,6,7\right]$	1.643 ($\mu = 5.6$)
w = 3	F(0) = 0	$[{f 0},{f 1},{f 1},{f 3},{f 3},{f 3},{f 7},{f 7}]$	1.409 (μ = 3.8)
	$F(0) = \pm 1$	$[\pm 1, 1, 1, 3, 3, 4, 4, 7]$	1.412 ($\mu = 5.1$)
	$F(0) = \pm 2$	$[\pm 2, 2, 2, 3, 3, 3, 4, 7]$	1.712 ($\mu = 7.1$)
	$F(0) = \pm 3$	$[\pm 3, 3, 3, 3, 3, 4, 5, 7]$	2.227 ($\mu = 10.0$)
w = 2	F(0) = 0	$\left[0,0,0,0,0,6,6,6\right]$	2.251 ($\mu = 8.6$)
	$F(0) = \pm 1$	$[\pm 1, 1, 1, 1, 1, 6, 6, 6]$	1.834 (μ = 6.4)
	$F(0) = \pm 2$	$[\pm 2, 2, 2, 2, 2, 2, 2, 2, 7]$	1.911 ($\mu = 8.3$)
	$F(0) = \pm 3$	$[\pm 3, 3, 3, 3, 3, 3, 3, 3, 7]$	2.014 ($\mu = 9.4$)

DE thresholds ($\eta = 0$) and corresponding gain factors (μ) are also reported. Best NS-FAIDs for w = 2 and w = 3are emphasized in bold. For comparison purposes, the DE threshold of the q = 4-bit MS decoder is also reported: MS threshold is equal to 1.643 dB, for $\mu = 5.6$. For w = 3, it can be observed that best NS-FAIDs with F(0) = 0 or $F(0) = \pm 1$ have better DE thresholds than the 4-bit MS decoder. The best NS-FAID is given by the framing function F = [0, 1, 1, 3, 3, 3, 7, 7] and its DE threshold is equal to 1.409 dB ($\mu = 3.8$), representing a gain of 0.23 dB compared to 4-bit MS. For w = 2, the best NS-FAID is given by the framing function $F = [\pm 1, 1, 1, 1, 1, 6, 6, 6]$ and its DE threshold is equal to $1.834 \,\mathrm{dB}$ ($\mu = 6.4$), which represents a performance loss of only 0.19 dB compared to 4-bit MS. To emphasize the benefits of the proposed NS-FAIDs extension, we note that for w = 2, best NS-FAIDs with $F(0) = \pm 1$, $F(0) = \pm 2$ or $F(0) = \pm 3$ have better DE thresholds than the best NS-FAIDs with F(0) = 0. The latter is given by the framing function F = [0, 0, 0, 0, 0, 6, 6, 6] and its DE threshold is equal to 2.251 dB ($\mu = 8.6$), thus resulting in a performance loss of approximately 0.61 dB compared to 4-bit MS.

B. Optimization of Irregular NS-FAIDs

As a case study, we consider the optimization of irregular NS-FAIDs for the WiMAX irregular LDPC codes with rate 1/2 [21] (of course, the proposed method can be applied to any other irregular codes in the same manner). The edge-perspective degree distribution polynomials are given by $\lambda(x) = 0.2895x + 0.3158x^2 + 0.3947x^5$ and $\rho(x) = 0.6316x^5 + 0.3684x^6$. Hence, VNs are of degree $d_v \in \{2, 3, 6\}$. For each VN-degree d_v , we consider that the corresponding framing function F_{d_v} may be of any weight $W_{d_v} \in \{2, 4, 8\}$, corresponding to a framing bit-length $w_{d_v} \in$ $\{2, 3, 4\}$. Hence, the total number of framing functions is given by $N_{\text{NS-FAID}}(7,2) + N_{\text{NS-FAID}}(7,4) + N_{\text{NS-FAID}}(7,8) = 2645$ (see Proposition 4). Since a different framing function may be applied for each VN-degree, it follows that the total number of irregular NS-FAIDs is equal to $2645^3 = 18504486125$. Clearly, even though we rely on DE, it is practically impossible to evaluate the decoding performance of all the irregular NS-FAIDs. To overcome this problem, we proceed as described below.

1) Optimization procedure: First, we evaluate the DE thresholds of NS-FAIDs applying one and the same framing

function to all the variable-nodes, irrespective of their degree, which for simplicity will be referred to as *uniform* NS-FAIDs throughout this section. Uniform NS-FAIDs with framing bitlength $w = \{2, 3, 4\}$ are then sorted with increasing DE threshold value, from the best to the worst decoder. Note that the case w = 4 represents a slight abuse of terminology, since there is only one such decoder, corresponding to the original MS decoder. We further denote by $\mathcal{U}^{(\text{best})}$ -NS-FAIDw the set of best uniform NS-FAIDs with framing bit-length w, determined as follows:

- $\mathcal{U}^{(\text{best})}$ -NS-FAID-2 is comprised of the uniform NS-FAIDs with w = 2, whose DE threshold is less than or equal to 5 dB; this represents 121 decoders out of the total of $N_{\text{NS-FAID}}(Q = 7, w = 2) = 196$ decoders.
- $\mathcal{U}^{(\text{best})}$ -NS-FAID-3 is comprised of the uniform NS-FAIDs with w = 3, whose DE threshold is less than or equal to 3 dB; this represents 946 decoders out of the total of $N_{\text{NS-FAID}}(Q = 7, w = 3) = 2450$ decoders.
- $\mathcal{U}^{(\text{best})}$ -NS-FAID-4 is comprised of the MS decoder only; its DE threshold is equal to 1.374 dB.

The limiting values of the DE thresholds for $\mathcal{U}^{(\text{best})}$ -NS-FAID-2 and $\mathcal{U}^{(\text{best})}$ -NS-FAID-3 are chosen such that the number of selected NS-FAIDs in each set is small enough.

For irregular NS-FAIDs, we denote by NS-FAID- $w_2w_3w_6$ the ensemble of NS-FAIDs defined by a triplet of framing functions (F_2, F_3, F_6) , corresponding to variable node degrees $d_v = 2, 3, 6$, with framing bit-lengths w_2, w_3, w_6 . Since $w_2, w_3, w_6 \in \{2, 3, 4\}$, there are 27 such ensembles. Since the number of NS-FAIDs in these ensembles can be very large, we only evaluate part of them, by further imposing the following two constraints:

Decoding performance constraint: We only consider irregular NS-FAIDs defined by triplets of framing functions (F_2, F_3, F_6) , such that $F_{d_v} \in \mathcal{U}^{(\text{best})}$ -NS-FAID- w_{d_v} , for any $d_v \in \{2, 3, 6\}$.

Memory size reduction constraint: We further impose the following inclusion constraint between the image sets of framing functions used for different VN-degrees. Let $w^{(\max)} = \max_{d_v} w_{d_v}$ and $d_v^{(\max)} = \operatorname{argmax}_{d_v} w_{d_v}$. We impose that $\operatorname{Im}(F_{d_v}) \subseteq \operatorname{Im}(F_{d_v^{(\max)}}), \forall d_v \in \{2,3,6\}$. According to Eq. (9), this constraint ensures that CN-messages can be represented by using only $w^{(\max)}$ bits, which is particularly suitable for layered architectures.

The number of irregular NS-FAIDs that satisfy the above two constraints is equal to $N_{\text{NS-FAIDs}}^{\text{irregular}} = 7\,017\,762.$

2) Density Evolution evaluation: For each of the $N_{\text{NS-FAIDs}}^{\text{irregular}}$ irregular NS-FAIDs, we compute its decoding threshold for a target bit error rate $\eta = 10^{-6}$, using the DE technique from Section II-E. The threshold computation also encompasses the optimization of the channel gain factor μ . Hence, for each NS-FAID, we first determine the gain factor μ that maximizes the η -threshold defined in Eq. (12). The corresponding η -threshold value is then reported as the η -threshold of the NS-FAID.

Density evolution results for the MS decoder (indicated as NS-FAID-444), as well as for the NS-FAIDs with the best η -thresholds from five NS-FAID- $w_2w_3w_6$ ensembles, are shown in Table III: the framing functions used for VN-degrees

	Framing	functions a	pplied to	SNR-thres (dB)	SNR	Memor	y size redu	ction (%)
NS-FAIDs Ensemble	d - 2	d - 3	d = 6	(& gain factor μ)	gain/loss	VN-	CN-m	essages
	$u_v - 2$	$u_v = 0$	$u_v = 0$	$@BER = 10^{-6}$	(+/-dB)	mess.	uncomp.	comp.
NS-FAID-444 (MS)	LUT0	LUT0	LUT0	$1.374 \ (\mu = 3.2)$	0.000	0.00	0.00	0.00
NS-FAID-432	LUT0	LUT1	LUT6	$1.188 \ (\mu = 3.0)$	+0.186	-27.63	0.00	0.00
NS-FAID-433	LUT0	LUT3	LUT2	$1.015 \ (\mu = 2.8)$	+0.359	-17.76	0.00	0.00
NS-FAID-332	LUT4	LUT3	LUT6	$1.273 \ (\mu = 2.6)$	+0.101	-34.87	-25.00	-13.04
NS-FAID-333	LUT4	LUT4	LUT3	$1.110 \ (\mu = 2.4)$	+0.264	-25.00	-25.00	-13.04
NS-FAID-222	LUT7	LUT5	LUT5	$2.299~(\mu = 2.3)$	-0.925	-50.00	-50.00	-26.09

 Table III

 HARDWARE COMPLEXITY VS. DECODING PERFORMANCE TRADE-OFF FOR OPTIMIZED IRREGULAR NS-FAIDS

 Table IV

 LUTS USED BY NS-FAIDS IN TABLE III

 m
 LUT0
 LUT1
 LUT2
 LUT3
 LUT4
 LUT5
 LUT6
 LUT7

0	0	0	0	0	0	± 1	± 1	± 1
1	1	0	1	1	1	1	1	1
2	2	2	1	1	1	1	1	1
3	3	2	2	3	3	1	1	5
4	4	3	2	3	3	5	7	5
5	5	3	7	3	7	5	7	5
6	6	7	7	7	7	5	7	5
7	7	7	7	$\overline{7}$	7	5	7	5
w	4	3	3	3	3	2	2	2

 $d_v = 2, 3, 6$ are shown in columns 2, 3, and 4, while the η threshold value (in dB) and the corresponding gain factor μ are shown in column 5. The SNR gain (+) or loss (-) reported in column 6 corresponds to the differences between the SNR threshold of the MS decoder (NS-FAID-444) and the SNR threshold of the best NS-FAID- $w_2w_3w_6$. The memory size reduction of the NS-FAID- $w_2w_3w_6$ decoders compared to the MS decoder is reported in columns 7-9, for both VN and CN messages. For CN messages, two possibilities are considered, according to whether they are stored in an *uncompressed* or *compressed* format, where compressed format means that only the signs, first minimum, second minimum, and index of the first minimum are stored [22]. Finally, the framing functions' LUTs of the best NS-FAID- $w_2w_3w_6$ decoders are reported in Table IV.

Fig. 1 captures the trade-off between decoding performance and memory size reduction, for each of the 27 NS-FAID $w_2w_3w_6$ ensembles. For each ensemble, we select the NS-FAID with the best threshold, and indicate the corresponding memory gains and decoding performance. The height of vertical bars indicates the VN memory size reduction (values on the left vertical axis), while their color indicates the CN memory size reduction (uncompressed CN message storage is assumed in the legend). The red stems indicate the SNR threshold gain or loss compared to MS decoder (values on the right vertical axis). It can be seen that the NS-FAID-332 decoder allows a significant memory size reduction for both variableand check-node messages, while still performing 0.1 dB ahead the MS decoder. The NS-FAID-433 decoder is also a very good candidate for applications requiring increased decoding performance: it achieves the best SNR gain (0.36 dB), while providing a VN memory size reduction by 17.76% with respect to the MS decoder.

Finally, it is worth noticing that the reported memory size



Figure 1. Memory size reduction vs. decoding performance

reductions do not necessarily translate as such in hardware implementations, for several reasons. First, depending on the hardware architecture, VN messages may or may not be stored in a dedicated memory. For instance, layered architectures only require the storage of CN messages, which can be further stored in either a compressed or uncompressed format. Moreover, VN processing units (VNUs) need to be equipped with a framing and a deframing module, which may offset part of the promised gains. This is even more true in case of irregular codes, for which some VNUs may need to implement more than one single framing function, since the same VNU may be reused to process VN of different degrees (except for fully parallel architectures). To assess the gains of NS-FAIDs in practical implementations, the integration of the NS-FAID mechanism (framing/deframing modules) into two different MS decoder architectures is discussed in the next section, and ASIC synthesis results for the CMOS 65 nm process technology are provided in Section V.

IV. HARDWARE ARCHITECTURES FOR NS-FAID DECODERS

In this section we propose two layered decoder architectures for QC-LDPC codes, with both MS and NS-FAIDs decoding kernels. Proposed architectures target high-throughput, while ensuring an efficient use of the hardware resources. Two possible approaches to achieve high-throughput are explored, consisting in either pipelining the datapath, or increasing the hardware parallelism.

We consider a QC-LDPC code defined by a base matrix B of size $R \times C$, and expansion factor z, corresponding to a parity check matrix H of size $M \times N$, with M = zR and N = zC. With the notation from Section II-E, we denote by $\underline{x} = (x_1, \ldots, x_N) \in \mathcal{X}^N$ the transmitted codeword, by $\underline{y} = (y_1, \ldots, y_N) \in \mathcal{Y}^N$ the received word, and by $(\gamma_1, \ldots, \gamma_N)$ the input LLRs of the decoder, where $\gamma_n = \varphi(y_n)$ and φ is the quantization map. VN and CN messages are denoted by $\alpha_{m,n}$ and $\beta_{m,n}$, respectively, and the *A Posteriori* (*AP*)-*LLR* of a VN n is denoted by $\tilde{\gamma}_n$. Hence, $\tilde{\gamma}_n = \gamma_n + \sum_{m \in H(n)} \beta_{m,n}$, where the sum is taken over all the check-nodes m connected to n, denoted by $m \in H(n)$. Input LLRs and exchanged messages are quantized on q-bits, while AP-LLRs are assumed to be quantized on \tilde{q} bits, with $\tilde{q} > q$.

A decoding layer (or simply referred to as a layer) consists of one or several consecutive rows of B, assuming that they do not overlap, *i.e.*, each column of B has at most one nonnegative entry within each layer. It is assumed that the same number of rows of B participate in each decoding layer, which is denoted by RPL (rows per layer). Hence, the number of decoding layers is given by L = R/RPL. We further define $Z = z \times RPL$, corresponding to the number of rows of H (parity checks) within one decoding layer, and referred to as the parallelism degree of the hardware architecture. To ease the description of the hardware architectures proposed in this section, we shall assume that all CNs have the same degree, denoted by d_c . However, no assumptions are made concerning VN degrees. We present each architecture assuming the MS decoding kernel is being implemented, then we discuss the required changes in order to integrate the NS-FAID decoding kernel.

A. Pipelined architecture

The proposed architecture with MS decoding kernel is detailed in Fig. 2. A high-level representation is also shown in Fig. 5(a), for both MS and NS-FAID decoding kernels. The architecture is optimized so that to reduce the critical path. In particular, we completely reorganize the interconnect network (barrel shifters BS_INIT and BS_R, see below), thus removing the need for a barrel shifter on the writing data back side. The main blocks of the architecture are discussed below.

Input/Output buffers: The input buffer, implemented as a number of Serial Input Parallel Output (SIPO) shift registers, is used to store the input LLR values (γ_n) received by the decoder. The output buffer, is used to store the hard bit estimates of the decoded word. Input/output buffers allow data load/offload operations to take place concomitantly with the decoding of the current codeword.

Memory blocks: Two memory blocks are used, one for AP-LLR values ($\tilde{\gamma}$ _memory) and one for CN-messages (β _memory). $\tilde{\gamma}$ _memory is implemented by registers, in order to allow massively parallel read or write operations. It is organized in *C* blocks, denoted by AP_j ($j = 1, \dots, C$), corresponding to the columns of the base matrix, each one consisting of $z \times \tilde{q}$ bits. Data are read from/written to

blocks corresponding to non-negative entries in the decoding layer being processed. β_{-} memory is implemented as a dual port Random Access Memory (RAM), in order to support pipelining, as explained below. Each memory word consists of $Z \times \beta_{-}$ messages, corresponding to one decoding layer. Depending on the Check Node Unit (CNU) implementation, β_{-} messages can be either "uncompressed" (*i.e.*, for a checknode *m*, the corresponding β_{-} message is given by the d_c values $[\beta_{m,n_1}, \ldots, \beta_{m,n_{d_c}}]$, where n_1, \ldots, n_{d_c} denote the variable nodes connected to *m*) or "compressed" (*i.e.*, for a checknode *m*, the corresponding β_{-} message is given by the signs of the above β_{m,n_i} messages, their first and second minimum, denoted by min1 and min2, and the index of the first minimum, denoted by indx min1) [22].

Read and Write Permutations (PER_R, PER_W): PER_R permutation is used to rearrange the data read from $\tilde{\gamma}$ _memory, according to the processed layer, so as to ensure processing by the proper VNU/CNU. PER_W block operates oppositely to PER_R.

Barrel Shifters (BS_INIT, BS_R): Barrel shifters are used to implement the cyclic (shift) permutations, according to the non-negative entries of the base matrix. The $\tilde{\gamma}_{-}$ memory is initialized from the input LLR values stored in the input buffer. However, input LLR values are shifted by BS_INIT block before being written to the $\tilde{\gamma}$ memory, according to the last non-negative shift factor on the corresponding base matrix column. BS R blocks are then used to shift the LLR values read from the $\tilde{\gamma}$ _memory, such that to properly align them with the appropriate VNU. Note that there are $d_c BS_R_{1,\ldots,d_c}$ blocks. In case RPL = 1, a decoding layer corresponds to a row of B, and each BS_R block is used to shift the LLR values within one of the d_c columns with non-negative entries in the current row. Let i be the index of the current row. The cyclic shift implemented by a BS_R block, corresponding to a column j with $b_{i,j} \ge 0$, is given by $-b_{i',j} + b_{i,j}$, where $b_{i',j}$ is the previous non-negative entry in column j (i.e., the previous row i' with $b_{i',j} \ge 0$). In case RPL > 1, each BS_R block actually consists of RPL sub-blocks as above, with one sub-block for each row in the layer. The values of the cyclic shifts are computed offline for each layer ℓ . This eliminates the need for data write-back barrel shifters, thus reducing the critical path of the design. Finally, the BS INIT block operates oppositely to BS_INIT, and is used to shift back the hard decision bits into appropriate positions.

Variable Node Units (VNUs) and AP-LLR Units: These units compute VN-messages $(\alpha_{m,n})$ and AP-LLR values $(\tilde{\gamma}_n)$. Each VN message is computed by subtracting the corresponding CN message from the AP-LLR value, that is $\alpha_{m,n} = \tilde{\gamma}_n - \beta_{m,n}$. This operation is implemented by a \tilde{q} -bit subtractor, hence the $\alpha_{m,n}$ value outputted by the VNU is quantized on \tilde{q} bits. The AP-LLR value is updated by the AP-LLR unit, by $\tilde{\gamma}_n = \alpha_{m,n} + \beta_{m,n}^{\text{new}}$, where $\beta_{m,n}^{\text{new}}$ is the corresponding CN message computed at the current iteration (see below).

Saturators (SATs): Prior to CNU processing, $\alpha_{m,n}$ values are saturated to q bits.

Check Node Units (CNUs): These processing units compute the CN-messages ($\beta_{m,n}$). For simplicity, Fig. 2 shows one CNU block with d_c inputs, each one of size $Z \times q$ bits. Thus,



Figure 2. Block Diagram of the Proposed Pipelined Architecture with MS-kernel

this block actually includes Z computing units, used to process in parallel the Z check-nodes within one layer. The CNU is implemented by using either: (i) the high-speed low-cost treestructure (TS) approach proposed in [23] for "compressed" CN-messages, or (ii) comparator trees for "uncompressed" CN-messages.

Decompress (DCP): This block is only used in case that the CN-messages are in compressed format (signs, min1, min2, indx_min1). It converts the β _messages from compressed to the uncompressed format.

Controller: This block generates control signals such as *count_layer_read*, *count_layer_write* to indicate which layers are being processed, *write_en* to enable data writing, etc. It also controls the synchronous execution of the other blocks.

Pipelining: To increase the operating frequency, the data path is pipelined by adding a set of registers after the VNUblocks. The timing schedule is shown in Fig. 5(a), where the two pipeline stages (P1 and P2) are indicated by purple and brown arrows. Hence, processing one layer takes 2 clock cycles, but at each clock cycle the two pipeline stages work on two consecutive layers of the base matrix. This imposes specific constraints on the base matrix, as consecutive layers must not overlap, in order to avoid $\tilde{\gamma}$ -memory conflicts (note that memory stall cycles would cancel the pipelining effect). An example of $d_c = 6$ regular base matrix without overlap between consecutive layers is given in Fig. 3, assuming that each layer corresponds to one row of the base matrix.

Regular NS-FAID decoding kernel: The changes required to integrate a regular NS-FAID decoding kernel, with framing

49	-1	-1	-1	-1	43	-1	-1	-1	-1	50	-1	-1	-1	-1	2	-1	27	-1	-1	-1	-1	-1	49
-1	-1	-1	10	41	-1	-1	-1	-1	52	-1	-1	32	-1	-1	-1	-1	-1	50	-1	50	-1	-1	-1
-1	-1	20	-1	-1	-1	-1	20	-1	-1	-1	51	-1	10	-1	-1	47	-1	-1	-1	-1	-1	33	-1
-1	24	-1	-1	-1	-1	22	-1	53	-1	-1	-1	-1	-1	31	-1	-1	-1	-1	18	-1	47	-1	-1
10	-1	-1	-1	15	-1	-1	-1	-1	-1	2	-1	-1	-1	-1	50	-1	13	-1	-1	-1	-1	-1	53
-1	-1	44	-1	-1	6	-1	-1	-1	-1	-1	29	-1	40	-1	-1	16	-1	-1	-1	13	-1	-1	-1
-1	2	-1	-1	-1	-1	-1	13	41	-1	-1	-1	-1	-1	42	-1	-1	-1	-1	48	-1	49	-1	-1
-1	-1	-1	36	-1	-1	24	-1	-1	50	-1	-1	12	-1	-1	-1	-1	-1	10	-1	-1	-1	48	-1
-1	-1	47	-1	50	-1	-1	-1	-1	-1	0	-1	-1	-1	-1	9	-1	7	-1	-1	-1	-1	-1	28
6	-1	-1	-1	-1	-1	5	-1	-1	-1	-1	13	-1	3	-1	-1	29	-1	-1	-1	16	-1	-1	-1
-1	-1	-1	35	-1	16	-1	-1	37	-1	-1	-1	4	-1	-1	-1	-1	-1	24	-1	-1	-1	29	-1
-1	24	-1	-1	-1	-1	-1	51	-1	38	-1	-1	-1	-1	6	-1	-1	-1	-1	23	-1	16	-1	-1

Figure 3. Base matrix of the (3,6)-regular QC-LDPC code

function F, are shown in Fig. 5(a). First, the Saturation (SAT) block used within the MS-decoding kernel is replaced by a Framing (FRA) block. Note that the output of the VNU consists of \tilde{q} -bit (unsaturated) VN-messages. Hence, the FRA block actually implements the concatenation of the following operations, corresponding to $F \circ s_{\mathcal{M}}$ in Eq. (4):

$$-\tilde{Q}, \dots, +\tilde{Q}] \xrightarrow{s_{\mathcal{M}}} [-Q, \dots, +Q] \xrightarrow{F} \operatorname{Im}(F) \xrightarrow{\sim} [-W, \dots, +W],$$
(13)

where $[-\tilde{Q}, \ldots, +\tilde{Q}]$ is the alphabet of unsaturated messages $(\tilde{Q} = 2^{\tilde{q}-1} - 1), F$ is the framing function being used, $\operatorname{Im}(F)$ is the image of F (which is a subset of $[-Q, \ldots, +Q]$ according to the framing function definition), and the last operation consists of a re-quantization of the $\operatorname{Im}(F)$ values on a number of w-bits, where $w = \lceil \log_2(W) \rceil + 1$ is the framing bit-length. The De-framing (DE-FRA) block simply converts back from w-bit to q-bit values $([-W, \ldots, +W] \xrightarrow{\sim} \operatorname{Im}(F) \subset [-Q, \ldots, +Q])$, *i.e.*, it inverts the re-quantization operation above. Although we have to add the de-framing blocks, the reduction of the CN-messages size may still save significant

	VNU1	VNU2	VNU3	VNU4	VNU5	VNU6	VNU7
Layer 1	<i>v</i> 2	v13	<i>v</i> 9	v10	<i>v</i> 3	v14	_
Layer 2	<i>v</i> 4	<i>v</i> 6	<i>v</i> 5	<i>v</i> 8	<i>v</i> 12	v15	v16
Layer 3	<i>v</i> 7	<i>v</i> 3	v11	v10	v17	v18	
Layer 4	<i>v</i> 1	<i>v</i> 6	v13	v12	<i>v</i> 8	v24	-
Layer 5	<i>v</i> 4	v3	v11	v10	v19	v20	-
Layer 6	v1	<i>v</i> 6	<i>v</i> 5	v8	v12	v21	v22
Layer 7	<i>v</i> 4	<i>v</i> 3	<i>v</i> 9	v10	v23	v24	-
Layer 8	<i>v</i> 2	<i>v</i> 6	ν7	v8	v12	v14	v15
Layer 9	<i>v</i> 1	<i>v</i> 3	<i>v</i> 9	v19	v16	v17	-
Layer 10	<i>v</i> 5	<i>v</i> 6	v13	v12	<i>v</i> 8	v18	v19
Layer 11	<i>v</i> 2	<i>v</i> 3	v7	v10	v20	v21	_
Layer 12	<i>v</i> 6	<i>v</i> 8	v11	v12	v22	v23	_
No. FRAs	2	2	1	1	2	1	1

Figure 4. Mapping between VNs and VNUs. In black: VNs of degree 2, in red: VNs of degree 3, in blue: VNs of degree 6.

hardware resources, as compared to MS decoding. This will be discussed in more details in Section V.

Irregular NS-FAID decoding kernel: First, we note that the pipeline architecture proposed in the section can be applied to the WiMAX QC-LDPC code with rate 1/2, considered in Section III-B, by assuming that each decoding layer consists of one row of the base matrix. Indeed, it is known that for this code, the rows of the base matrix can be reordered, such that any two consecutive rows do not overlap [24].

Regarding the integration of an irregular NS-FAID decoding kernel, the same framing (FRA) or de-framing (DE-FRA) block is reused for several VNs, which may be of different degrees. This may require several framing functions to be implemented within the FRA/DE-FRA blocks, thus increasing the hardware complexity. To overcome this problem, one may change the way the VNs are mapped to the processing units, by reordering the columns of the base matrix processed within each decoding layer. We determine offline such a reordering for each decoding layer, so as to minimize the number of FRA/DE-FRA blocks implementing more than one single framing function. Hence, the PER_R and PER_W blocks, which ensure the proper alignment between data and processing units, are redefined accordingly.

The optimal mapping between VNs and VNUs is shown in Fig. 4, for the base matrix with reordered rows from [24]. For each VNU, we indicate the index of the VN (or equivalently, base matrix column) processed by the VNU, within each decoding layer. The last row of the table indicates the number of framing functions that have to be implemented within the FRA/DE-FRA blocks corresponding to each VNU. One may see that 3 of the FRA/DE-FRA blocks must implement two framing functions, while the other 4 FRA/DE-FRA blocks implement only one framing function.

B. Full layers architecture

A different possibility to increase throughput is to increase the hardware parallelism, by including several non-overlapping rows of the base matrix in one decoding layer. For instance, for the base matrix in Fig. 3, we may consider RPL = 4 consecutive rows per decoding layer, thus the number of decoding layers is L = 3. In this case, each column of the base matrix has one (and only one) non-zero entry in each decoding layer; such a decoding layer is referred to as being *full*. Full layers correspond to the maximum hardware parallelism that can be exploited by layered architectures, but they also prevent the pipelining of the data path. One possibility to implement a full-layer decoder is to use a similar architecture to the pipelined one, by removing the registers inserted after the VNU (since pipelining is incompatible with the use of full-layers), and updating the control unit. However, in such an architecture, read/write operations from/to the β memory would occur at the same memory location, corresponding to the current layer being processed ℓ . This would require the use of asynchronous dual-port RAM to implement the β _memory, which in general is known to be slower than synchronous dualport RAM. The architecture proposed in this section, shown in Fig. 5(b), is aimed at avoiding the use of asynchronous RAM, while providing an effective way to benefit from the increased hardware parallelism enabled by the use of full layers. We discuss below the main changes with respect to the pipelined architecture from the previous section, consisting of the α memory and the barrel shifters blocks (the other blocks are the same as for the pipelined architecture), as well as a complete reorganization of the data path. However, it can be easily verified that both architectures are logically equivalent, *i.e.*, they both implement the same decoding algorithm.

 α _memory: This memory is used to store the VN-messages for the current decoding layer (unlike the previous architecture, the AP-LLR values are not stored in memory). Since only one \tilde{q} -bit (unsaturated) VN-message is stored for each variablenode, this memory has exactly the same size as the $\tilde{\gamma}$ _memory used within the previous pipelined architecture. VN-messages for current layer ℓ are read from the α memory, then saturated or framed depending on the decoding kernel, and supplied to the corresponding CNUs. CN-messages computed by the CNUs are stored in the β memory (location corresponding to layer ℓ), and also forwarded to the AP-LLR unit, through the DCP (decompress) and DE-FRA (de-framing) blocks, according to the CNU implementation (compressed or uncompressed) and the decoding kernel (MS of NS-FAID). The AP-LLR unit computes the sum of the incoming VN- and CNmessages, which corresponds to the AP-LLR value to be used at layer $\ell + 1$ (since already updated by layer ℓ). The AP-LLR value is forwarded to the VNU, through corresponding BS and PER blocks. Eventually, the VN-message for layer $\ell + 1$ is computed as the difference between the incoming AP-LLR and the corresponding layer- $(\ell + 1)$ CN-message computed at the previous iteration, the latter being read from the β _memory.

PER/BS blocks: PER_1/BS_1 blocks permute/shift the data read from the input buffer, according to the positions/values of the non-negative entries in the first decoding layer. Similarly to the BS_R blocks in the pipelined architecture, the PER_WR/BS_WR blocks permute/shift the AP-LLR values, according to the *difference* between the positions/values of the current layer's (ℓ) non-negative entries and those of the next layer ($\ell + 1$). This way, VN-messages stored in the α _memory are already permuted and shifted for the subsequent decoding layer. Finally, PER_L/BS_L blocks permute/shift the hard decision bits (sign of AP-LLR values), according to the positions/values of the non-negative entries in the last decoding layer.



Figure 5. High-Level Description of the Proposed HW Architectures, with both MS and NS-FAID kernels

V. IMPLEMENTATION RESULTS

This section reports implementation results, as well as the error correction performance of the implemented codes, in order to corroborate the analytic results obtained in Section III. As mentioned in the previous section, both architectures are logically equivalent, thus they both yield the same decoding performance (assuming that they implement the same MS/NS-FAID decoding kernel), but they may have different performance in terms of area and throughput.

A. Regular LDPC Codes

We consider the (3, 6)-regular QC-LDPC code with base matrix B of size $R \times C = 12 \times 24$, shown in Fig. 3. The expansion factor z = 54, thus the codeword length is N = zC = 1296 bits. The base matrix can be divided in either L = 12 decoding layers (RPL = 1), for the pipelined architecture, or L = 3 horizontal decoding layers (RPL = 4), for the fulllayer architecture.

Fig. 6(a) shows the Bit-Error Rate (BER) performance of the MS decoder with quantization parameters $(q, \tilde{q}) = (4, 6)$, as well as q = 4-bit NS-FAIDs with w = 2 and w = 3(framing functions F corresponding to w and F(0) values in the legend are those from Table II). Binary input AWGN channel model is considered, with 20 decoding iterations. It can be seen that the simulation results corroborate the analytic results from Section III-A, in terms of SNR gain / loss provided by NS-FAIDs, as compared to MS. For comparison purposes, we have further included simulations results for the floatingpoint Belief Propagation (BP) decoder [12], as well as the MS decoder with (3, 5) and (2, 4)-quantization.

ASIC post-synthesis implementation results on 65nm-CMOS technology are shown in Table V, for the MS(4,6)

decoder and the NS-FAIDs with (w = 3, F(0) = 0) and $(w = 2, F(0) = \pm 1)$, indicated in the table as NS-FAID-3 and NS-FAID-2, respectively. The first (Variant) row in Table V indicates the architecture (pipelined or full layers) and the CNU type (compressed or uncompressed). We also note that for the NS-FAID-2, the assumption that 0 is mapped to either -1 or +1, with equal probability, is only needed for theoretical analysis (the symmetry of the decoder allows reducing the analysis to the all-zero codeword). However, in practical situations one may always map 0 to +1, since random codewords are transmitted (for instance, in telecommunications systems, pseudo-randomness of the transmitted data is ensured by a scrambling mechanism).

Throughput reported in Table V is given by the formula:

Throughput =
$$\frac{N \times f_{\text{max}}}{\delta + L \times n_{\text{iter}}},$$
 (14)

where f_{max} is the maximum operating frequency (post synthesis), n_{iter} is the number of decoding iterations (set to 20), and $\delta = 1$ for the pipelined architecture or $\delta = 0$ for the full layers architecture. To keep the throughput comparison on an equal basis, we further define the *Throughput to Area Ratio* metric TAR = Throughput / Area (Mbps/mm²).

While the NS-FAID-3 decoder outperforms the baseline MS(4, 6) decoder by 0.19 dB at BER = 10^{-5} (Fig. 6(a)), it can be seen from Table V that it also exhibits a TAR improvement between 18.88% and 31.61%, depending on the hardware architecture and CNU type. As predicted, the NS-FAID-2 decoder exhibit a performance loss of 0.21 dB compared to MS(4, 6), but yields a significant TAR improvement, by 34.37% to 58.75%.



Figure 6. BER performance of optimized regular and irregular NS-FAIDs

 Table V

 ASIC post-synthesis implementation results on 65nm-CMOS technology for (3, 6) regular LDPC

Variant pipelined.uncompressed					elined.com	pressed	full_l	ayers.uncon	npressed	full_layers.compressed			
Decoder	MS(4,6)	NS-FAID-3	NS-FAID-2	MS(4,6)	NS-FAID-3	NS-FAID-2	MS(4,6)	NS-FAID-3	NS-FAID-2	MS(4,6)	NS-FAID-3	NS-FAID-2	
Max. Freq. (MHz)	200	222	227	175	200	208	151	172	192	125	147	172	
Throughput (Mbps)	1075	1193	1220	941	1075	1118	3261	3715	4147	2700	3175	3715	
Area (mm ²)	0.45	0.42	0.38	0.41	0.38	0.36	0.80	0.72	0.68	0.75	0.67	0.65	
TAR (Mbps/mm ²)	2389	2840	3210	2295	2828	3105	4076	5159	6098	3600	4738	5715	
$\pm\%$ w.r.t. MS(4,6)	0	+18.88	+34.37	0	+23.22	+35.29	0	+26.57	+49.61	0	+31.61	+58.75	

B. Irregular LDPC Codes

We consider the irregular WiMAX QC-LDPC code of rate 1/2, with base matrix of size $R \times C = 12 \times 24$ [21]. The expansion factor z = 96, thus resulting in a codeword length N = zC = 2304 bits. The pipelined architecture from Section IV-A is implemented, with RPL = 1 row per decoding layer, after reordering the rows of the base matrix, such that any two consecutive rows do not overlap [24]. Note that the full layers architecture does not apply to irregular WiMAX LDPC codes, since it is not possible to group the rows of the base matrix in full decoding layers.

BER results for the MS(4,6) decoder and the NS-FAID $w_1w_2w_3$ decoders from Table III are shown in Fig. 6(b), while ASIC post-synthesis implementation results on 65nm-CMOS technology are shown in Table VI. The throughput reported is computed using Eq. (14). TAR results and corresponding gain/loss (+/-) with respect to the MS(4,6) decoder are reported on the last row. The NS-FAID-433 and NS-FAID-432 decoders outperform the MS decoder by 0.3 dB and 0.15 dB (at BER = 10^{-5}), respectively, at the price of a small degradation of the TAR. NS-FAIDs-333 improves the BER performance by $0.12 \,\mathrm{dB}$, with TAR improvement by 13.51% to 16.39%, depending on the CNU type (compressed or uncompressed). NS-FAIDs-332 exhibits similar BER performance, with TAR improvement by 13.51% to 19.30%. The NS-FAID-222 decoder yields the most significant TAR improvement (up to 42.09%), but this comes at the price of a significant BER degradation by $\approx 1 \, dB$ as estimated in Section III-B.

To further emphasize the high-throughput characteristic of the proposed architecture, the irregular NS-FAID-332 decoder is further compared with other state of the art implementations of WiMAX decoders in Table VII. We also report the TAR and Normalized TAR (NTAR) metrics, so as to keep the throughput comparison on an equal basis with respect to technology, area, and number of iterations. To scale throughput and area to 65nm, we use scale factors (technology_size/65) and (65/technology_size)², respectively, as suggested in [28]. The computation of the TAR and NTAR metrics is detailed in the footnote to Table VII. Note that for all the reported implementations, the achieved throughput is inversely proportional to the number of iterations, hence the NTAR metric corresponds to the TAR value assuming that only one decoding iteration is performed. We mention that the decoders proposed in [24], [27] are reconfigurable decoders that support the IEEE 802.16e (WiMAX) and and the IEEE 802.11n (WiFi) wireless standards. The reported throughput is the maximum achievable coded throughput for the (1152, 2304) WiMAX code, with either 10 or 5 decoding iterations. From Table VII it can be seen that the proposed irregular NS-FAID compares favorably with state of the art implementations, yielding a NTAR value of 45.86 Gbps/mm²/iteration.

VI. CONCLUSION

In this paper, we first introduced the new framework of Non-Surjective FAIDs, which allows trading off decoding

Variant		р	ipelined.u	ncompress	sed	pipelined.compressed						
Decoder	MS(4,6)	NS-FAID	NS-FAID	NS-FAID	NS-FAID	NS-FAID	MS(4,6)	NS-FAID	NS-FAID	NS-FAID	NS-FAID	NS-FAID
		433	432	333	332	222		433	432	333	332	222
Max. Freq. (MHz)	175	172	178	192	192	200	161	156	161	178	178	200
Throughput (Mbps)	1673	1644	1701	1835	1835	1912	1539	1491	1539	1701	1701	1912
Area (mm ²)	0.87	0.88	0.90	0.82	0.80	0.70	0.77	0.79	0.79	0.75	0.75	0.72
TAR (Mbps/mm ²)	1922	1868	1890	2237	2293	2731	1998	1887	1948	2268	2268	2655
$\pm\%$ w.r.t. MS(4,6)	0	-2.81	-1.66	+16.39	+19.30	+42.09	0	-5.56	-2.50	+13.51	+13.51	+32.88

Table VI ASIC post-synthesis implementation results on 65nm-CMOS technology for WiMAX LDPC

Table VII COMPARISON BETWEEN THE PROPOSED NS-FAID AND STATE OF THE ART IMPLEMENTATIONS FOR THE WIMAX QC-LDPC CODE

Decoders	K. Zhang'09 [25]	B. Xiang'11 [6]	T. Heidari'13 [26]	W. Zhang'15 [24]	K. Kanchetla'16 [27]	This work NS-FAID-332
Code length	2304	576-2304	2304	576-2304 ^(†)	576-2304(†)	2304
Technology (nm)	90	130	130	40	90	65
Frequency (MHz)	950	214	100	290	149	192
Iterations	10	10	10	10	5	20
Throughput (Mbps)	2200	955	183	2227	955	1835
Tput scaled to 65nm (Mbps)	3036	1910	366	1370	1318	1835
Area (mm ²)	$2.90^{(*)}$	$3.03^{(*)}$	$6.90^{(**)}$	2.26 ^(*)	$11.42^{(*)}$	$0.80^{(*)}$
Area scaled to 65nm (mm ²)	$1.51^{(*)}$	$0.76^{(*)}$	$1.73^{(**)}$	5.97(*)	5.94(*)	$0.80^{(*)}$
TAR (Mbps/mm ²)	2011	2513	212	229	222	2293
NTAR (Mbps/mm ² /iter)	20110	25130	2120	2290	1110	45860

(†) support both WiMAX and Wi-Fi standards

(*) only core area is reported

(**) total chip area is reported

TAR = (Throughput scaled to 65nm) / (Area scaled to 65nm)

NTAR = TAR \times Iterations

performance for hardware complexity reductions. NS-FAIDs have been optimized by density evolution and shown to provide significant memory size reductions, with similar or event better decoding performance, as compared to the MS decoder. Then, two hardware architectures have been presented, making use of either pipelining or increased hardware parallelism in order to increase throughput. Both MS and NS-FAID decoding kernels have been integrated into each of the two proposed architectures, and compared in terms of area and throughput. ASIC post synthesis implementation results demonstrated the effectiveness of the NS-FAID approach in yielding significant improvements in terms of area and throughput, as compared to the MS decoder, with even better or only slightly degraded decoding performance.

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Note concerning prior work: Preliminary version of part of this work has been previously published in [17], [18]. In this paper, the previous definition and density-evolution analysis of NS-FAIDs [17] is extended to framing functions with $F(0) = \pm \lambda$, such as to cover a larger class of decoders, which is shown to significantly improve the decoding performance in case that the exchanged messages are quantized on a small number of bits (e.g., 2 bits per exchanged message). Optimization results presented in Section III are new, and they report on the optimization of regular and irregular NS-FAIDs, by taking into account the proposed extension. The hardware architectures proposed in [18] have been extended to cover the case of irregular NS-FAIDs. In addition, implementation results reported in this paper target an ASIC technology, which is more likely to reflect the benefits of the proposed NS-FAID approach in terms of throughput/area trade-off. All the implementation results reported in Section V (for both regular and irregular codes) are new.