Editorial

As 2018 draws to an end, so does my second and final term as the Editor-in-Chief (EiC) of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTERGATION (VLSI) SYSTEMS (TVLSI). It gives me great pleasure to announce that Prof. Massimo Alioto from the National University of Singapore will be the new EiC, effective from January 2019. Massimo is widely respected for his outstanding research in many areas of VLSI circuits and system design, and he served admirably as an Associate EiC of TVLSI during my two EiC terms. I am grateful to him for his help and constant support. Under Massimo's able leadership, TVLSI will continue to be the leading journal and top-choice publication venue for VLSI system design. His biography and photograph are included below. As the incoming EiC, Massimo will select the new editorial board. However, the current AEs will continue to make decisions until all the papers assigned to them have received final decisions. This should enable a seamless transition from this TVLSI EiC term to the next.

It also gives me great pleasure to report on the state of the journal and our performance metrics. Over the past four years, TVLSI has seen a healthy increase in the number of submissions—from 687 in 2014 to 868 in 2017, and at the time of writing of this editorial, we are at 672 submissions for 2018. We expect the number of submissions for 2018 to cross 800 before the end of the year. TVLSI, therefore, continues to be the premier archival journal for university researchers and industry practitioners in the broad area of VLSI system design.

We continue to be highly selective in order to ensure quality, and our acceptance rate today stands at 34.5%. The authors deserve a lot of credit for submitting their quality publications to TVLSI and helping to raise its standards. Our review cycle times have improved significantly since 2014 and we take pride in providing authors with thorough reviews within two months of submission in most cases. For regular papers, our average time-to-decision for the first round of review is only 58 days. For brief papers, we provide a decision within 58 days on average. When revised manuscripts are also counted, our time-to-decision for regular (brief) papers is only 50 days. This accomplishment has been made possible by the hard work and continued diligence of the Associate Editors. I thank them for their dedicated service, commitment to timeliness, and emphasis on quality for the papers that are recommended for publication. TVLSI is proud to have such an outstanding editorial board, and it has been my honor and privilege to lead this group of editors. I also commend the reviewers who have so tirelessly discharged their duties over the last four years by consistently providing timely and thorough reviews and helping us to maintain our high standards and time-to-decision timeline.

I am also glad to report that, during my two terms as the EiC, we have successfully addressed the long-standing problem of publication backlog for TVLSI. When I started my EIC term, we were limited to an annual page budget of 2400 pages and papers were in the publication queue for nearly 1.5 years. While IEEE Xplore provides Early Access in a timely manner for accepted papers, it is nevertheless frustrating for authors to wait for so long to see their papers printed in hardcopy form. I am grateful to IEEE for increasing our annual page budget to 3600 papers and our publication wait time is now down to a "steady-state" of four months.

Thanks to our increased page budget and shorter publication wait time, we have been able to publish special sections on hot topics and emerging themes in the past two years. We will publish two special sections in 2019 titled *Security and Privacy Analytics* and *Security Challenges and Solutions with Emerging Computing Technologies.* In October 2017, we published a special section titled *Alternative Computing and Machine Learning for Internet of Things*. A special section titled *Memristive Device-Based Computing: Circuit and Architecture Design, Automation and Computing* is being published in this issue.

I take this opportunity to thank the TVLSI steering committee for support and guidance. I am grateful to the steering committee members for the trust and confidence that they have placed in me. Profs. Niraj Jha (2015–2016) and Joerg Henkel (2017–2018) have been my pillars of support, along with the other committee members [An-Yeu (Andy) Wu, Yehea Ismail, Jorge Henkel, Kevin Skadron, and Hideto Hidaka].

I also thank Stacey Weber Jackson for her immeasurable contributions to TVLSI as the journal administrator. She has been my go-to-person on all TVLSI administrative matters and a constant source of support for authors, reviewers, and Associate Editors. I applaud her dedication to TVLSI and thank her for her efforts in ensuring that the journal runs smoothly in every way. I am very glad that Stacey will continue to be associated with TVLSI as the journal administrator during the new EiC's term. I would also like to thank Mr. Patrick Kempf, Ms. Joanna Gojlik, Ms. Sonal Parikh, Ms. Kylie Fritzinger, and all other staff members at IEEE for their help in ensuring smooth journal operations.

I note with sadness the passing away recently of the former TVLSI EiC and steering committee member Prof. Nagarajan (Ranga) Ranganathan. Ranga was a dear friend and I will always feel his loss. In this issue, we are publishing an *In Memorium* piece dedicated to Ranga.

In conclusion, I wish the TVLSI readership a very happy new year and continued professional success. I look forward to being associated with TVLSI in other roles and contribute to its future success.

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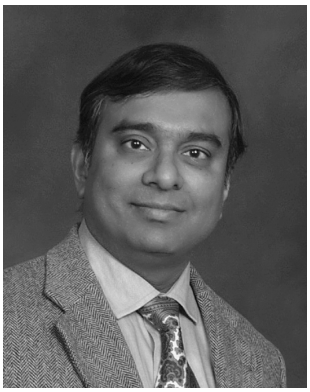
KRISHNENDU CHAKRABARTY, *Editor-in-Chief*



Krishnendu Chakrabarty (S'91–M'92–SM'00–F'08) received the B.Tech. degree from IIT Kharagpur, Kharagpur, India, in 1990, and the M.S.E. and Ph.D. degrees from the University of Michigan, Ann Arbor, MI, USA, in 1992 and 1995, respectively.

He is the William H. Younger Distinguished Professor of Engineering, the Department Chair of Electrical and Computer Engineering, and a Professor of computer science at Duke University, Durham, NC, USA. He was a Visiting Professor at the University of Tokyo, Tokyo, Japan, and the Nara Institute of Science and Technology, Ikoma, Japan, and a Visiting Chair Professor at Tsinghua University, Beijing, China, and National Cheng Kung University, Tainan, Taiwan. He is currently an Honorary Chair Professor at National Tsing Hua University, Hsinchu, Taiwan, and an Honorary Professor at Xidian University, Xi'an, China. He holds 11 U.S. patents, with several patents pending. His current research interests include testing and design-for-testability of integrated circuits and systems; microfluidic biochips; hardware security; machine learning for fault diagnosis and failure prediction; and neuromorphic computing systems. He has authored 20 books on these topics (with one translated into Chinese and three more books in press), published over 680 papers in journals and refereed conference proceedings, and given over 300 invited, keynote, and plenary talks.

Dr. Chakrabarty is a Fellow of the Association for Computing Machinery (ACM), a Fellow of the American Association for the Advancement of Science (AAAS), and a Golden Core Member of the IEEE Computer Society. He is a Research Ambassador of the University of Bremen, Bremen, Germany, and a Hans Fischer Senior Fellow at the Institute for Advanced Study, Technical University of Munich, Munich, Germany. He was a recipient of the 2008 Duke University Graduate School Dean's Award for Excellence in Mentoring and the 2010 Capers and Marion McDonald Award for Excellence in Mentoring and Advising from the Pratt School of Engineering, Duke University, the National Science Foundation CAREER Award, the Office of Naval Research Young Investigator Award, the Humboldt Research Award from the Alexander von Humboldt Foundation, Germany, the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS Donald O. Pederson Best Paper Award in 2015, the *ACM Transactions on Design Automation of Electronic Systems* Best Paper Award in 2017, and over a dozen best paper awards at major conferences. He was also a recipient of the IEEE Computer Society Technical Achievement Award in 2015, the IEEE Circuits and Systems Society Charles A. Desoer Technical Achievement Award in 2017, the Semiconductor Research Corporation Technical Excellence Award in 2018, the IEEE Test Technology Technical Council Bob Madge Innovation Award in 2018, the Distinguished Alumnus Award from IIT Kharagpur in 2014, and multiple IBM Faculty Awards and HP Labs Open Innovation Research Awards. He was a 2018 recipient of the Japan Society for the Promotion of Science Fellowship in the Short Term S: Nobel Prize Level Category. He has also presented 60 tutorials at major international conferences. He has served as the Editor-in-Chief for IEEE DESIGN & TEST OF COMPUTERS from 2010 to 2012 and the *ACM Journal on Emerging Technologies in Computing Systems* from 2010 to 2015. He currently serves as the Editor-in-Chief for the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He is also an Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, the IEEE TRANSACTIONS ON MULTISCALE COMPUTING SYSTEMS, and the *ACM Transactions on Design Automation of Electronic Systems*. He has served as a Distinguished Visitor of the IEEE Computer Society from 2005 to 2007 and from 2010 to 2012, a Distinguished Lecturer of the IEEE Circuits and Systems Society from 2006 to 2007 and from 2012 to 2013, and an ACM Distinguished Speaker from 2008 to 2016.