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2019

Liang, Y., Boon, C. C., Li, C., Tang, X.-L., Ng, H. J., Kissinger, D., ... Yu, H. (2019). Design and analysis of D-Band on-chip modulator and signal source based on split-ring resonator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 27(7), 1513-1526. doi:10.1109/TVLSI.2019.2906680

https://hdl.handle.net/10356/138119

https://doi.org/10.1109/TVLSI.2019.2906680

Design and Analysis of D-band on-chip Modulator and Signal Source based on Split-Ring Resonator

Yuan Liang, *Student Member*, *IEEE*, Chirn Chye Boon, *Senior Member*, *IEEE*, Chenyang Li, Xiao-Lan Tang, Herman Jalli Ng, *Member, IEEE*, Dietmar Kissinger, *Senior Member, IEEE*, Yong Wang, *Member, IEEE*, Qingfeng Zhang, *Senior Member, IEEE*, and Hao Yu, *Senior Member*, *IEEE*

***Abstract*— In an effort towards high-speed and low-power I/O data link in future Exa-scale data server, this paper presents a signal source and a modulator in D-band. Split-ring resonator (SRR) structures are used in both to boost the signal power and extinction ratio (ER). The modulator manifests itself as a compact SRR whose magnetic resonance frequency can be modulated by high speed data. Such a magnetic metamaterial achieves a significant reduction of radiation loss with high ER by stacking two auxiliary SRR unit-cells with interleaved placement. The high-*Q* tank for oscillation is realized by a stacked SRR decorated with slow-wave transmission line (T-line) for electric field confinement. A 4-ways power combined fundamental 80-GHz coupled-oscillator-network is magnetically synchronized by the slow-wave T-line, which is frequency doubled to 160 GHz. Fabricated in 65-nm CMOS process, the measured results show that: 1) the modulator achieves 3 dB insertion loss at on-state with 43 dB isolation at off-state, leading to a 40-dB ER at 125 GHz within an area of only 40 µm × 67 µm. 2) The signal source achieves 6.3% frequency tuning range (FTR) with 3.7 mW peak output power at 160 GHz within 0.053 mm^2 active area. It has a measured phase noise of –105 dBc/Hz at 10 MHz offset, 5.5% DC-to-RF power efficiency, 70.1 mW/mm^2 power density, FOM of –171 dBc/Hz and FOM$_T$ of –172.7 dBc/Hz.**

***Index Terms*—CMOS oscillator, coupled oscillator network, high output power density, metamaterial, modulator, slow wave, split-ring resonator, terahertz (THz).**

I. Introduction

FUTURE EXASCALE data servers require integration of 1000 cores with high speed (>20 Gb/s) communications on-chip and high energy efficiency (<1 pJ/b/mm) [1]. Two mainstream circuit solutions, including electronics [1], [2] and photonics [3], [4], are preferred. Optical interconnects have shown good energy efficiency with reconfigurable capability, but it is difficult to be fully integrated in CMOS technology. Furthermore, broadband electronic I/O is constrained by loss and EM crosstalk in high frequencies.

This paragraph of the first footnote will contain the date on which you submitted your paper for review. This work was supported by the Singapore Ministry of Education Academic Research Fund Tier 1 (MOE RG86/16).

Y. Liang, C. C. Boon and C. Li are with the School of Electrical and Electronic Engineering, Nanyang Technological University, 639798 Singapore. (E-mail: eccboon@ntu.edu.sg)

H. J. Ng is with IHP GmbH, 15236 Frankfurt (Oder), Germany. (E-mail: herman.j.ng@ieee.org)

D. Kissinger is with the Institute of Electronic Devices and Circuits, Ulm University, 89081 Ulm, Germany.

Y. Wang is with School of Information and Communication Engineering, University of Electronic Science and Technology of China, 611731 China. He was with IHP GmbH, 15236 Frankfurt (Oder), Germany. (E-mail: yongwang@uestc.edu.cn)

X. -L. Tang, Q. Zhang and H. Yu are with Southern University of Science and Technology (SUSTech), 51805 China. (E-mail: yuh3@sustc.edu.cn)

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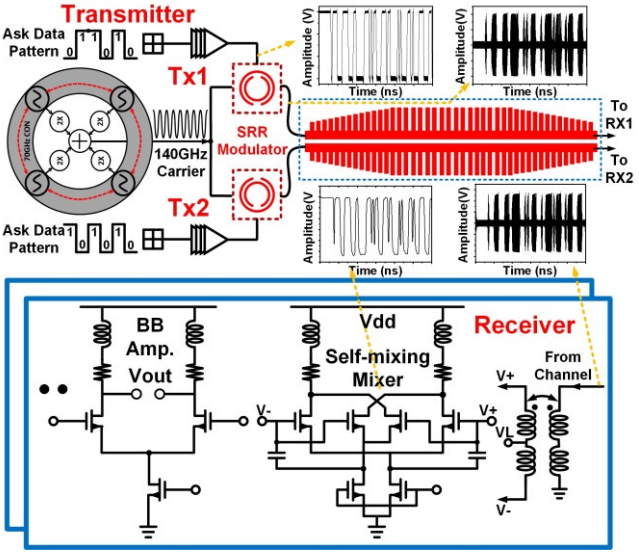

Fig. 1. Dual-channel 140-GHz all-surface-wave I/O transceiver for crosstalk-immune high speed wireline communication [16].

Millimeter wave to terahertz (THz) bands have recently attracted great interest because all components can be implemented in CMOS technology [5]. Known as THz gap, CMOS devices operating close to THz region suffers from huge transmission loss. The main loss of electromagnetic signal is from radiation loss in presence of skin/proximity effects. Moreover, CMOS back-end-of-line (BEOL) is normally narrow and thin, resulting in high loss with crosstalk. Conventional inductive resonators such as inductor [5]–[7] or transmission line (T-line) [8]–[11] are either low-*Q* or bulky for on-chip modulation or oscillation. The low-*Q* of inductive components also limits the achievable extinction ratio (ER) for effective on/off switching [6], [9]. With significant capacitive loading, modulation by switching power amplifier consumes large silicon area with low modulation speed [7]. Additionally, as existing CMOS transistor has low power gain at D-band, single oscillators are difficult to generate strong output power for low bit error rate (BER) communication. Power combining techniques by λ/2 T-line has high loss and low power density in millimeter wave frequencies [12], [13].

To address above challenges, the metamaterial based I/O transceiver has been recently proposed in D-band toward low crosstalk, low power yet high speed communication [14]–[16]. As conceptualized in Fig. 1, the on-chip modulator and signal source are the two critical components for efficient on-off

keying (OOK) communication. The concept and the behavior of the modulator will be proposed and analyzed for the first time to achieve 40 dB ER in D-band. Compared to current arts, the proposed modulator achieves the highest ER using the smallest area without power consumption. Moreover, the *slow-wave* T-line is proposed and modelled to synchronize all oscillator unit-cell toward the highest power density in silicon. The model lies on the fact that the slow-wave characteristic can be well described by a group of distributed lossy T-line model. Based on the new model, design methodologies including in-phase power combining and phase noise reduction are addressed.

The SRR-based source and modulator are designed and analyzed based on the stacked split-ring resonator (SRR) reported in previous literature [17]. By suppressing electric dipole with field enhancement on magnetic flux, the stacked SRR attenuates the metallic surface current. The current crowding effect is hereby minimized, and the resonance frequency and quality factor are primarily manipulated by auxiliary SRR cells. Based on these merits, the passive modulator is evolved from the stacked SRR where the inner rings of the auxiliary SRRs are modulated by high speed data through MOS switches. The transition between stop-band and pass-band by on/off switching is only 20 ps because of the drastic drift of resonance frequency. This leads to a significant improvement on ER without power consumption. The D-band signal source is implemented using a novel slow-wave SRR resonator. An array of metallic grooves perpendicular to the current direction are drilled onto SRR lanes. The field confined slow-wave is thereby excited throughout the stacked SRR. The dispersion curve of such a slow-wave T-line is bending away from the light line, freezing the free electrons into the periodic grooves. This leads to a higher quality factor with reduced physical length for in-phase power combining. To attain high output power, four oscillator unit-cell are magnetically synchronized through the slow-wave T-line, forming a novel coupled oscillator network (CON).

In light of the previous art [16], this work mainly has the following contributions: 1) the SRR-based modulator is modeled, analyzed and experimentally verified; 2) the slow-wave T-line resonator and coupling network are proposed; 3) the slow-wave SRR resonator is described by a novel distributed model; 4) based on the new model, the in-phase coupling of signal source are realized toward high power density in D-band. This paper is organized as follow. Section II introduces the concept of the proposed stacked SRR, followed by the design of stacked-SRR based modulator. The D-band slow-wave CON is designed and analyzed in Section III. Section IV presents the measurement results with comparisons. This work is summarize in Section V.

II. D-band Stacked-SRR Based Modulator

Negative index magnetic metamaterials attracts increasing attention due to their exceptional EM performances. The split-ring resonator (SRR) is a planar artificial structure to attain switching between resonance and passband at the frequency of interest. In microwave regions, the simultaneously negative value of both ε and μ at the resonance is observed. This leads to the fact that the wave vector k and the vector **E** and **H** establishes a left-handed region, in which the phase and group velocity is anti-parallel. The resulting backward wave radiation occurs at the magnetic resonance. Periodic SRR coupled to planar T-line is a potential approach to realize the modulation by alternating the propagation mode. However, due to the skin/proximity effects commonly observed in CMOS metals, the planar SRR is bulky and lossy for on-chip modulation.

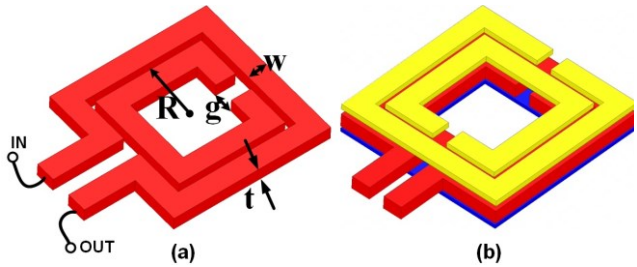

Fig. 2. (a) SRR unit-cell realized by only one metal layer, and (b) proposed stacked SRR structure.

A. Stacked SRR sizing in D-band

Radiation loss is one of the primary concerns in THz metamaterial. Owing to the cross-polarization effect, both electric and magnetic fields are excited inside the SRR loops [17]–[20]. To attenuate the radiation loss of single SRR [17], the surface residue currents generated by electric dipole must be suppressed. To achieve this, one additional SRR (or the inner ring) is placed opposite to the existing SRR to form a SRR unit-cell, as shown in Fig. 2(a). However, as the inner ring is now magnetically coupled to the outer ring, the surface residue current is generated in the inner loop coupled with current crowding effect, converting EM energy into heat. This can be addressed in a compact area by stacking two more SRR unit-cell in a vertical fashion, each orientating opposite to the main SRR unit-cell (or the host-SRR), as illustrated in Fig. 2(b). The top-most auxiliary SRR (yellow) is realized by Aluminum with metal thickness of 1.325 μm, while the host-SRR (red) and the bottom auxiliary SRR (blue) are both implemented by Copper with metal thickness of 3.3 μm and 0.9 μm, respectively. Note that the outer ring of the host-SRR (red) also serves as the host T-line to excite all auxiliary SRRs. As the surface current flows in the opposite direction at each SRR, the excited electric field (*E*-field) will mutually cancel each other, whereas the magnetic field is enhanced.

To validate the above observations, the simulated surface current intensity of the top-most SRR unit-cell is illustrated in Fig. 3(a) using the commercial EM software HFSS. The strength scales from red to blue. Though the current tends to crowd toward the metal surface, the magnitude of the surface current has been clearly suppressed. The result is the reduction of both radiation loss and high frequency resistive loss. The *E*-field distribution of the SRR plane is illustrated in Fig. 3(b). Obviously, the *E*-field is strongly established inside the ring slit. Therefore, by manipulating the ring slit, it is possible to effectively modulate the magnetic resonance frequency (MRF) of the stacked SRR.

Once the SRRs are vertically interleaved, the strength of magnetic resonance and the dispersion relation will be manipulated by the auxiliary SRR ring slit. The resonance frequency of the SRR can be expressed by $f_0 = 1/2\pi\sqrt{LC}$, where

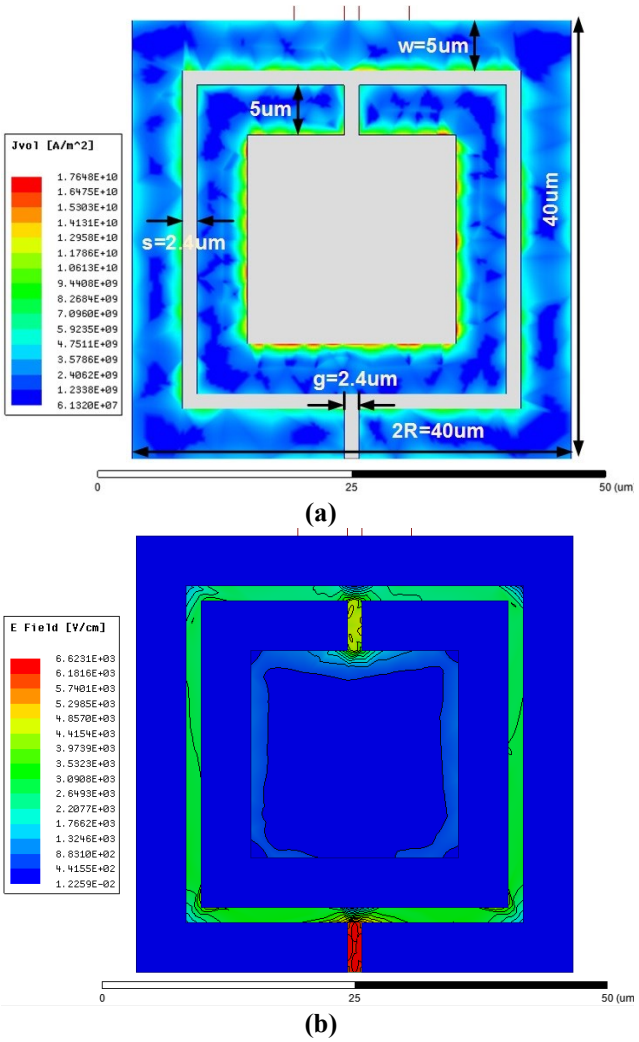

Fig. 3. EM Simulated (a) surface current distribution, and (b) *E*-field distribution of the top-layer auxiliary SRR, at 140 GHz.

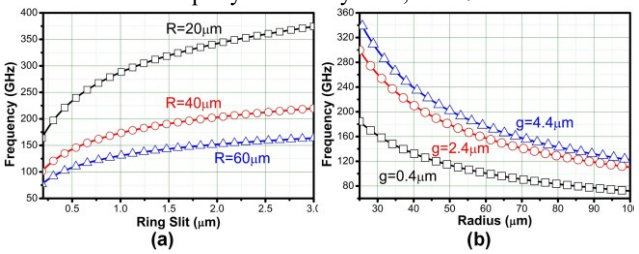

Fig. 4. Analytical magnetic resonance frequency (GHz) of the single-layer SRR related to the ring slit size (*g*) and ring radius (*R*).

L is the rectangle inductance of the loop and *C* is the equivalent capacitance looking into the SRR:

$$C = \varepsilon_0 \left[\frac{wt}{g} + \frac{2t}{\pi} \ln\left(\frac{4R}{g}\right) + \frac{2\pi t}{\ln(2.4t/w)} \right] \quad (1)$$

Here, *w* is the SRR metallic lane width, *R* is the radius, *t* is the metal thickness, and *g* is the ring slit size. The dependency of resonance frequency on the ring slit *g* and *R* are plotted in Fig. 4, where $t = 3.3$ μm and $w = 5$ μm. It is evident that when *R* is small, a small variation of ring slit *g* from 3 μm to 0.2 μm leads to significant reduction of MRF from 310 GHz to 100 GHz or below, whereas *R* has a minor impact on the MRF. This

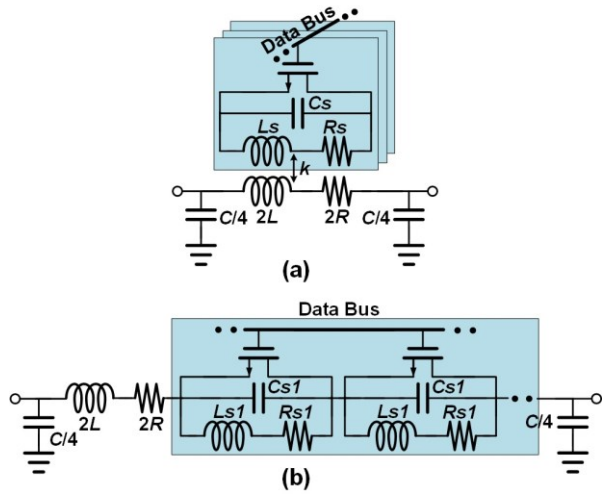

Fig. 5. (a) Equivalent *RLC* circuit of the stacked SRR, and (b) simplified version of (a).

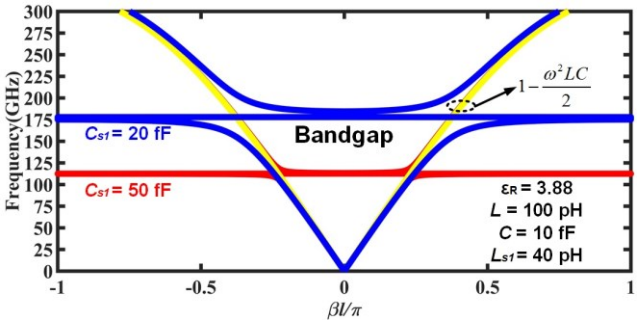

Fig. 6. Analytical dispersion curve and magnetic resonance frequency (MRF) of the proposed SRR as a function of C_s.

is because frequency tuning by *R* primarily relies on the variation of inductance. This result reveals that the stacked SRR can be sized to be very compact to attain desirable resonance frequency, whereas traditional resonators (such as inductor or T-line) are bulky and difficult to tune. Based on this concept, modulation of high-*Q* stacked SRR can be realized by manipulating the ring slit of SRRs.

To boost the quality factor of SRR resonance, the inner ring should be closely coupled to the outer ring (i.e. the host T-line) [20]. The ring gap is thereby chosen as $s = 1.5$ μm complied with the minimum design rule. Note that the metallic width of the host T-line is chosen as $w = 5$ μm to match the 50 Ω impedance of external transmission lines connected to the SRR, thus avoiding additional impedance transformation and loss.

B. Stacked SRR based modulation

The behavior of the periodically arranged SRRs can be better described by lumped element equivalent circuit [19]. Based on the model, the equivalent circuit of the proposed stacked-SRR based modulator is conceptually illustrated in Fig. 5(a), where *N* stages auxiliary SRRs unit-cell are magnetically coupled to the host SRR, each having a MOS switch to govern their states. Since all the auxiliary SRRs are excited by one host T-line, Fig. 5(a) can be simplified to Fig. 5(b), where each auxiliary SRR forms a *RLC* resonance network on the signal propagation path. The *ABCD* matrix is given by (2), where parameter *L*, *C* and *R* is the host T-line inductance, capacitance and resistance, respectively; L_{s1} is the auxiliary SRR loop inductance; C_{s1}

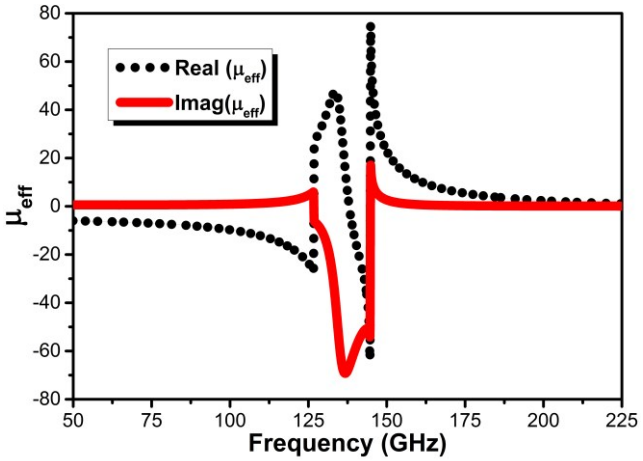

Fig. 7. Extracted permeability μ of the on-chip stacked SRR.

contains the parasitic capacitance of switches and the SRR intrinsic loop capacitances C_s, and R_{s1} represents the loss of auxiliary SRR loops. Note that both C_s and R_{s1} could be minimized by suppressing the SRR loop surface current. For simplicity, assume the network is lossless, i.e., $R = R_{s1} = 0$, and each auxiliary SRR is identical, the serial impedance of the modulator is obtained as follows:

$$Z_{IN} = \frac{4\left[4\left(\omega_0^2-\omega^2\right)-2LC\omega^2\left(\omega_0^2-\omega^2\right)-N\omega^2CL_{s1}\omega_0^2\right]}{j\omega C\left[8\left(\omega_0^2-\omega^2\right)-2LC\omega^2\left(\omega_0^2-\omega^2\right)-N\omega^2CL_{s1}\omega_0^2\right]} \quad (3)$$

where $\omega_0 = 1/\sqrt{L_{s1}C_{s1}}$ is the resonance frequency of the auxiliary SRRs. At the resonance $\omega = \omega_0$, Z_{IN} becomes purely capacitive. The signal is thus prohibited from propagation due to the open circuit established by the resonance of L_{s1} and C_{s1}.

By taking the Euler's formula, when N ($N \geq 1$) stages auxiliary SRRs unit-cell are stacked, the dispersion relation is given by

$$\cosh(\beta l) = 1+\frac{j\omega RC-\omega^2LC}{2}+N\frac{C/C_1+j\frac{R_{s1}C\omega_0^2}{\omega}}{4(1-\frac{\omega_0^2}{\omega^2}-j\frac{R_{s1}C\omega_0^2}{\omega})} \quad (4)$$

The ω–β relation is plotted in Fig. 6, where β is the propagation constant for Bloch waves and l is the period of the structure. Parameters L and C can be extracted from the host T-line $RLGC$ model. Clearly, a frequency gap around the resonance frequency f_0 of the rings is observed. The result is a stopband around f_0 with a level of rejection that depends on C_{s1}. For example, with C_{s1} = 50 fF, the bandgap is narrow with strong rejection. By tuning C_{s1} from 50 fF to 20 fF (the blue

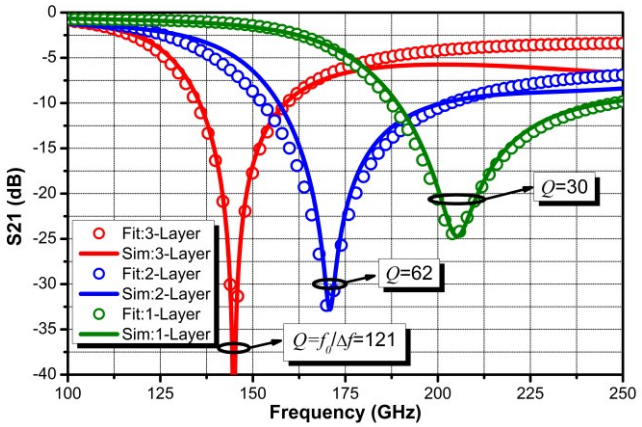

Fig. 8. Comparison of the simulated and calculated transmission S_{21} of the single and stacked SRR structure.

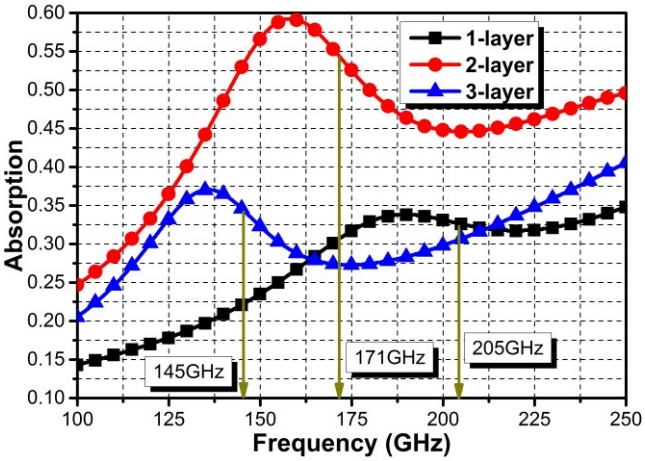

Fig. 9. Simulated absorption loss of single and stacked SRR.

line), the MRF shifts from 113 GHz to 176 GHz, demonstrating the effective frequency tuning capability. To attain a larger C_{s1}, the ring slit g should be reduced. Moreover, when the switches are turned on, all auxiliary SRRs are shorted along the signal path. The result hereby mimics the T-line dispersion relation following $\cos(\beta l) = 1 - \omega^2 LC/2$. This study reveals a drastic transition of the stacked SRR from a magnetic metamaterial to a T-line simply by manipulating the states of the auxiliary SRRs. In addition, multiple stages of auxiliary SRRs is preferred for strong rejection at the resonance.

C. *Stacked SRR optimization*

Among the numerous artificial metamaterial resonators, the vertical stack is a preferred fashion for minimizing IC footprint. The negative μ_{eff} extracted from the simulated S-parameters is illustrated in Fig. 7, confirming its metamaterial property. In a

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1+\frac{j\omega RC-\omega^2LC}{2}+N\frac{C/C_1+j\frac{R_{s1}C\omega_0^2}{\omega}}{4(1-\frac{\omega_0^2}{\omega^2}-j\frac{R_{s1}C\omega_0^2}{\omega})} & \frac{1}{j\omega C} \\ j\omega C\left[2+\frac{j\omega RC-\omega^2LC}{2}+N\frac{C/C_1+j\frac{R_{s1}C\omega_0^2}{\omega}}{4(1-\frac{\omega_0^2}{\omega^2}-j\frac{R_{s1}C\omega_0^2}{\omega})}\right] & 1+\frac{j\omega RC-\omega^2LC}{2}+N\frac{C/C_1+j\frac{R_{s1}C\omega_0^2}{\omega}}{4(1-\frac{\omega_0^2}{\omega^2}-j\frac{R_{s1}C\omega_0^2}{\omega})} \end{bmatrix} \quad (2)$$

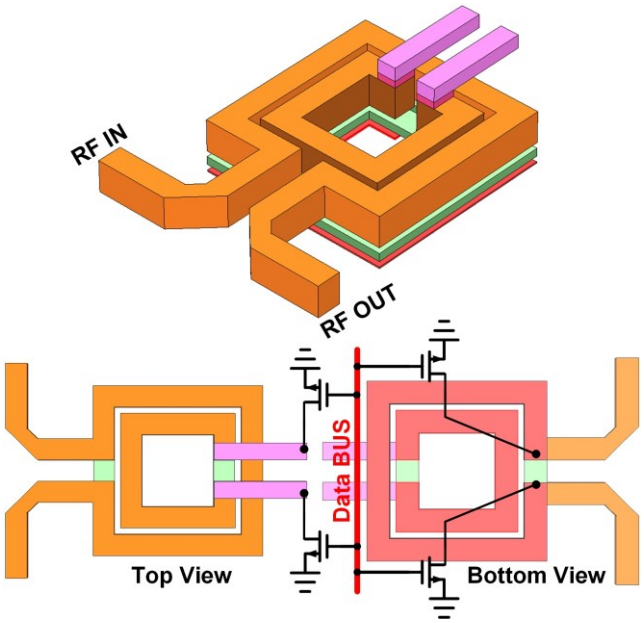

Fig. 10. Illustration of the proposed stacked-SRR based modulator and the configuration of MOS switches.

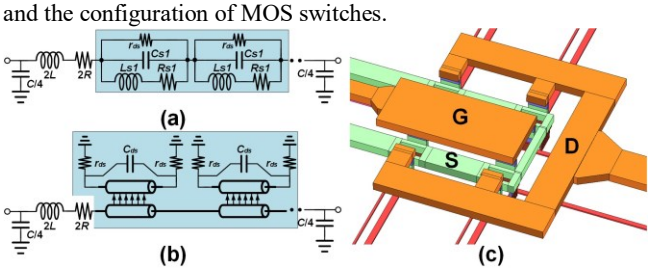

Fig. 11. (a) Equivalent circuit of the modulator at off-state, (b) equivalent circuit of the modulator at on-state, and (c) layout parasitics of the MOSFET switches.

small region near the resonance frequency, the stacked SRR evolves to a non-transmission medium ($\varepsilon \cdot \mu < 0$), leading to a strong negative reflection. A sharp stopband region is thereby established (shown later), and the resonance will be governed by the magnetic dipole which has a lower high-frequency loss than the electric dipole. This is because electric dipole introduces radiation loss and high frequency resistive loss in high frequency for on-chip thin film metals. Traditional on-chip resonant devices such as T-lines or inductors are difficult to generate such a sharp stopband due to the low-Q of resonance.

Both the simulated and calculated transmission coefficient (S_{21}) are depicted in Fig. 8. The analytical results are in good agreement with the simulated ones in a wideband. When three layer SRRs are stacked on-chip, the rejection is strong, leading to the highest quality factor ($Q = f_0/\Delta f_{3dB}$), at the price of the reduced MRF. Here, Δf_{3dB} is defined as the 3-dB bandwidth above the S_{21} dip [21], [22]. The absorption loss are illustrated in Fig. 9. Compared to single SRR unit-cell (Fig. 2(a), $N = 0$), the stacked SRR structure ($N = 1$) may introduce additional absorption loss around the respective MRF. However, by stacking one more auxiliary SRRs unit-cell ($N = 2$) on the top, the surface residue current is further attenuated, reducing the absorption loss around the resonance frequency.

The E-field localization inside the ring slit potentially allows for adding diode or varactor directly onto the opening for modulation. With parasitics capacitance loaded, the result is the

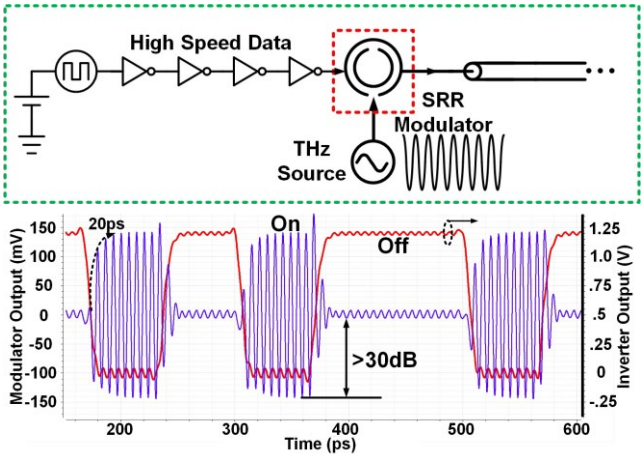

Fig. 12. Transient simulation result of the proposed modulator.

further reduction of MRF. Moreover, CMOS BEOL only provides three or less thick layer metals for low loss routing. Note that the metal resistive loss is another source to decrease the resonance quality. Further stacking auxiliary SRR realized by thin film metal will introduces additional resistive loss with capacitive parasitics. As such, $N = 2$ is adopted in our design toward modulation in D-band.

D. Implementation of on-chip stacked SRR based modulator

Based on the merit of the stacked SRR, one high-Q modulator is proposed in Fig. 10. The proposed modulator are constructed using the top-most three Copper metals with one Aluminum layer. Four NMOS switches are incorporated into the bottom and up auxiliary SRRs to tune the MRF of modulator.

The equivalent circuits of the proposed modulator at off-state is illustrated in Fig. 11(a). The MOS switches are now turned off, and the transistor channel resistance r_{ds} is in parallel with the parasitic capacitance C_{ds} (included in C_{s1}). Note that the modulator has been degenerated to a resonator. Here, r_{ds} is more than 1000 times larger than the metal resistive loss, and C_{ds} will only affect the modulator resonance frequency as implied by the dispersion diagram shown in Fig. 6.

In the on-state, the MOS switches are turned on, and the switches tend to short the inner ring of modulator to the ground. Here, for the signal propagation the equivalent circuit is shown in Fig. 11(b). Now the modulator degenerates to a planar T-line coupled to a short stub together with a parallel parasitic capacitance C_{ds}. To suppress the loss due to the short stub, r_{ds} should be reduced. However, as r_{ds} is not on the wave propagation path, its impact on insertion loss is minimized.

Each switch has the size of 20×1 μm/65 nm considering the resonance frequency and insertion loss. Meanwhile, it is important to accurately extract the parasitics of MOS transistors in high frequencies, as the existing RF transistor model is valid up to the bottom metal M1 only. Shown in Fig. 11(c), both the vias and interconnects (from M2 to top) are merged in layout such that their mutual coupling can be captured by the EM simulator. To further reduce the metal resistive loss along the data path, both gate and drain are routed by the thickest copper metal. The source is enclosed by a ground plane so as to minimize the parasitic inductance and resistance. Using large switches, the resonance frequency varies by around ±2.7%

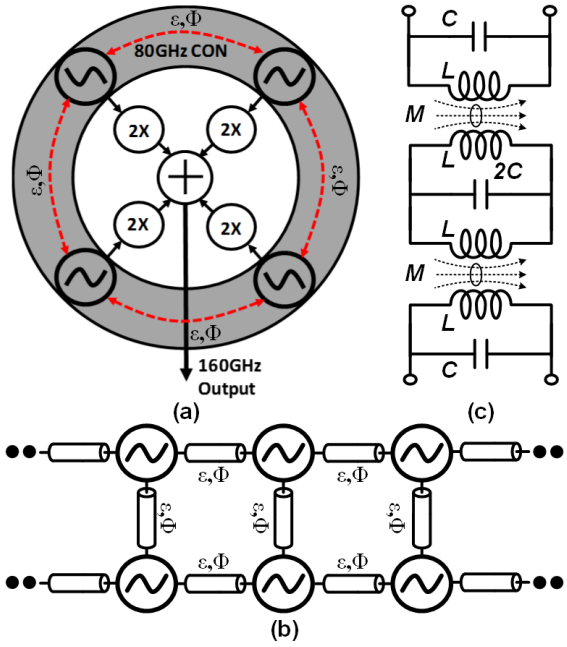

Fig. 13. (a) Closed-loop 4-way power combined coupled oscillator network (CON); CON realized via (b) distributed T-line coupled [23], [25]–[28], and (c) magnetically coupled by transformer [24].

under PVT, and the on/off ratio is better than 30 dB for all corners. A wide tuning range signal source is thus necessary to cover the frequency variations.

Fig. 12 illustrates the simulated transient result of the proposed SRR modulator. To drive the modulator in high speed, the inverter size should be increasingly scaled. With 0-dBm output power from the signal source, the simulated transition time is about 20 ps with around 30 dB on/off ratio. However, the active modulator realized by switching power amplifier requires over 50 ps for state transition [7]. Note that the large size of the inverter buffer may degrade the on/off ratio of modulator.

III. SRR-BASED COUPLED OSCILLATOR NETWORK

A. On-chip D-band signal source

Although the continuous scaling of CMOS transistors contributes to the improvement of f_{max}, the inductive resonators realized by top-layer metal have large radiation loss and low-Q [8], [23]–[27]. As such, it is challenging to design a signal source to obtain large output power, high efficiency (DC-to-RF power ratio) and high power density in D-band.

B. On-chip coupled oscillator network

To boost the output power, multiple oscillator unit-cell are coherently combined, forming a coupled oscillator network (CON). The harmonic currents can be hereby extracted from the sum of the frequency multiplier output, as illustrated in Fig. 13(a). The closed-loop CON is naturally a self-sustained synchronized system, where each oscillator converges to a certain frequency at the steady state.

On-chip CON is commonly realized as shown in Fig. 13(b), where each oscillator unit-cell is coupled by distributed T-lines [23]. The coherent synchronization requires λ/2 physical length

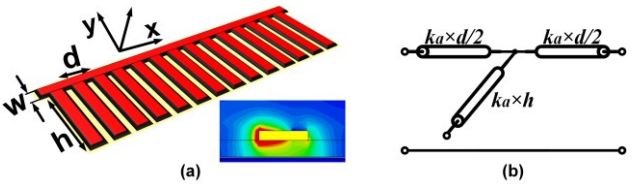

Fig. 14. (a) Illustration of the slow-wave T-line structure, near-field result evaluated at *yz* plane, and (b) T-model of the unit-cell.

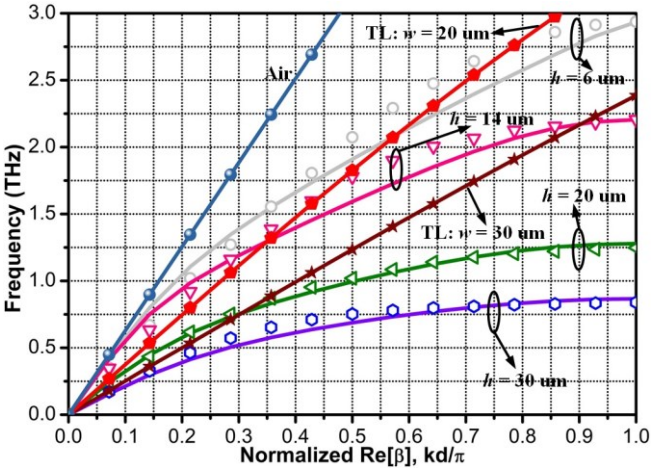

Fig. 15. Comparison of analytical and simulated dispersion curve of the slow-wave T-line up to THz region. (Sim.: solid line, Cal.: dot)

for coupling while λ/4 for resonance which is bulky and lossy for high-Q oscillation. The magnetic coupling by transformer in Fig. 13(c) is another approach to synchronize all oscillator unit-cell in a compact area [24]. However, on-chip transformer suffers from phase/amplitude imbalances, leading to the degraded output power and phase noise. Moreover, on-chip transformer with high transformation ratio is lossy in D-band.

C. D-band slow-wave transmission line

To maintain the phase/amplitude balance while achieve high-Q oscillation, one possible approach is to use the slow-wave T-line. The slow-wave approaches allows for shrinking the size of resonators by increasing the effective dielectric constant, which not only reduces the required area but also boost the Q of resonator [28]. The coupling network can be thereby implemented by the slow-wave T-line as well. The slow-wave T-line is commonly featured by two differential metallic strip on the top metal layer with an array of bottom ribbons orthogonally oriented to the propagation direction. However, the spatial arrangement of the structure suffers from crosstalk to adjacent conductors with radiation loss into the free space.

One slow-wave structure featured by a group of periodic grooves drilled onto the conventional T-line is proposed for on-chip E-field confinement [29], as illustrated in Fig. 14(a). The groove periodic pitch is d. h represents the groove depth. With proper mode conversion for both impedance and momentum matching [30]–[31], the confined mode will be established among the grooves, forming resonances with localization of free electrons by exciting the *surface wave* [29]. The propagation along the x-direction is low loss and low crosstalk because the spatial confinement of E-field exponentially decays along the y-direction, while the H-field maintains its polarization toward the z-direction even for ultra-thin metals.

The detail of field confinement is illustrated in Fig. 14(a) evaluated at the *yz* plane.

To study the slow-wave characteristic of the proposed slow-wave T-line, Fig. 14(b) depicts the unit-cell characterized by two horizontal T-line with length of $d/2$ and one vertical T-line with depth of h. The *ABCD* matrix can be hereby obtained in (5) by multiplying N section of the unit-cell. Here, $\gamma = \alpha + j\beta$ is the propagation constant and c_i is the coefficient of the product form. In a special case of $h = 0$, (5) degenerates to a lossy T-line model. Note that the lumped model developed in [32] may be difficult to describe the distributed behavior of the slow-wave T-line from millimeter-wave to THz region.

According to Floquet theorem, owing to the periodic nature of the structure, the eigenvalue of the transmission matrix must be in the form of $e^{\gamma p}$, where p is the period. As such, the dispersion relation can be derived from (5) as below

$$\cosh(\gamma p) = \cosh(\gamma d) + \frac{\sinh(\gamma d)}{2}\tanh(\gamma h) \tag{6}$$

where k_x is the effective wavenumber along the *x*-direction.

Fig. 15 illustrates the analytical and simulated ω–k relationship. The eigenvalue of the T-section unit-cell is simulated using CST Studio where the metal is treated as perfect electric conductor (PEC). It shows that all the dispersion curves gradually bend away from that of the light line or the planar T-line, and approach their respective cut-off frequencies, exhibiting the slow-wave behavior. The analytical results are well matched to the simulated result for the frequencies below 1.25 THz. The maximum deviation up to 12% is found for h = 6 µm. This is because the resonances between the shunt branches of the open stub become significant as frequency increases, which has been underestimated in the T-section model. In the sense of circuit, the serial inductance and the dispersive capacitance of the open stub resonates similar to the way of resonance of free electrons in the metal and the EM-field established between the grooves at these high frequencies. As such, the simulated ω–k curves are more bending away from the light line. However, (6) is simple yet effective to evaluate the slow-wave dispersion up to THz.

D. Slow-wave oscillator unit-cell

The proposed slow-wave T-line can be used to replace the conventional on-chip T-line for D-band source generation. Recent sub-THz T-line structures are summarized in Table I. By generating the field confined slow-wave, loss reduction is achieved on the lossy substrate (ρ = 10 Ω·cm).

The concept of the slow-wave VCO is depicted in Fig. 16(a), and the equivalent circuit is illustrated in Fig. 16(b). To establish the standing-wave in the slow-wave T-line, the negative resistance provided by the NMOS cross-coupled pair must compensate the tank losses. When N-section slow-wave

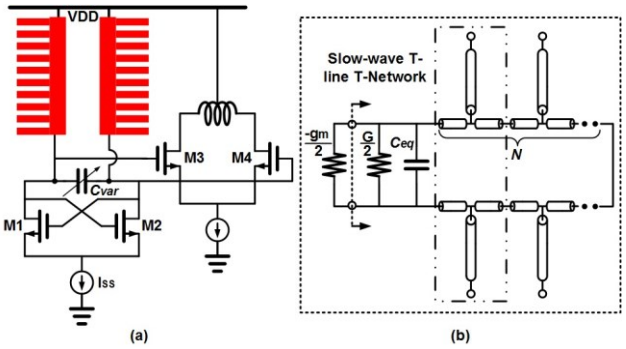

Fig. 16. (a) Slow-wave oscillator unit-cell loaded with distributed slow-wave T-line, and (b) equivalent circuit of (a).

TABLE I
SUB-TERAHERTZ TRANSMISSION LINE PERFORMANCE SUMMARY

Ref.	[33]	[34]	[35]	This work
Freq. (GHz)	220	220	220	220
Excitation Mode	Goubau	Goubau	Quasi-TEM	Slow wave
Substrate Type	α–SiO_2 Z-cut, ε_r=4.5	Glass ε_r=5.5	Si	Si ε_r=11.6
Substrate Loss	tanδ =1.10^{-4}	/*	/	tanδ >4×10^{-3}
Substrate Height (µm)	450	700	325	720
Metal and Thickness	Gold 3 µm	0.5µm	2 µm	Copper 3.3 µm
Width (µm)	60	60	25$^{\overline{T}}$	12.4
Reflection (dB)	<–11	<–12	<–10	<–8
Loss(dB/mm)	4	16.7	4	1

*: A 2-mm-thick absorber has been placed below the sample to push back parasitic ground plane effect.
$^{\overline{T}}$: including the CPW ground plane.

unit-cell (Fig. 14(b)) are cascaded, the total differential tank admittance is given by (7):

$$Y_T = j\omega C_{eq} + \frac{1}{2}\left(G_D - g_m\right) + \frac{\frac{1}{2}\left[\gamma d\tanh(\gamma h)\right]^N + \sum_{i=1}^{N-1} c_i\left[\frac{\gamma d}{2}\tanh(\gamma h)\right]^i + \cosh(\gamma d)}{2\left[\frac{1}{4}(\gamma d)^{N+1}\tanh^N(\gamma h) + \sum_{i=1}^{N-1} c_i\left(\frac{\gamma d}{2}\right)^{i+1}\tanh^i(\gamma h) + \sinh(\gamma d)\right]} Y_0 \tag{7}$$

where g_m is the transconductance of the cross-coupled pair, Y_0 is the characteristic admittance, G_D is primarily determined by the MOS channel conductance and the varactor conductance, and $C_{eq} \approx C_{var} + 0.5(C_{gs} + C_{gd}) + 2C_{buf}$ is the total capacitance seen by the tank.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}^N \approx \begin{bmatrix} \dfrac{2^{N-1}\left[\frac{\gamma d}{2}\tanh(\gamma h)\right]^N + \sum_{i=1}^{N-1} c_i\left[\frac{\gamma d}{2}\tanh(\gamma h)\right]^i + \cosh(\gamma d)}{2^{N-1}\left(\frac{\gamma d}{2}\right)^{N-1}\tanh^N(\gamma h) + \sum_{i=1}^{N-1} c_i\left(\frac{\gamma d}{2}\right)^{i-1}\tanh^i(\gamma h) + \sinh(\gamma d)} & Z_0 \times \left\{2^{N-1}\left(\frac{\gamma d}{2}\right)^{N+1}\tanh^N(\gamma h) + \sum_{i=1}^{N-1} c_i\left(\frac{\gamma d}{2}\right)^{i+1}\tanh^i(\gamma h) + \sinh(\gamma d)\right\} \\ \dfrac{1}{Z_0} & 2^{N-1}\left[\frac{\gamma d}{2}\tanh(\gamma h)\right]^N + \sum_{i=1}^{N-1} c_i\left[\frac{\gamma d}{2}\tanh(\gamma h)\right]^i + \cosh(\gamma d) \end{bmatrix} \tag{5}$$

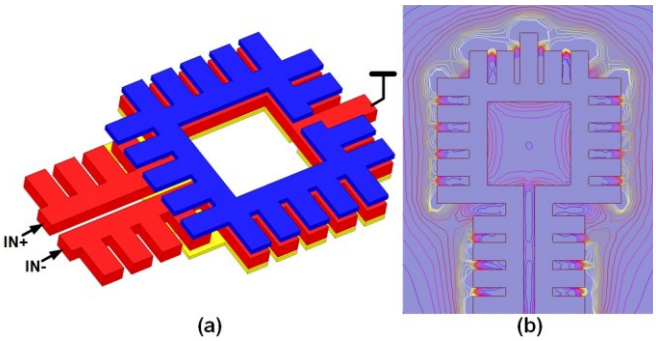

Fig. 17. (a) Slow-wave resonator evolved from the stacked SRR structure, and (b) simulated *E*-field distribution at 120 GHz.

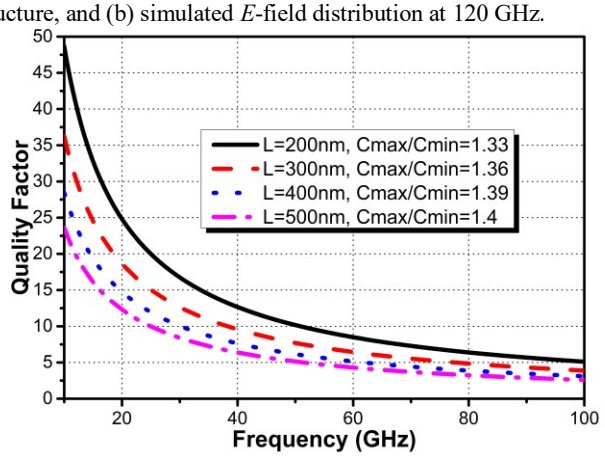

Fig. 18. Simulated quality factor Q_{var} of the varactor.

To further improve the slow-wave oscillation and reduce the metal absorption, a high-Q slow-wave resonator is proposed in Fig. 17(a). The structure evolves from the stacked SRR proposed in Fig. 2(b) where each lane of the SRRs are drilled by the periodic grooves such that the slow wave can be established throughout the structure. The resonator maintains the TM mode excitation while the residue currents are suppressed. As shown in Fig. 17(b), the differential *E*-field line pattern suggests that the confined mode are established and propagates through the resonator at 120 GHz.

E. Frequency tuning

The frequency tuning range (FTR) is commonly determined by the varactor size. However, there exists a trade-off between the varactor quality factor and FTR. Fig. 18 illustrates the varactor quality factor and the capacitance ratio (C_{max}/C_{min}) in terms of varactor channel length L from the post-layout simulation. Clearly, C_{max}/C_{min} improves only 5% by increasing L from 200 nm to 500 nm, but the quality factor drops from 6 to 3 at 80 GHz. Therefore, we choose the minimum channel length of 200 nm to prevent excessive Q degradation with over 1 GHz/V VCO gain. In addition, it is clear that VCO operating at fundamental frequency higher than 100 GHz suffers from poor quality factor due to the varactor.

F. Phase noise of slow-wave CON

Phase noise of the cross-coupled oscillator in Fig. 16(a) depends on the quality factor of resonator, the bias current I, and the transistors sizing. The phase noise at the frequency offset $\Delta\omega$ for a standalone oscillator is given by

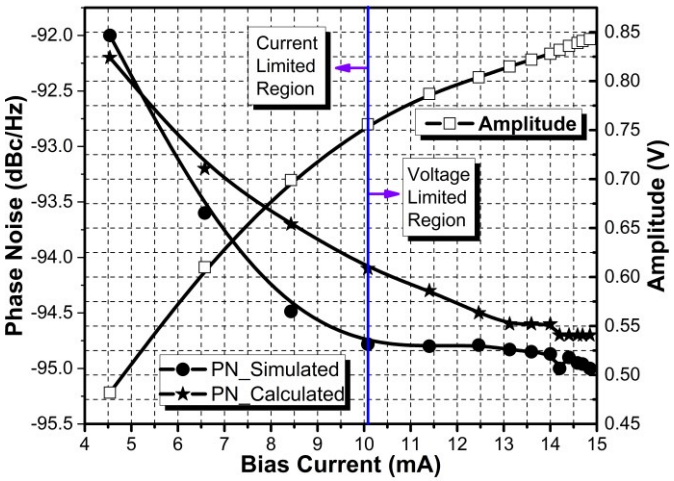

Fig. 19. Harmonic balance simulation results of phase noise and amplitude of the slow-wave oscillator unit-cell at 120 GHz.

$$L\{\Delta\omega\} = \frac{4kTF}{G\left(\frac{1}{2}V_{p-p}\right)^2}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \qquad (8)$$

Where $G = R_P//G_s$ is the parallel conductance seen by the tank, F is the excess noise factor comprising of the tank conductance noise, cross-couple pair noise and the current source noise, and Q is the tank quality factor.

By using the square law of MOS transistor, the maximum output swing can be obtained by $V_{p\text{-}p} = 4\sqrt{2}I_{SS}(R_P//G)/\pi \approx 1.8I_{SS}(R_P//G_s)$. Fig. 19 illustrates the post-layout simulated phase noise and single-ended average amplitude ($V_{p\text{-}p}/2\sqrt{2}$) of the standalone 120-GHz fundamental slow-wave oscillator under 1.2-V bias loaded by the proposed surface-wave resonator. The phase noise at 1-MHz offset decreases quadratically with I_{ss}, but it becomes flat above 10 mA. This is because the excess noise factor F is proportional to I_{ss} as well, and the MOSFET conductance shrinks dramatically when the cross coupled pair enters into voltage limited region. The calculated phase noise is close to the simulation result under $I_{bias} < 10$ mA. As shown in Fig. 19, $V_{p\text{-}p}$ increases almost linearly in the current limited region but starts to saturate at the voltage limited region. To compromise the trade-off between phase noise and power, the cross-coupled pair should be biased at the boundary of each region, indicating $I_{ss} = 10$ mA. The integrated RMS jitter from 10 kHz to 1 GHz is around 0.5 ps.

Apart from power combining, the four-ways coupled oscillator topology shown in Fig. 13(a) potentially generates multi-phase for complex modulation scheme. Thus, the phase perturbation is a particular interest in wireline signaling. It has been proven that the phase perturbation of a standalone oscillator is expressed by $\delta\bar{\theta} = [\delta\theta_1\ \delta\theta_2 \ldots \delta\theta_N]^T$, and the following $N \times N$ matrix represents the injection-locked dynamics of the N-ways power combined CON where each standalone VCO couples only one adjacent VCO at each side [36]:

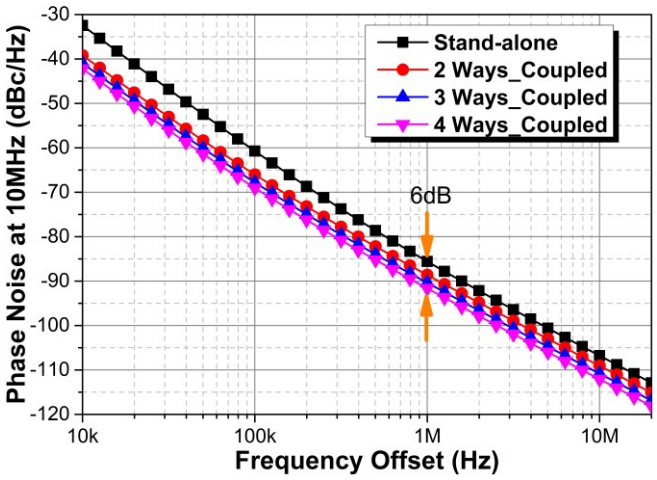

Fig. 20. Simulation phase noise of the proposed slow-wave power-combined CON at 120 GHz.

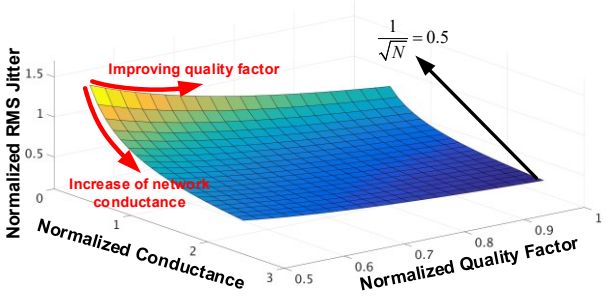

Fig. 21. Analytical RMS jitter of the 4-way slow-wave power-combined CON versus network quality factor Q_L and conductance G_L.

$$N=\begin{bmatrix} -2\varepsilon-j\omega & \varepsilon & 0 & 0 & 0 & \varepsilon \\ \varepsilon & -2\varepsilon-j\omega & . & 0 & . & 0 \\ 0 & \varepsilon & . & . & 0 & . \\ . & 0 & . & . & \varepsilon & 0 \\ 0 & . & 0 & . & -2\varepsilon-j\omega & \varepsilon \\ \varepsilon & 0 & 0 & 0 & \varepsilon & -2\varepsilon-j\omega \end{bmatrix} \tag{9}$$

where $\omega = \Delta\omega/(\omega_0/Q)$, ε is the coupling factor. The noise dynamics is expressed by $\boldsymbol{N}\,\delta\bar{\theta} = \overline{B_n^2}/G_L$ where $\overline{B_n^2}$ is the uncorrelated noise susceptance of each VCO. The phase perturbation of each oscillator unit-cell in the loop is given by:

$$\left|\delta\theta_k\right|^2 = \frac{\overline{B_n^2}}{\omega^2 G_L^2}\sum_{j=1}^{N}\omega^2\left|p_{kj}\right|^2 \tag{10}$$

Here, p_{kj} is the element in the matrix $\mathbf{P} = \mathbf{N}^{-1}$, and the term $\overline{B_n^2}/\omega^2 G_L^2$ is given by (9). Fig. 20 depicts the harmonic balance simulation result of the phase noise for standalone VCO and CON with N from 2 to 4, where the noise improvement is 2.1 dB, 4.8 dB and 6 dB, respectively. Slow wave T-line with groove depth of h = 12 is used for coupling.

The phase perturbation is dependent on the network topology given by (9), network conductance $G_L = G_s + N\times G_c$, and equivalent quality factor $Q_L \approx 2(Q_s//Q_c)$, where G_c is the conductance of the coupling network. The RMS jitter of a 4-way power combined CON can be attained by the phase noise conversion from (11):

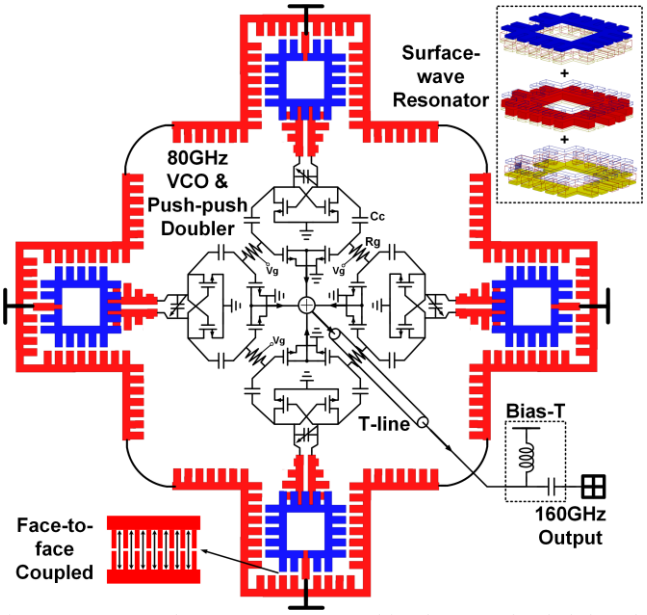

Fig. 22. Proposed 4-way power-combined CON loaded by the proposed slow-wave resonator and slow wave T-line network.

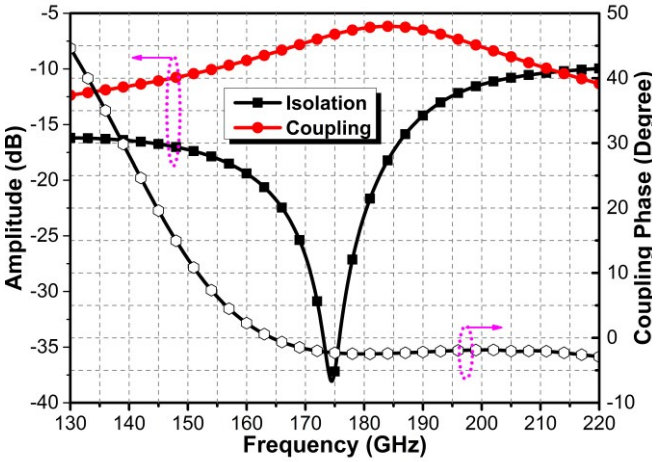

Fig. 23. Simulated coupling factor of the proposed slow-wave T-line coupler and the simulated coupling phase.

$$J_{RMS} = \frac{1}{2\pi f_0}\sqrt{2\int_{f_1}^{f_2} 10^{\frac{L(\omega)}{10}}\,df}\Bigg|_{\omega=\Delta f/(\omega_0/Q_L)} = \frac{1}{2\pi f_0}\sqrt{2\int_{f_1}^{f_2}\frac{\omega^8+32\varepsilon^2\omega^6+360\varepsilon^4\omega^4+1216\varepsilon^6\omega^2+1024\varepsilon^8}{\left(\omega^4+20\varepsilon^2\omega^2+64\varepsilon^4\right)^2}\left(\frac{\overline{B_n^2}}{\omega^2 G_L^2}\right)df} \tag{11}$$

where the integration interval is from 1 kHz to 1 GHz, and ε has been set to 0.4. The dependence of J_{RMS} on Q_L and G_L is illustrated in Fig. 21. Note that J_{RMS} has been normalized to a standalone surface-wave oscillator with Q = 40. The center frequency is 120 GHz. Clearly, when the normalized Q_L increases higher than 0.5, the normalized J_{RMS} drops below unity rapidly. Meanwhile, J_{RMS} decrease linearly with the increase of loaded quality factor Q_L. In addition, it is obvious that the loaded conductance has a stronger impact on J_{RMS}

against the loaded quality factor. By using the deep groove slow-wave T-line, the noise susceptance is reduced due to a larger G_L. In the frequency range away from the cut-off frequency, with deeper the groove, a higher Q_c is obtained to improve Q_L. Note that a larger G_L in the conventional T-line coupling network is obtained by widening the line width, which increases the shunt loss to the substrate and thereby degrades the Q_L. As such, compared to a single oscillator unit-cell, the power combined slow-wave CON reduces the phase noise and jitter.

G. Output power of CON

High output power is hard to achieved by increasing the size of oscillator core devices in D-band due to the following reasons: 1) the increase of parasitics reduces the quality factor and self-resonance frequency of resonator; 2) To maintain the same oscillation frequency, the voltage swing of the cross-coupled pair drops due to the smaller inductance used; 3) increasing the size of push-push frequency doubler further exacerbates 1) and 2).

When multiple oscillators are synchronized in a closed loop for power combining, the resulting synchronized output voltage after frequency multiplication can be expressed as below under the small perturbation condition:

$$V(t) = A\sum_{j=1}^{N}\cos(2\omega_0 t + \delta\theta_j + \delta\theta_D) \approx NA\cos(2\omega_0 t + \frac{1}{N}\sum_{j=1}^{N}\delta\theta_j + \delta\theta_D) \quad (12)$$

where $\delta\theta_j$ is the random noise of each oscillator unit-cell, and $\delta\theta_D$ is the total noise contribution from the frequency doubler. Therefore, to achieve high output power, the integral phase perturbation throughout the coupling network must be minimized, which can be realized by the proposed slow-wave high-Q CON topology.

H. Implementation of slow-wave CON

The proposed 4-way power combined CON is designed centered at 160 GHz as depicted in Fig. 22, where each 80-GHz fundamental cross-coupled VCO is loaded by the proposed slow-wave resonator in Fig. 17(a). The size of the core device is 12 µm/60 nm.

To synchronize all oscillator unit-cell in the loop, the resonator core is further coupled to the external slow-wave T-line by a face-to-face arrangement [15]. Once the slow-wave is excited, the field enhancement maintains among the grooves. Moreover, the phase shift and network conductance can be manipulated by the groove depth h. With transistor loadings considered, the simulated results in Fig. 23 show that the coupling loss is 6.2 dB with over 20 dB isolation around 160 GHz, and a zero-phase (or in-phase) shift is achieved for in-phase power combining. The in-phase directional coupling network also ensures the CON to be synchronized to reject residue oscillation modes. Besides, the directional coupling establishes the one directional flow in the loop, satisfying the assumption of (9).

Note that only the host SRR is coupled to the external slow-wave T-line for closed loop injection locking. This is because the magnetic resonance quality is mainly determined by the auxiliary SRRs. As such, each oscillator unit-cell will be

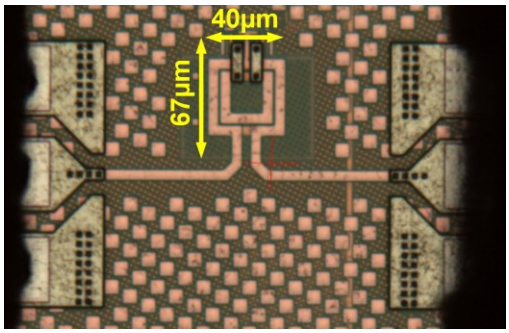

Fig. 24. Die photo of the proposed on-chip D-band modulator.

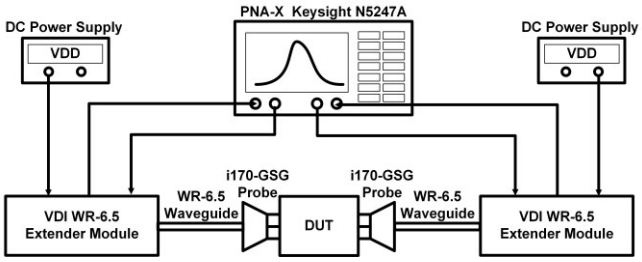

Fig. 25. D-band (110–170 GHz) S-parameter measurement setup.

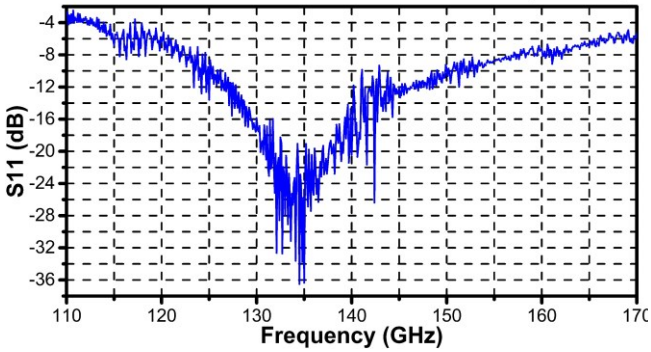

Fig. 26. Measured reflection coefficient S_{11} at the on-state.

magnetically coupled in TM mode through the slow-wave T-lines. This topology also minimizes the frequency drops arisen from the coupling network. As the Q of interconnects are much smaller than the magnetic resonator, directly paralleling the coupling network degrades Q_L significantly. Moreover, the layout of CON is fully symmetrical.

As the VCO output swing $V_0 \propto I_{SS}Q\omega_0 L$, boosting Q also improves the output swing, and the push-push frequency doubler experiences more abrupt on/off switching. The size of the doubler is chosen as 2×14 µm/60 nm, a compromised result balancing the output power and the tank resonance frequency. The layout of VCO core should be symmetrical to ensure phase/amplitude balance for maximum 2nd harmonic extraction at the doubler output. The AC-coupled capacitor C_c isolates the doubler from the cross coupled pair, and the doubler can be DC-biased via resistor R_b near the subthreshold region in which the second harmonic is rich. The strong 2nd harmonics current is extracted and combined at the CON geometrical center, which is further guided by a T-line to the output for impedance matching and testing. All transistor layouts are considered in EM simulation similar to Fig. 11(c). The simulated output power under PVT is from 3.7 to 6.2 dBm using the same voltage bias, and the oscillation frequency drifts by about ±2%.

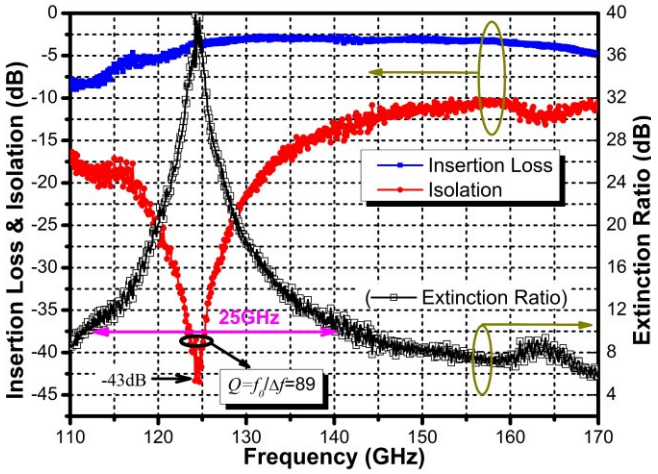

Fig. 27. Measured insertion loss, isolation, extinction ratio and quality factor of the proposed D-band modulator.

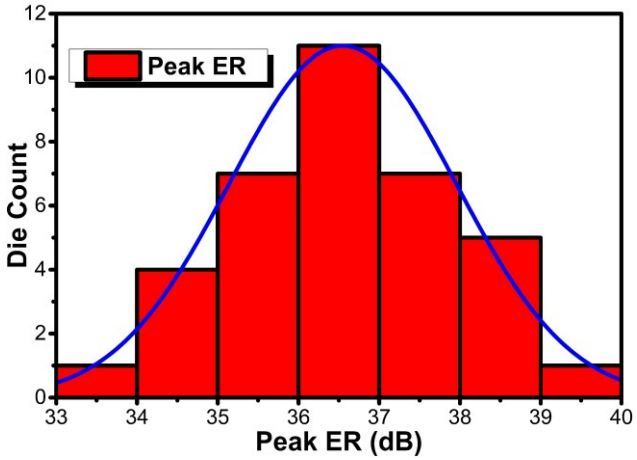

Fig. 28. Statistical distribution of the measured extinction ratio.

IV. Measurement Results

The proposed stacked SRR modulator and slow-wave CON were fabricated in a standard 65-nm CMOS process. The prototypes are measured on CASCADE Microtech Elite-300 probe station and Agilent PNA-X with the VDI providing the signal source. The RF PAD has been calibrated during the measurement [30].

A. D-band stacked SRR modulator

Fig. 24 shows the modulator die photo and the testing setup is illustrated in Fig. 25. The occupied area is only 40 µm × 67 µm. To prevent degrading the Q-factor, the substrate under the device is the intrinsic silicon region without P+ implant, and the dummy-fill is prohibited within the structure. S-parameters calibration is done before probing the DUT. Fig. 26 shows the measured reflection coefficient S_{11}, which is smaller than –10 dB from 125–150 GHz. As demonstrated in Fig. 27, a strong resonance is observed at 125 GHz. The measured insertion loss and isolation at 125 GHz is 3 dB and 43 dB, respectively, implying a peak 40 dB ER. The resulting Q-factor can be evaluated by $Q = f_0/\Delta f_{3dB} = 89$. For signal integrity, the ER should be higher than 13 dB for low BER OOK communication [37], and the measured modulator bandwidth is 25 GHz for this

TABLE II
D-band Modulator Performance Summary

Ref.	[6]	[8]	[9]	[10]	[11]	**This work**
Type	Passi.	Passi.	Passi.	Passi.	Acti.	**Passi.**
Freq. (GHz)	135	110	144	60	120	**125**
Reflection(dB)	–16.3	<–15	–8.7	/	/	**<–30**
Loss (dB)	4.3	3–4	<3.6	6.6	0.1*	**3**
Isolation (dB)	12.5	25	>19.5	33.2	18.1	**43**
ER (dB)	8.2	22	17.4	26.6	18.2	**40**
BW(GHz)	20	50	60	/	>10	**25**
Power (mW)	/	/	0	0	28	**0**
Area (mm²)	0.21	0.3	0.013	0.18	0.11	**0.002**
CMOS Process	0.13µm	90nm	65nm	90nm	45nm	**65nm**

*: Gain.

requirement. The high insertion loss at the frequency below 120 GHz could be due to the reflection as observed in Fig. 26.

To verify the robustness, the statistics of ER is collected by measuring 36 dies. Shown in Fig. 28, the worst case is 33.4 dB, while the dominant case ranges from 35 dB to 38 dB. Note that the random probing loss and calibration also fluctuates the collected data. The design consumes no static power. State-of-the-art on-chip modulator performances are summarized and compared in Table II. Clearly, the proposed modulator achieves the best isolation and ER at D-band. Besides, the occupied area is at least 50 times smaller than state-of-the-art [6]–[11]. The obtained high on/off ratio is attributed to the SRR metamaterial property of high-Q resonance. In contrast, two inductively coupled resonators, such as transformers operating at their resonance frequencies, are difficult to generate large on/off ratio at D-band due to the low-Q of resonance.

B. 160 GHz on-chip slow-wave CON

Fig. 29 (a) shows the 4-way combined CON die photo with active area of 0.053 mm². The measurement setup is shown in Fig. 29(b). The proposed CON design burns 67 mW from a 1.2-V power supply. To maximize the output power, the tail current source has been omitted. However, it has be included in the I/O link design [16] to optimize the power efficiency of the transceivers.

Fig. 30 illustrates the measured spectrum of the signal source at 159.12 GHz. After calibration of losses from waveguide, connector and IF cable, the measured output power is 5.7 dBm. The reflection is illustrated in Fig. 31, implying –15 dB and below reflection loss in a wideband. Therefore, the peak power is 3.7 mW, leading to the DC-to-RF efficiency of 5.5%.

Due to the limitation of instruments, the phase noise cannot be directly measured. Instead, we measure the phase noise through the spectrum in Fig. 30 by using the equation below:

$$PN = P_{Carrier} - P_{Noise@10MHz} - 10log(RBW) \qquad (13)$$

With the resolution bandwidth (3-MHz) known, the measured phase noise at 10-MHz offset is around –105 dBc/Hz. Note that the result is 7 dB worse than the post-layout simulation result shown in Fig. 20. This is expected because the tank quality factor could be degraded by the surrounding metal dummy fill or inaccurate full-wave EM modelling. High frequency

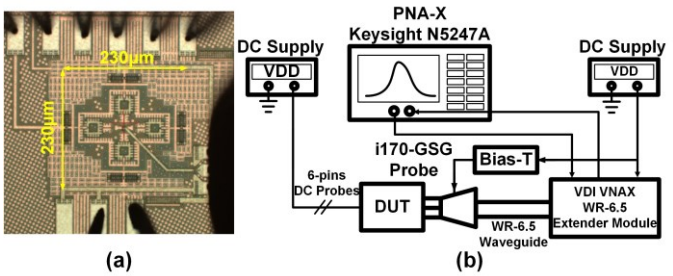

Fig. 29. (a) CON Die photo, and (b) D-band measurement setup.

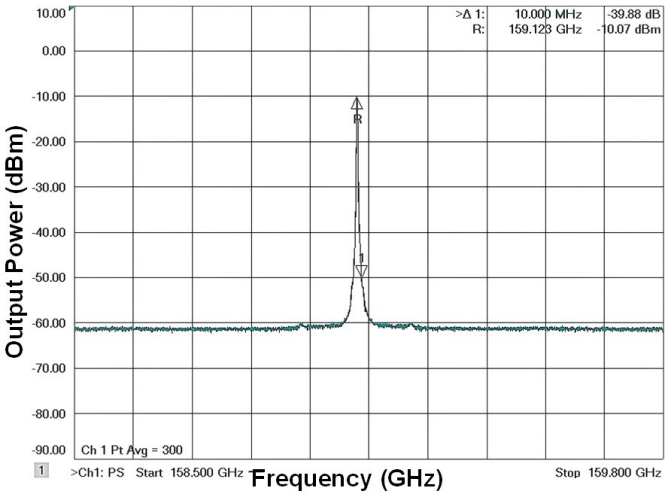

Fig. 30. Measured output spectrum at 159.12 GHz.

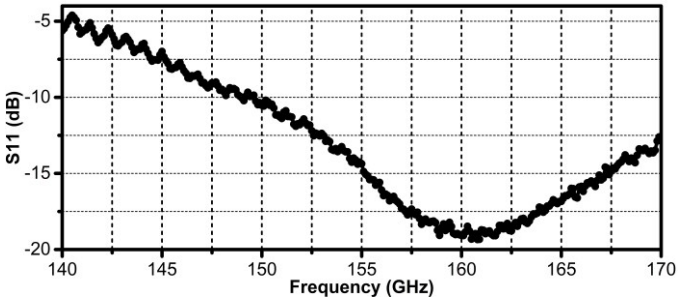

Fig 31. Measured output reflection coefficient S_{22} of CON.

modelling of noise in RF-MOSFET is difficult as well. In addition, supply noise, harmonic mixer noise, spectrum analyzer oscillator noise and acquisition time all contributes to the distortion of the measured spectrum.

The phase noise under different supply voltage is summarized in Fig. 32. Below 0.7-V supply no oscillation occurs. Above 0.7-V the phase noise improves almost linearly with supply voltage. This is due to the increase of the current sunk by the cross-coupled pair, and the output swing grows proportionally, as predicted by (8). The best measured phase noise is -106 dBc/Hz at V_{DD} = 1.35 V. However, by further increasing the supply the phase noise degrades, because the cross-coupled pair potentially operates into the junction breakdown region. The deep N-well MOSFET may be considered to achieve both high power and low phase noise by increasing the supply voltage, and it inherently suppresses the substrate coupling as well. The measured phase noise in relation to the VCO control voltage V_{ctrl} is summarized in Fig. 33.

Note that at millimeter-wave frequencies or above, the Q of varactor decreases significantly, and thus dominates the tank

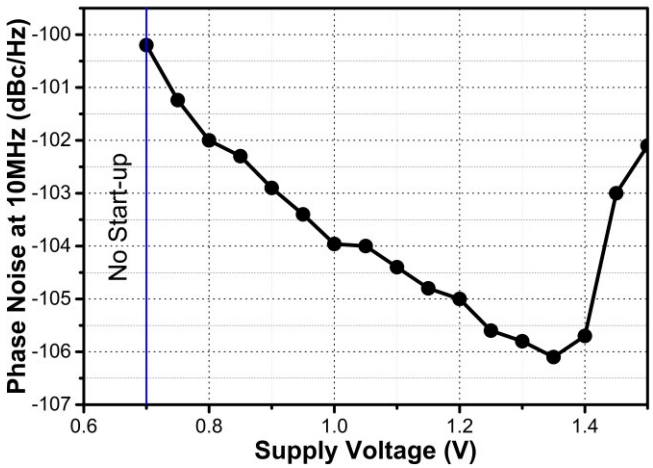

Fig 32. Measured CON phase noise at 10-MHz offset under various supply voltages.

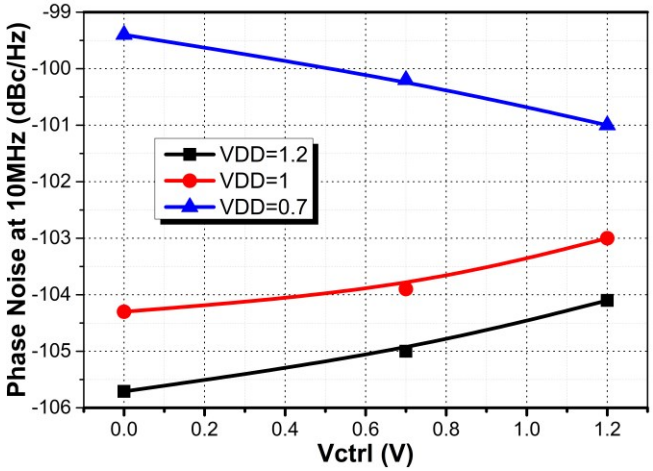

Fig 33. Measured CON phase noise varied with V_{ctrl}.

quality factor:

$$\frac{1}{Q_T}=\frac{1}{Q_{Var}}+\frac{1}{Q_L}\approx\frac{1}{Q_{Var}}=\frac{1}{\omega R_s C_{Var}} \qquad (14)$$

Here, varactor quality factor Q_{Var} is process dependent and the loss can only be minimized through sizing as shown in Fig. 18, whereas the metallic routing parasitics are highly sensitive to layout. However, compared to traditional T-line based resonator and power combiner [12], [13], [23], the slow-wave technique shrinks the size by at least a factor of 2 for power combining.

The frequency tuning can be done by adjusting both varactor and the supply voltage. The measured frequency tuning is shown in Fig. 34. Wide tuning range from 156.1 to 166 GHz can be observed, which is equivalent to 6.3% FTR. Note that the parasitics capacitance ($\approx C_{gs} + 0.3C_{gd}$) of the doubler changes with supply, leading to variation of the capacitive load for the CON core. Fig. 35 shows the output power and DC-to-RF efficiency over wideband. As the stacked SRR is a narrow-band metamaterial, the output power is not constant over frequency. In spite of this, the measured output power is better than 0 dBm, and the DC-to-RF power efficiency is higher than 2%, within the tuning range. Moreover, the proposed CON achieves the highest output power density (output power/area, mW/mm^2). State-of-the-art on-chip signal source performances

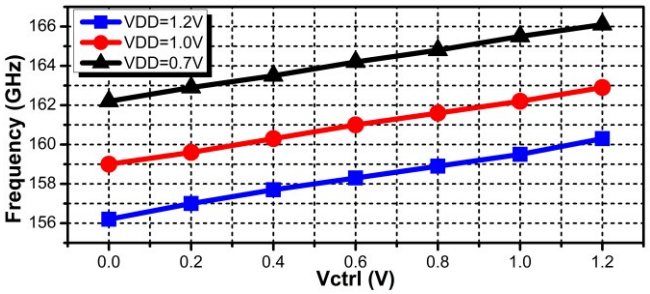

Fig 34. Measured frequency tuning range of the proposed CON.

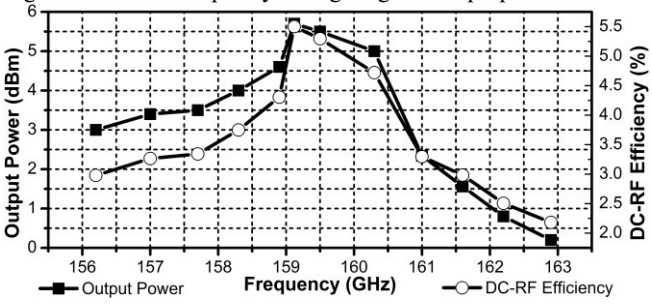

Fig. 35. Measured CON output power and the DC-to-RF efficiency.

are summarized and compared in Table III.

V. Conclusions

Split-ring resonator based devices are key components in the D-band OOK transceiver toward low power communication. In this paper, the stacked SRR modulator and slow-wave signal source are designed, analyzed and validated in D-band in 65-nm CMOS. The two designed are featured by compact high-Q magnetic SRR with the metal surface current strongly suppressed.

The dispersion relation, sizing and field distribution of the stacked SRR modulator are simulated and analyzed. Measured results show that the proposed modulator achieves 3 dB loss, peak 43 dB isolation, and state-of-the-art Q-factor of 89 and 40 dB extinction ratio at 125 GHz. The proposed design burns no static power while occupying only 40 µm × 67 µm silicon area.

A 4-way slow-wave coupled oscillator network is designed centered at 160 GHz. The slow-wave is generated on-chip with low loss as signal source for compact power combining in D-band. Measurement results show that the proposed CON achieves 3.7 mW output power, 5.5% DC-to-RF efficiency, 6.3% FTR and –105 dBc/Hz phase noise at 10 MHz offset, leading to state-of-the-art 70.1 mW/mm^2 power density, FOM of –171 dBc/Hz and FOM$_T$ of –172.7 dBc/Hz.

TABLE III
Sub-THz Signal Source Performances Comparison

Ref	[23]	[24]	[25]	[26]	[27]	[5]	This Work
Process (nm)	65	32	130 SiGe	45 SOI	65	65	**65**
Freq. (GHz)	105	136	190.5	170	215	132	**160**
Power (dBm)	4.5	2.3	–2.1	0	5.6	5.4	**5.7**
PN (dBc/Hz)	–93 @1M	/	–103 @10M	/	–94.6 @1M	–104 @25M	**–105 @10M**
Effi. (%)	5.3	5.3	0.22	1.1	4.6	2.4	**5.5**
FTR (%)	9.5	24	20.7	13.6	0.7	9.7	**6.3**$^{\overline{T}}$
Area (mm^2)	0.228	0.28	0.64	0.56	0.08	0.13	**0.053**
Power density (mW/mm^2)	12.4	6.1	0.96	1.8	45.4	26.7	**70.1**
FOM (dBc/Hz)	–172	/	–171.8	/	–159	–158	**–171**
FOM$_T$ (dBc/Hz)	–175	/	–169.7	/	–165	–154	**–172.7**

$$FOM = \mathcal{L}(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right)$$

$$FOM_T = \mathcal{L}(\Delta f) - 20\log\left(\frac{f_0}{\Delta f} \times \frac{FTR}{10}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) - P_{out}$$

$^{\overline{T}}$: frequency tuning by both varactor bias voltage and core drain bias voltage.

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Yuan Liang (S'18) is currently pursuing the Ph.D. degree in the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, focusing on mm-wave to terahertz integrated circuits design.

Chirn Chye BOON (M'09-SM'10) is currently with Nanyang Technological University, Singapore, as an Associate Professor. He specializes in the areas of radio frequency (RF) & MM-wave circuits and systems design for Biomedical and Communications applications.

Chenyang Li (S'13) is currently working toward Ph.D. degree in electrical engineering in Nanyang Technological University, Singapore, focusing on power amplifier design in CMOS.

Xiao-Lan Tang is currently a Research Assistant Professor with the Department of Electrical and Electronic Engineering, Southern University of Science and Technology, Shenzhen, China. Her current research interests include the silicon-based mm-wave integrated circuits design and passive device design based on surface wave transmission lines.

Herman Jalli Ng (M'16) received the Ph.D. degree in mechatronics from Johannes Kepler University, Linz, Austria in 2014. Currently he heads the Millimeter-Wave Wireless Group at IHP in Frankfurt (Oder), Germany.

Dietmar Kissinger (S'08–M'11–SM'14) received the Dipl.-Ing., Dr.-Ing. and habil. degree in electrical engineering from FAU Erlangen-Nürnberg, Germany, in 2007, 2011 and 2014, respectively.

He is currently a Full Professor for High-Frequency Circuit Design at Ulm University and the Head of the Institute for Electronic Devices and Circuits.

Yong Wang (S'11–M'16) received the Doctor of Philosophy degree in Electrical and Electronic Engineering from Nanyang Technological University, Singapore, in 2015. He is currently a Full Professor with School of Information and Communication Engineering, University of Electronic Science and Technology of China (UESTC).

Qingfeng Zhang (S'07–M'11–SM'15) is currently with the Southern University of Science and Technology, Shenzhen, China, as an Assistant Professor. His current research interests include emerging novel electromagnetics technologies and multidisplininary topics.

Hao Yu (M'06–SM'14) received the B.S. degree from Fudan University, Shanghai, China, and the Ph.D. degree from the Department of Electrical Engineering, University of California at Los Angeles, Los Angeles, CA, USA. He was with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. He is currently with the Southern University of Science and Technology, Shenzhen, China. His current research interests include CMOS emerging technology for data sensors, links, and accelerators.