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Postbond Test of Through-Silicon Vias With Resistive Open Defects

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Abstract—Through-silicon vias (TSVs) technology has attracted industry interest as a way to achieve high bandwidth, and short interconnect delays in nanometer three-dimensional integrated circuits (3-D ICs). However, TSVs are critical elements susceptible to undergoing defects at steps, such as fabrication and bonding or during their lifetime. Resistive open defects have become one of the most frequent failure mechanisms affecting TSVs. They include microvoids, underfilling, misalignment, pinholes in the oxide, or misalignment during bonding, among others. Although considerable research effort has been made to improve the coverage of TSV testing, little attention has been paid to weak (resistive) open defects causing small delays. In this work, a postbond oscillation test strategy to detect such small delay defects is proposed. Variations in the duty cycle of transmitted signals after unbalanced logic gates are shown to help in the detection of weak open defects in TSVs. HSPICE simulations, including process parameter variations, have been considered, and results show the effectiveness of the method in the detection of weak open defects above 1 kΩ. Experimental work on a 65-nm IC also corroborates the detection capability of the proposal.

Index Terms—Design for testability, duty cycle (DC), resistive open defect, three-dimensional integrated circuit (3-D IC), through-silicon via (TSV), TSV testing.

I. INTRODUCTION

THE semiconductor industry is continuously demanding products with higher integration density and performance, lower power consumption, and reduced cost. Among the different alternatives, three-dimensional integrated circuits (3-D ICs) have developed as a solution to meet such demands [1]. A 3-D IC integrates a vertical stack of tiers of thinned 2-D ICs into a single package interconnected by means of through-silicon vias (TSVs). A TSV is a vertical via formed between tiers through silicon or oxide layers. TSVs reduce interconnectivity length, permit higher density, and generate low-capacity interconnects compared to traditional wire bonds.

Both vertical and horizontal interconnections in TSV-based 3-D ICs are susceptible to a variety of manufacturing defects. However, the special features of 3-D ICs induce particular test challenges that are of major importance [2]. These challenges are related to the known-good-die (KGD) problem, i.e., determining the quality of every tier before being stacked. Since new defect types arise from the particular processing steps of 3-D ICs, testing these specific structures (TSVs) not present in other circuits is a must [2], [3].

Current fabrication techniques allow TSV densities up to tens of thousands per mm^2 [4]. Thus, efficient testing of such delicate and numerous structures becomes a major concern. In fact, TSVs are susceptible to undergoing defects during fabrication, bonding to the next tier, or their lifetime [4]. Typical defects during fabrication are microvoids and underfilling (both leading to weak opens) or pinholes in the oxide (leading to shorts between the TSV and the substrate). Ineffective removal of the seed layer may also generate shorts between TSVs, and misalignment during bonding may generate opens or shorts. During the product's lifetime, differences in the coefficients of thermal expansion (CTEs) of different materials might cause thinned dies to warp. Furthermore, weak opens with small impact during normal operation may degenerate into a catastrophic defect (full open) due to electromigration [6], [7].

TSVs are tested at different stages of the fabrication process. Prebond test, applied before every tier is stacked, is desirable to prevent stacking yield loss. Postbond test is also required since new defects may appear during the bonding process, and some defects that appeared during the prebonding stage might not have been detected. As TSV yield may still not be satisfactory, redundancy TSVs and self-repairing mechanisms for each TSV could be included to ensure full functionality of 3-D ICs [8]–[12].

As far as prebond testing is concerned, TSVs are too small for a test probe, and the number of test probe pads required is not affordable. Thus, although research is devoted to overcoming such disadvantages [8]–[14], the prebond test of TSVs is still challenging. As an alternative to probe testing, built-in self-test (BIST) structures have been proposed to detect the presence of a defective TSV. In the presence of weak defects, the BIST circuit must consider the analog properties of the TSV. In this direction, some works have been proposed to detect voids (opens) [14]–[16] and pinholes (shorts) [17]–[20] during the prebond testing.

Although considerable research effort has been expended on improving postbond TSV testing in the case of catastrophic defects, little attention has been paid to weak defects, especially weak open defects and shorts, which cause delay faults

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in the circuit. During postbond testing, a TSV behaves as an interconnect element. Therefore, existing methods to detect interconnect defects can be applied [5]. In this direction, a method is proposed in [22] to estimate the additional delay introduced by a resistive open defect in a TSV. This method activates a voltage divider in each TSV created through one transistor and the TSV itself, and an analog comparator and a reference voltage determine the pass/fail result. Another postbond TSV test method requiring analog comparators and reference voltages, in addition to some supporting digital blocks, is presented in [23] and [24]. The authors propose the detection of faulty TSVs by comparing their output voltage through two voltage comparators. The work does not consider the impact of process variations and presents results at the simulation level only.

More recently, a method able to measure the RGC parameters of TSVs by using switched-capacitor circuits and a proper calibration step has been proposed in [25]. Fault detection effectiveness is evaluated with electrical simulations. The main drawback of this method is the long measurement time.

A BIST architecture to detect delay defects by means of a postbond oscillation test [26] is evaluated in this work. The concept of delay characterization of TSVs using oscillation test was previously used in [27]–[29], where the technique is applied to pairs of TSVs connected in such a way that they create two-stage ring oscillators (ROs). By changing the strength of the drivers (sensitivity analysis), the authors extract the delay generated by each of the TSVs belonging to the tested pair. The same authors presented an evolved technique called variable output thresholding in [30], where each TSV output driver may become a Schmitt-trigger inverter. By changing the threshold voltage of the inverter, the period of oscillation changes, and this difference reflects the propagation delay across each TSV. However, the measurement of frequency required to apply the method may be time-consuming.

More recently, an oscillation-based postbond TSV test method able to detect resistive open defects in multiple TSVs in parallel was presented at the simulation level [31]. TSVs are compared in pairs, and the method requires extra area proportional to the number of TSVs.

The postbond TSV testing technique proposed in this work consists in transmitting a periodical oscillating signal through the TSV under test. Next, the signal is fed into unbalanced logic gates, and the measurement of the duty cycle (DC) of the resulting signals determines whether there is a delay fault.

The rest of this paper is organized as follows. Section II shows the electrical model used for the TSV structure. Section III reviews the concept of test based on DC variations. Section IV analyzes the impact of the frequency of the oscillating signal, while Section V analyzes the impact of process parameter variations. Simulation results derived from the designed circuit are summarized in Section VI. Area overhead and the test time estimation are given in Section VII. Experimental results are shown in Section VIII. Finally, conclusions on the effectiveness of the proposal are drawn in Section IX.
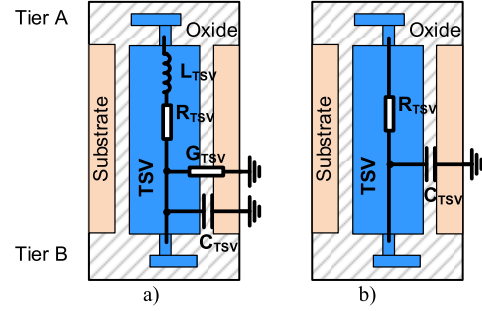

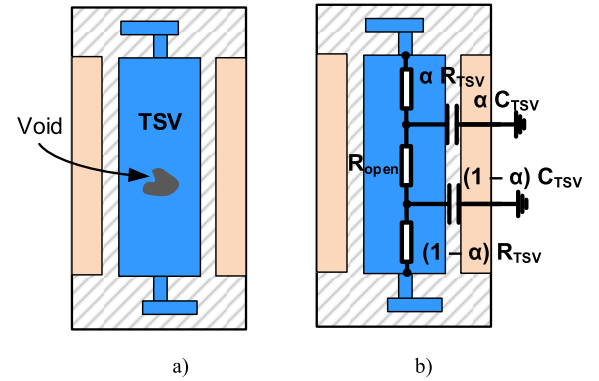Fig. 1. (a) Dumped electrical model of a defect-free TSV and (b) simplified *RC* model.

Fig. 2. (a) Void in the metal connection between tiers and (b) electrical *RC* model of a TSV with a resistive open defect located at a distance α from the top tier end of the via.

II. TSV ELECTRICAL MODEL

A widely accepted model describing the electrical behavior of an isolated TSV consists of a lumped *RLCG* element, as illustrated in Fig. 1(a) [31]. A TSV is modeled with a resistance (R_{TSV}) on the order of a few tens of mΩ, an inductor (L_{TSV}) on the order of a few pHs, and a capacitor (C_{TSV}) on the order of tens of fF. All of these components are strongly dependent on the physical dimensions of the TSV. For present manufacturing technologies and low or middle range frequencies below 1 GHz, the conductance and inductance components have a low impact on the electrical behavior of the TSVs and can be eliminated from the model [33], leading to a pure *RC* behavior Fig. 1(b).

The electrical effect of a void or underfilling created during the manufacturing process or normal operation in the field can be modeled as an increment in the equivalent series-resistance of the TSV [21]–[34]. Fig. 2 illustrates a defective TSV with a resistive open modeled by R_{open}. The defect is located at a distance α (in the percentage of the total length) from the top tier end of the via.

In Section III, the electrical behavior of a TSV with a weak open defect, as well as the basis of the testing technique proposed, is described.

III. TEST BASED ON DUTY CYCLE VARIATIONS

This section reviews the proposed testing strategy based on the transmission of a periodical oscillating signal through
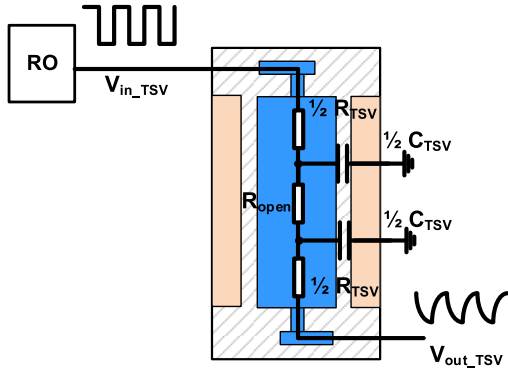
Fig. 3. Defective TSV with a resistive open (located at $\alpha = 0.5$) excited by a periodical oscillating signal.

Fig. 5. (a) Charge and discharge voltage of a capacitor ($C = 50$ fF) through a constant resistance ($R = 1$ kΩ) and normalized power supply. (b) Voltage at the output of a balanced inverter with logic threshold voltage $0.5V_{DD}$(black), an unbalanced inverter with logic threshold voltage equal to $0.2V_{DD}$(blue) and$0.8V_{DD}$(red).
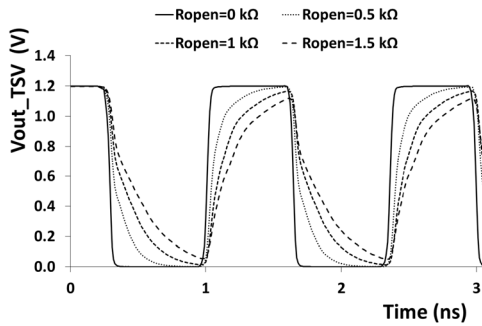

Fig. 4. Voltage response to a periodical square signal at the output of the TSV for different resistive defects. For a given location of the defect, the higher the resistance, the slower is the response.

the TSV under test [26]. The technique consists of measuring the DC variations of the transmitted signal after crossing an unbalanced logic gate.

Let us assume a periodical oscillating signal connected to one end of the TSV under test, as shown in Fig. 3, where the output of an RO has been used for this purpose. In the case of a defect-free via, the resistive and capacitive components of the TSV (R_{TSV} and C_{TSV}) and the current strength of the driver determine the voltage response at the output of the via (out_TSV). However, the presence of a resistive defect in the circuit (R_{open}) impacts this expected response, as illustrated in Fig. 4 for different resistive defects on the order of kΩ. These HSPICE simulations were carried out with a 65-nm STMicroelectronics technology and a TSV modeled by $C_{TSV} = 50$ pF and $R_{TSV} = 10$ mΩ with the open located at $\alpha = 0.5$, and nominal $V_{DD} = 1.2$ V. Parameter α indicates the distance from the driving tier (in the percentage of the total length). In the case of high R_{open}, the oscillations can even be prevented from happening.

Although the frequency of the transmitted signal (V_{out_TSV}) is the same as for the input signal (V_{in_TSV}), the transmitted signal may be degraded due to the highly resistive nature of the open defect. Fig. 4 illustrates this fact, where the delay of the rising/falling edges of the TSV response increases with R_{open}. The direct measurement of this extra delay added by the defect is complex due to the difficulty in synchronizing input and output signals since they belong to different tiers.
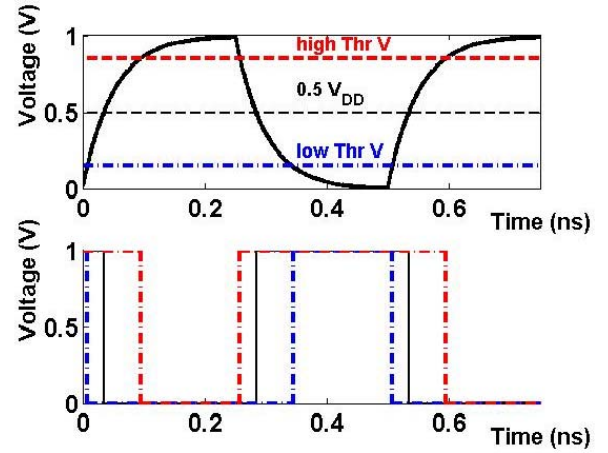
This work proposes the connection of an unbalanced inverter to the output of the TSV to detect the open defect in the via under test. In order to illustrate this concept, let us assume the charge and discharge of a capacitor $C = 50$ fF through a resistance $R = 1$ kΩ at a constant voltage of 1 V, as illustrated in Fig. 5(a). Let us assume that this signal is propagated through three ideal inverters in parallel: one with a logic threshold voltage equal to half the power supply ($0.5V_{DD}$), another with a lower threshold voltage (l_th), and the third with a higher threshold voltage (h_th), as indicated in Fig. 5(a) by the corresponding horizontal voltage levels. The outputs of the three inverters are shown in Fig. 5(b), where the dotted red and blue (black solid) signals correspond to the output of the unbalanced (equilibrated) inverters. Although the frequency of the three signals is the same (and equal to that of the input signal), this is not the case for the DC.

It is straightforward to see that the DC of the signal coming from the balanced inverter remains 50% independently of R. However, the DC of the output of the unbalanced inverters decreases or increases proportionally with R. In the particular cases of $l\_th = 0.2V_{DD}$ and $h\_th = 0.8V_{DD}$, their DCs are 36% and 64%, respectively. Note that the period of the input signal must be on the order of the time constant of the TSV charging/discharging circuit in order to obtain clearly different DC values.

To take advantage of the DC variations caused by excessive TSV resistances, let us consider the circuit in Fig. 6. The response at the output of the unbalanced inverter (V_{out_inv}) is shown in Fig. 7(a) for the case of a low threshold voltage inverter, and in Fig. 7(b) for the case of a high threshold voltage one.

In order to design a low threshold voltage inverter, the nMOS transistor was designed wider than the pMOS transistor ($W_n = 5W_p$ in this example). The rising edge is more sensitive to the slope of the input voltage than the falling edge due to the smaller size of the pMOS transistor. Using a first-order approximation (as illustrated in Fig. 5), the extra RC
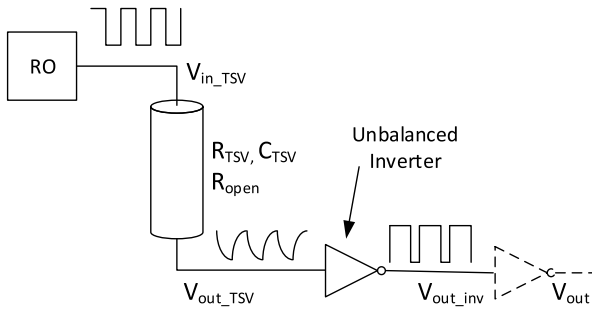
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Fig. 6.   Circuit proposed for TSV testing.

Fig. 8.   DC of the unbalanced inverter output (Vout_inv in Fig. 6) versus the resistance of the open defect (Ropen) in the case of low (solid line) or high (dotted line) logic threshold voltage.
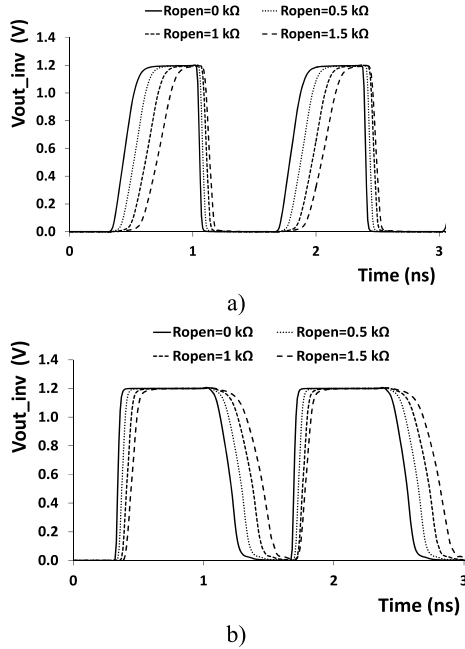

Fig. 7.   Voltage at the output of the unbalanced inverter connected to the TSV under test in Fig. 6 with (a) low or (b) high logic threshold voltage.

Fig. 9.   Response at the output of the defective TSV (Vout_TSV in Fig. 6) for two different periods of the transmitted signal, namely, (a) $T = 1.5$ ns and (b) $T = 4$ ns.
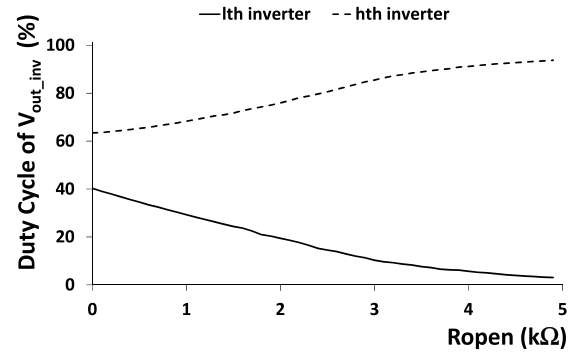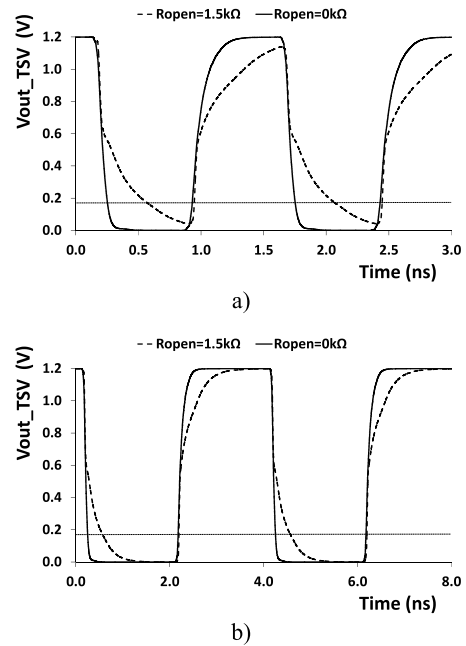
delay created by the resistive defect depends on the product $R_{open}C_{TSV}$ and impacts the percentage of the high voltage time with respect to the time the signal is low. A symmetrical behavior is found for the case of a high threshold voltage inverter. This phenomenon is proposed to test the TSV against resistive open defects. Fig. 8 illustrates the DC of the voltage at the output of the unbalanced inverters versus the resistance of the defect.

Note that the effect of R_{open} on the DC of the output at the unbalanced inverter can be propagated to the output of the circuit (V_{out} in Fig. 6) through one or more balanced inverters. This subsequent inverter helps in shaping the voltage into a square wave signal.

IV. IMPACT OF THE TRANSMITTED SIGNAL FREQUENCY

This section analyzes the behavior of a defective TSV versus the frequency of the transmitted signal.

As shown in Fig. 5, the main electrical nature of the TSV is capacitive. The charging/discharging time as a response

to an input square signal depends on the time constant of the system made up of the resistance of the pulling network and the parasitic capacitance of the 3-D via. The signals transmitted through the defective TSV (V_{out_TSV} in Fig. 6) for two different periods are shown in Fig. 9. The selected frequencies, $T = 1.5$ ns and $T = 4$ ns in this case, are on the order of the time constant of the system.

To clearly detect the open defect in the TSV, the percentage of change in the response compared to the defect-free case needs to be significant and measurable. Thus, it is advisable that the period of the signal be small enough, as illustrated in Fig. 9, where the outputs of the defective TSV for input square signals of $T = 1.5$ ns and $T = 4$ ns are shown. Although the charging time is the same, the percentage of change between the defect-free case (Ropen = 0 kΩ) and the defective case (Ropen = 1.5 kΩ) is greater for a higher

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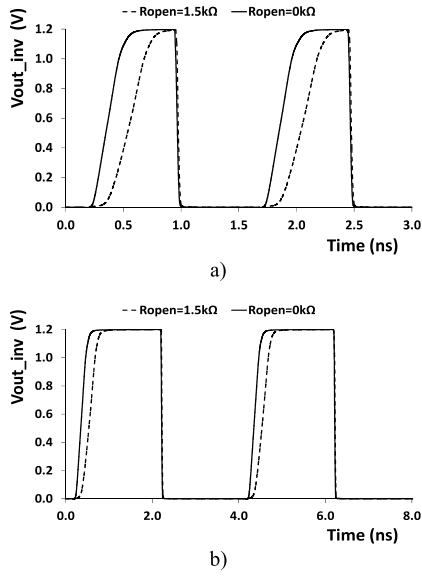RODRÍGUEZ-MONTAÑÉS *et al.*: POSTBOND TEST OF THROUGH-SILICON VIAS WITH RESISTIVE OPEN DEFECTS 5

Fig. 10. Response at the output of the unbalanced inverter (Vout_inv in Fig. 6) for two different periods of the transmitted signal, namely, (a) $T = 1.5$ ns, where DCs are 38% and 22% for Ropen = 0 kΩ and Ropen = 1.5 kΩ, respectively, and (b) $T = 4$ ns, where DCs are 52% and 46% for Ropen = 0 kΩ and Ropen = 1.5 kΩ, respectively.
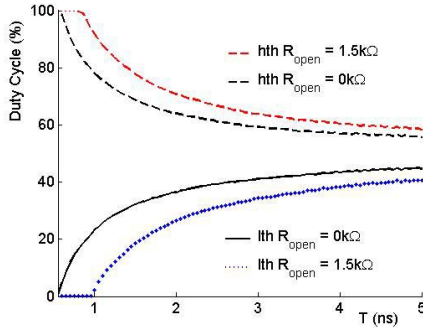
Fig. 11. DC of the output of two unbalanced inverters versus the period of the transmitted signal T. High threshold voltage h_th inverter results (black dotted and red lines) and low threshold voltage l_th results (black solid and blue dashed lines), as well as defect-free case (Ropen = 0 kΩ) and illustrative defective case with Ropen = 1.5 kΩ, are shown.

frequency. As a consequence, the output of the unbalanced inverter (see Fig. 10) shows a more significant DC change in the case of shorter periods of the oscillating signal. In the example of Fig. 10, the DC difference is 16% for $T = 1.5$ ns versus 6% for $T = 4$ ns.

Fig. 11 shows the dependence of the DC of the transmitted signal after two unbalanced inverters with low (l_th) and high (h_th) threshold voltage versus the period of the transmitted signal. The case of Ropen = 1.5 kΩ was selected for the example versus the defect-free case. As can be seen, the lower the frequency, the less significant the change in the DC (except for the case of a nonoscillating defective signal).

The characterization in Fig. 11 helps in the selection of the range of frequencies useful to detect the targeted defective TSV. Also, note that in the proposed circuit, where an RO is used as the signal generator, the increase in the power voltage
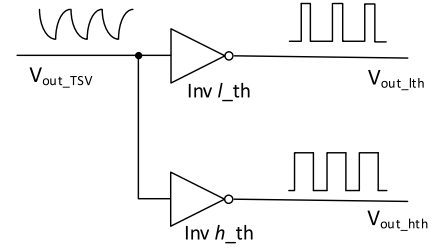
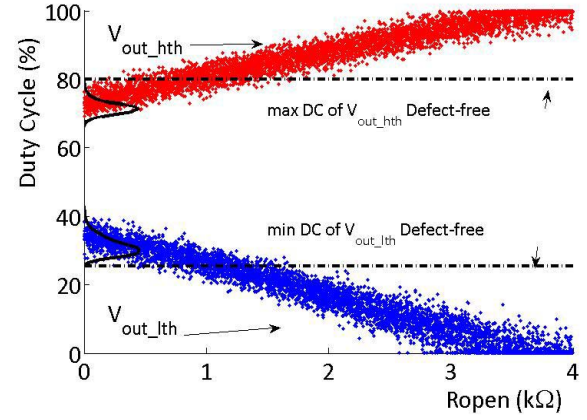Fig. 12. Unbalanced inverters connected to the output of the TSV under test.

Fig. 13. DC distribution of the output of inverters with l_th (blue) and h_th (red) versus the resistance of the open defect. Dotted horizontal lines indicate the boundaries of the defect-free distributions caused by process parameter variations.
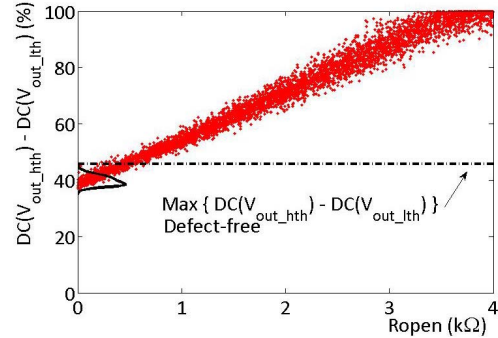
Fig. 14. Difference of the DC of the signals at the outputs of the two asymmetrically unbalanced inverters (see Fig. 12) versus the resistance of the defect. The histogram of the defect-free distribution is indicated on the y-axis (x-axis dimension is meaningless). The horizontal line enables the range of detectable defects to be identified.

will decrease the period of the signal (for a given circuit), and this oscillating signal connected to the defective TSV will, in turn, increase the significance of the DC variation. In the case of a nonoscillating signal, the detection of the defect is straightforward.

In Section V, the effect of the process parameter variations on the DC is analyzed.

V. PROCESS PARAMETER VARIATIONS

HSPICE simulations were carried out to characterize the impact of process variations on the proposed testing strategy. Process variations were assumed for transistors according to
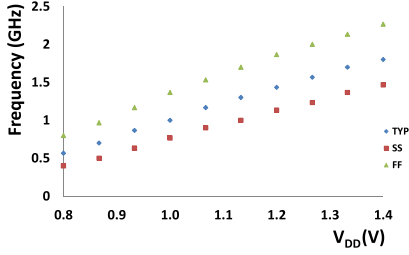
Fig. 15.   HSPICE simulation results of the RO frequency used to generate the periodical square signal. Results for different corners are shown.

Fig. 17.   Illustrative structure of eight TSVs under test with their selecting MUXs and TGs. The DCD circuit is detailed in Fig. 18.
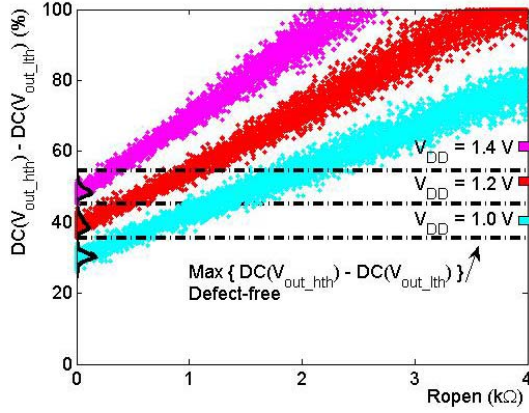

Fig. 16.   Difference of the DC of signals at the outputs of the two asymmetrically unbalanced inverters (see Fig. 12) versus the resistance of the defect at different power supplies. The histogram of the defect-free distribution is indicated on the y-axis (x-axis dimension has no meaning). The horizontal line enables the range of detectable defects to be identified.

the information provided by the manufacturer of the technology considered. Also, variations of the electrical parameters of TSVs were assumed according to a Gaussian distribution with sigma equal to 5% of their nominal value.

The circuit in Fig. 12 includes two asymmetrically unbalanced inverters connected to the TSV under test. The upper inverter has a low threshold voltage (l_th) since the nMOS transistor is several times wider than the pMOS (five times in this example). Symmetrically, the lower inverter has a high threshold voltage (h_th).

Fig. 13 illustrates the effect of process variation on the outputs of the circuit in Fig. 12. A set of 5000 samples was considered. The DC distribution of the output at the low (high) threshold voltage inverter is plotted in blue (red) versus the resistance of the defect. Both distributions are symmetrical, as expected. Furthermore, attached to the y-axis are the histograms of the DC of 5000 defect-free cases, where the boundaries limiting the detection of defective TSVs are indicated by horizontal lines.

Based on the results in Fig. 13, open resistances higher than 2 kΩ can be detected by the proposed technique. However, the combination of the outputs of both inverters can improve the range of defect detection, as shown next.

Process variations have an impact on the frequency of the signal generated by the RO, which increases with adding variations in the electrical parameters of the TSV. However,
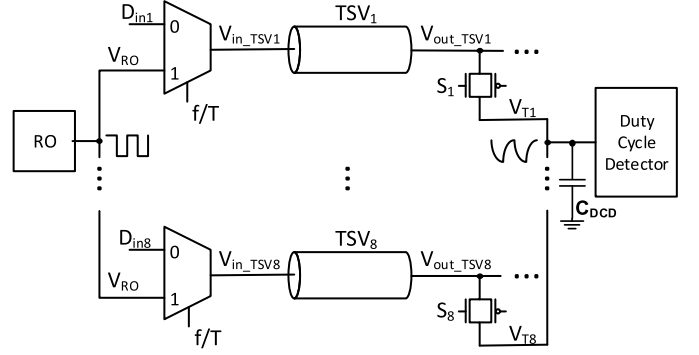
the input voltage connected to the two inverters is the same, and this can neutralize the effect of such process parameter variations. Fig. 14 shows the distribution of the difference between the DC of the output at the inverter with a high logic threshold voltage (V_{out_hth}) and the DC of the output at the inverter with a low logic threshold voltage (V_{out_lth}) versus R_{open}. The histogram of the difference between DCs of 5000 defect-free circuits is shown on the y-axis (x-axis dimension is meaningless). Its maximum value (dotted horizontal line) indicates the minimum R_{open} able to be detected, which is on the order of 700 Ω. Thus, by using the difference between DCs, the minimum R_{open} detected decreases from 2 to 0.7 kΩ.

As pointed out in Section IV, the increase of the oscillating signal frequency, up to a certain security margin, improves the detection of open defects. Since the increase of power supply also increases the RO oscillation frequency, as shown in Fig. 15, the detectability results are expected to vary with V_{DD} changes. Fig. 16 illustrates this fact, where defects higher than 1 kΩ are undetected at $V_{DD} = 1.0$ V while this limit drops to 0.5 kΩ at $V_{DD} = 1.4$ V.

VI. SIMULATION RESULTS

This section presents the simulation results for the application example in Fig. 17, which consists of a structure under test made up of eight TSVs. The duty cycle detector (DCD) was implemented in a digital block as a simpler alternative to general DCDs [35], which require analog structures occupying large areas and complex control signals. Simulations accounted for the process variations of the 65-nm STMicroelectronics technology used. $C_{TSV} = 50$ fF and $R_{TSV} = 10$ mΩ were assumed with a variation up to 10% of their nominal values. Defects were injected with a uniform distribution of R_{open} from 0 to 5 kΩ (5000 samples).

In the circuit, the output of the RO is shared by the TSVs under test, and a function/test mode is selected (f/T) through MUXs. The outputs of the TSVs are connected to the digital DCD by means of transmission gates that select one individual TSV under test each time. The basis of the DCD is the circuit in Fig. 12 with similar operation as in [26].

The DCD used in this example is illustrated in Fig. 18, where NP_{l_th} (NP_{h_th}) indicates the count of pulses

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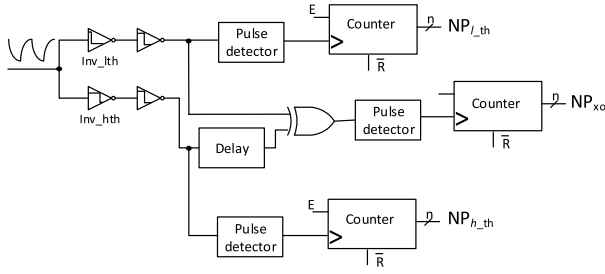

Fig. 18. DCD circuit. Pulse detector blocks are illustrated in Fig. 19 while the delay block is composed of four inverters.
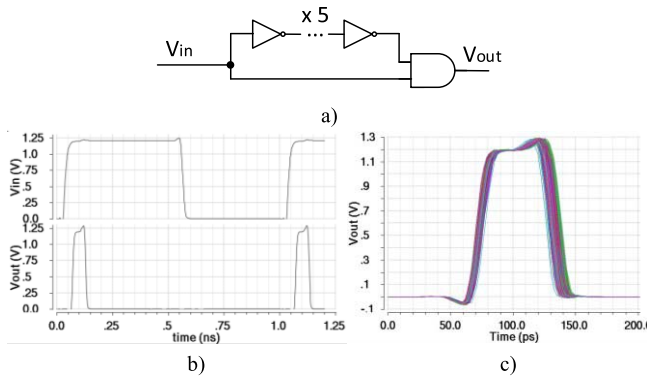

Fig. 19. (a) Pulse detector circuit, (b) V out response at rising transitions (Vin), and (c) output voltage pulse under process variations (1000 samples).

Fig. 20. Test results for R_{open} < 2 kΩ (2000 samples) at different power supplies. (a) All R_{open} > 900 Ω are detected (in blue) at nominal V_{DD} = 1.2 V while (b) all R_{open} > 550 Ω are detected (in blue) at V_{DD} = 1.4 V.

transmitted through the low (high) threshold voltage inverter. Note that only one of these counts is needed since their behavior in the presence of defects is symmetrical. A third count (NP$_{xo}$) is used to extract information about the overlapping characteristic between the previous ones (NP$_{l\_th}$ and NP$_{h\_th}$). Overlapping time informs about the difference between the DC of the output at the inverters with a high and low logic threshold voltage (for more details, see [26]).

Pulse detectors were added to properly activate the corresponding binary counters considered to test the TSVs. By using pulse detectors, the width of the clock signal of each counter is assured to be longer than the required minimum pulse width. The gate-level schema of the pulse detector used is shown in Fig. 19(a), consisting of a chain of five inverters and one AND gate. After the pulse detector receives a rising transition at the input, a pulse is generated at the output as illustrated in Fig. 19(b). The size of transistors was designed to minimize the impact of process variations, as shown in Fig. 19(c).

The test time needed by the DCD to evaluate the relationship between the DC at the output of the unbalanced inverters is on the order of several periods of the RO output signal, i.e., a few ns.

Simulation results in Fig. 20 show that R_{open} higher than 900 Ω can be detected at nominal power supply voltage. However, the impact of the process parameter variations causes part of R_{open} lower than 900 Ω to escape the test, as shown in red in Fig. 20. Better results are obtained at higher V_{DD}, as expected.
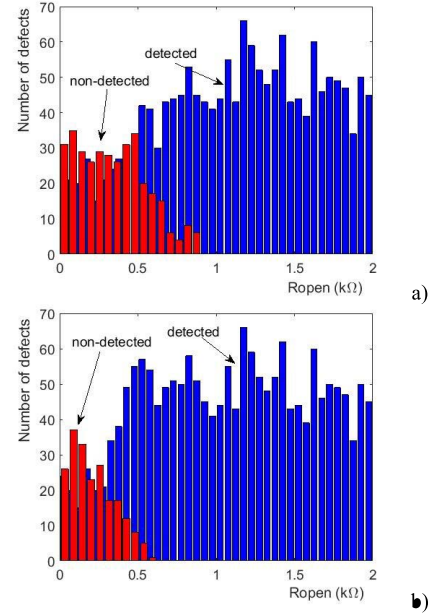
VII. AREA COST AND TEST TIME ESTIMATION

The present proposal requires a set of extra logic gates to test a group of N TSVs. Derived from Fig. 17, the following logic structures are needed to control, feed, and analyze the response of the circuit.

1) One multiplexer at the input of each TSV (as a selector between the functional or testing signal).
2) One transmission gate (TG) at the output of each TSV (to send the testing response to the DCD).
3) One control block (ring counter) to select one TSV each test time (through signal S_i). This block needs one flip-flop (FF) per TSV (not shown in Fig. 17).
4) One RO to generate the oscillating test signal of the whole set of TSVs under test.
5) One DCD per each set of TSVs

$$\text{Area (Test } N \text{ TSVs)} = N(A_{\text{MUX}} + A_{\text{TG}} + A_{\text{FF}}) + A_{\text{RO}} + A_{\text{DCD}}.$$

The area occupied by the designed blocks listed above is detailed in Table I according to the STMicroelectronics CMOS 65-nm technology considered in this work. A total of 45.4 μm^2 area is required per TSV, considering the MUX (5.5 μm^2), TG (7.7 μm^2) and selecting FF (32.2 μm^2) modules. As for the global circuit, the RO area is 43.2 μm^2 while the DCD area is 214.2 μm^2.

The DCD was implemented according to the schematic in Fig. 18 where a total of 46.2 μm^2 area is occupied by the unbalanced and balanced inverters, delay block, XOR and pulse detectors. These blocks must be close enough to the set of TSVs under test to limit extra capacitive load of interconnect lines on the considered signals. The two counters required in the design could be shared by different DCDs at the expense

TABLE I
INDIVIDUAL PER TSV AND GLOBAL CIRCUITS AREA OVERHEAD

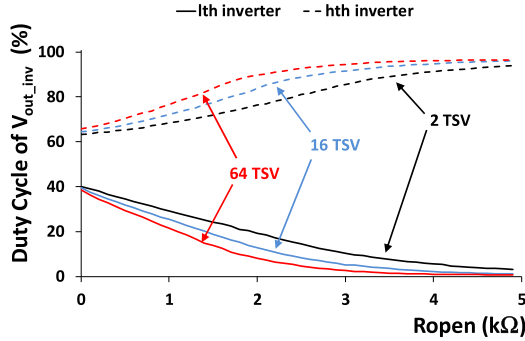|	Circuit per TSV			Global to N TSVs	
	MUX	TG	FF	RO	DCD
Area (μm^2)	5.5	7.7	32.2	43.2	214.2

Fig. 21. Effect on the DC of the transmitted signal of multiple TSVs interconnected at the input of the DCD in Fig. 17.

of more test time. Each counter occupies 84 μm^2. Note that only one out of NP$_{l\_th}$ and NP$_{h\_th}$ is needed because they both provide equivalent information. A total of 214.2 μm^2 area is required for the complete DCD (46.2 μm^2 for the logic blocks and 168 μm^2 for the two counters).

To determine the number N of TSVs able to be tested with the same DCD, the effect of the parasitic capacitance at the input of the DCD (C_{DCD} in Fig. 17) was evaluated by means of HSPICE simulations. Fig. 21 illustrates the DC variation of the transmitted signal V_{out_inv} (Fig. 6) after the unbalanced inverters of the DCD for 2, 16, or 64 interconnected TSVs (Fig. 17). Due to the low-pass filter topology of the R_{open}/C_{TSV} and TG/C_{DCD} pairs, the impact of C_{DCD} on the average transmitted value (directly related to the DC) is limited, and up to 64 TSVs can be connected without important impact on the electrical behavior. The simulations assumed a spacing of 10 μm between TSVs and a parasitic capacitance per unit length of 0.16 fF/μm for a 65-nm technology [36].

The test time needed to select each TSV corresponds to one test clock cycle plus the time to evaluate the response of each via, which equals several periods of the RO signal (on the order of 1 GHz). The choice of 16 or 32 cycles requires around 16/32 ns per TSV to evaluate the defective/defect-free behavior. Since the postbond test is performed by using a wafer automatic test equipment (ATE) with long test clock cycles on the order of tens of ns, one test clock cycle can be enough to count the pulses transmitted from the RO through the TSV under test.

A comparison between this work and previous postbond test techniques [22], [23] and oscillation-based methods published by other authors [30] is summarized in Table II. Not provided data is indicated with a dash (-). Note that neither the extra area required for the functional or test signal selection through MUX nor the control circuit based on FFs is provided

TABLE II
COMPARISON WITH PREVIOUS WORKS

| Test proposal	[22]	[23]	[30]	This work
Principle	Voltage divider	Voltage divider	Oscillation period measure	Duty Cycle measure
Analog voltage reference	yes	yes	no	no
Process variations	no	no	yes	yes
Test circuit per TSV	nMOS + comparator	nMOS + pMOS + inverter	ST inverter + XOR	TG
Area per TSV (μm^2)	-	-	35	7.7
Global circuit per N TSVs	-	comparator	12-bit counter	RO + DCD
Global Area per N TSVs (μm^2)	-	11	-	257.4
N	1	thousands	thousands	64
Technology node	45nm	45nm	90nm	65nm
Minimum Ropen	1kΩ	Hundreds of Ω ?	2kΩ	550Ω
Test time per TSV (T$_{CLKC}$)	-	1 x	1.5 x	1 x
Experimental work	no	no	no	yes
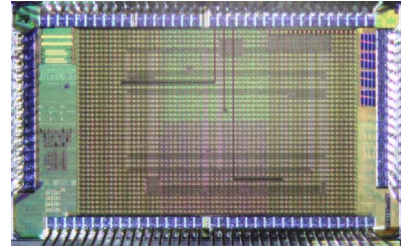
Fig. 22. Manufactured integrated circuit.

in Table II. However, they are assumed to be of the same nature and complexity for all the works.

The main advantage of the present proposal is that only a total of 11.72 μm^2 area overhead is needed per TSV (without considering the MUX selectors and control circuit). This value is derived from (1) the area overhead of one TG per TSV (7.7 μm^2) and (2) the global RO area (43.2 μm^2) plus the DCD area (214.2 μm^2) shared by each group of 64 TSVs (resulting in 4.02 μm^2 per TSV). A further advantage is that the range of resistive defects detected is on the order of hundreds of Ω.

VIII. EXPERIMENTAL RESULTS

A circuit was designed and sent to fabrication based on STMicroelectronics CMOS 65-nm technology. The design includes the test circuit proposed in previous sections to corroborate the presented methodology. The structure under test is based on the architecture in Fig. 17, while the DCD is the one in Fig. 18. A manufactured multiproject IC, where the design area and its corresponding pads occupy part of the left area of the die, is shown in Fig. 22.
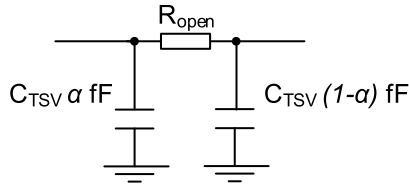
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Fig. 23. Circuit of defective TSVs considered in the experimental design. Parameter α selects the location of the defect ($\alpha = 0$ for defects at the left end of the TSV and $\alpha = 1$ for the defect at the right end of the TSV).

TABLE III

LIST OF LOCATIONS AND VALUES OF FIXED RESISTANCES IN TSVs

TSV	α % (location)	Ropen kΩ
TSV$_1$	20	1
TSV$_2$	40	2
TSV$_3$	50	0.65
TSV$_4$	50	1
TSV$_5$	50	1.5
TSV$_6$	50	2
TSV$_7$	50	4
TSV$_8$	60	3
TSV$_9$	80	3

TABLE IV

LOCATIONS OF TRANSMISSION GATES IN TSVs

TSV	α % (location)
TSV$_{10}$	20
TSV$_{11}$	40
TSV$_{12}$	50
TSV$_{13}$	60
TSV$_{14}$	80

Since the available design kit does not allow the use of the optional 3-D kit of the technology, the TSVs were emulated by two different capacitive elements. These capacitive elements are either metal–insulator–metal or metal-to-metal capacitors [15]. The capacitive behavior of a TSV during the postbond phase is expected to be similar enough to that of the emulated TSVs to derive results, which confirm the efficiency of the proposal. Another advantage of using such capacitors is the ease of injecting open defects at different locations along the capacitive element, as shown in Fig. 23. The nominal parasitic capacitance value for these equivalent TSVs is 100 fF.

Fixed resistances and TGs were used as resistive elements for emulating open defects. Table III shows the list of fixed resistances, with their locations (TSV$_1$ to TSV$_9$) and values on the order of kΩ. These values are around the expected critical resistance for the worst-case scenario, with $\alpha = 0.5$, assuming the proposed test structure is in both tiers.

TGs were considered to vary the resistance of each open defect. Table IV shows their chosen locations (TSV$_{10}$ to TSV$_{14}$) and Fig. 24 illustrates their configuration. The range of the equivalent resistance obtained with each TG versus V_{DD} (normalized) is shown in Fig. 25 for the case of the nominal supply voltage ($V_{DD} = 1.2$ V) and variations of $\pm$ 0.1 V.
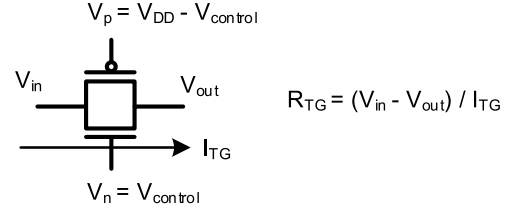

Fig. 24. Transmission gate configuration used to generate a variable resistance for emulating resistive open defects.
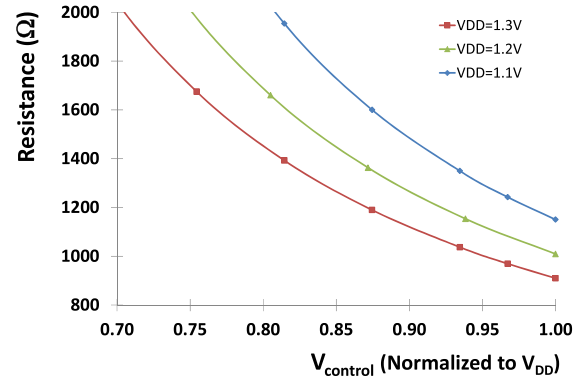

Fig. 25. HSPICE simulated equivalent resistance of the transmission gate versus $V_{control}$ (normalized to V_{DD}) according to the circuit in Fig. 24.

TABLE V

SIZE OF TRANSISTORS FOR SPECIAL INVERTERS AND XOR GATE

Logic Gate (L_{min}=60nm)	W_n	W_p
Low Threshold inverter	22 L_{min}	2.25 L_{min}
High Threshold inverter	2.25 L_{min}	34 L_{min}
Compensating_delay inverter	13.5 L_{min}	20 L_{min}
XOR	10 L_{min}	20 L_{min}

In order to implement the unbalanced inverters, compensating delay inverters and the XOR gate, the transistor sizes in Table V were selected. Widths of transistors sufficiently large to minimize process parameter variation effects were chosen, based on extensive HPSICE simulations.

In Sections VIII-A and VIII-B, detectability results experimentally obtained with the manufactured circuit are presented.

A. Experimental Characterization of the RO and TGs

Ten available chips were measured for the experimental work. The inclusion of a defect-free via (TSV$_0$) allowed the characterization of RO frequency variability at different V_{DD} voltages. Fig. 26 illustrates the number of pulses counted by the DCD (see Fig. 18) arriving from the low threshold voltage inverter path (NP$_{l\_th}$) versus the high threshold voltage inverter path (NP$_{h\_th}$) of each IC. A maximum of one unit difference appears between the counts of each particular sample for an illustrative 30 ns measure time. The count difference between samples is below 10%, as predicted by the technology variability.
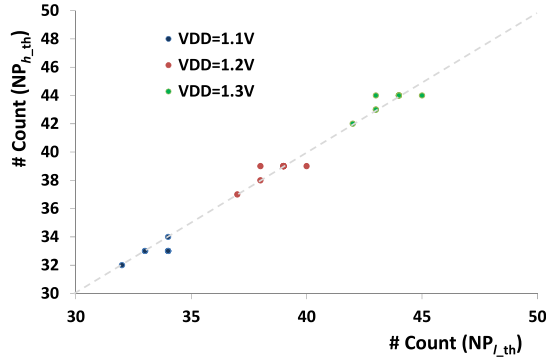
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Fig. 26.   Pulse count of the transmitted signal through the low threshold voltage inverter path (NP$_{l\_th}$) versus pulse count of the transmitted signal through the high threshold inverter path (NP$_{h\_th}$) for each sample at different V_{DD} values for the defect-free TSV$_0$.
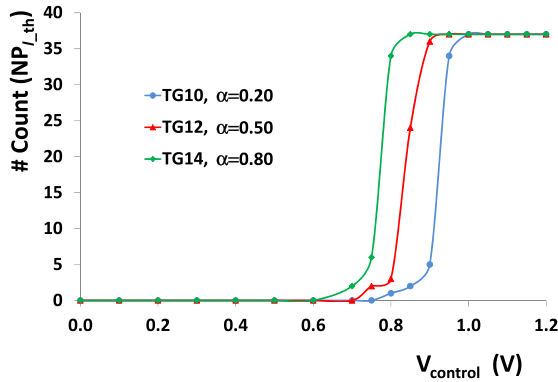

Fig. 27.   Count of the transmitted signal pulses for different locations of the defect and resistive values (chip sample #1).
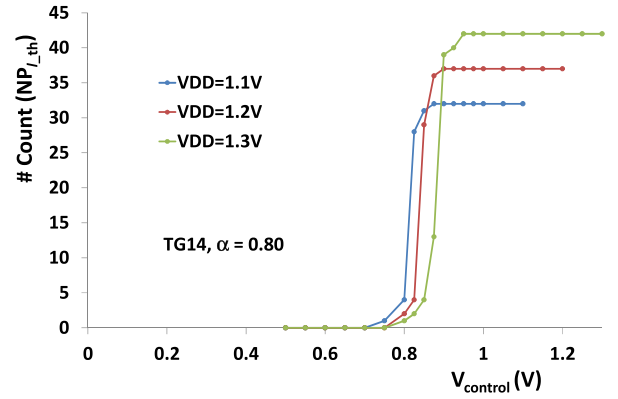

Fig. 28.   Count of the transmitted signal pulses NP$_{l\_th}$ versus $V_{control}$ and different V_{DD} for a defective TSV with a TG (chip sample #2).
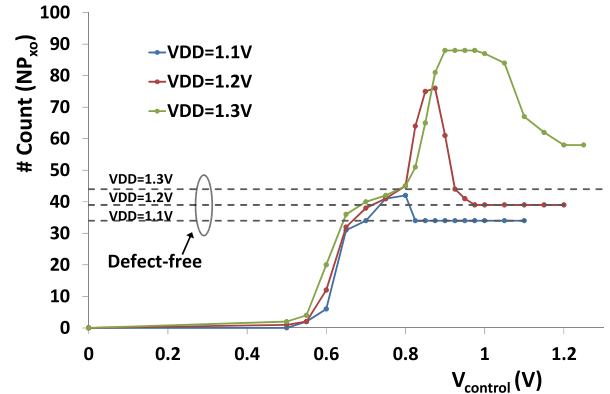

Fig. 29.   Count of the transmitted signal pulses NP$_{xo}$ versus $V_{control}$ and different V_{DD} for a defective TSV with a TG (chip sample #2).

To evaluate the effectiveness of TGs as resistive elements controllable with voltage $V_{control}$, Fig. 27 illustrates the influence of TG location on the TSV. For $V_{control}$ around V_{DD}, the equivalent resistance generated is low enough, and the number of transmitted pulses is similar to that of the defect-free case. On the contrary, for low $V_{control}$ values, the number of transmitted pulses decreases even to zero since the equivalent resistance of the TG is on the order of kΩ (according to Fig. 25). For intermediate $V_{control}$, there is a transition between both behaviors where TG location determines the range of the intermediate resistances. The closer the defect is to the RO (low α), the higher the time constant $R_{open} \cdot C_{TSV}$ since the via is more sensitive to the defect. Thus, small resistances are detected in the case of $\alpha = 0.2$ compared to $\alpha = 0.5$ or $\alpha = 0.8$ in Fig. 27.

The behavior of defective TSVs with a TG versus power voltage is shown in Fig. 28, where high V_{DD} allows the detection of small resistive defects, as presented in previous sections.

The use of count NP$_{xo}$ in the DCD helps in the detection of TSVs with low resistance defects. Fig. 29 illustrates the behavior of NP$_{xo}$ versus $V_{control}$ for different V_{DD} where the range of detected resistances improves the results obtained using NP$_{l\_th}$ (see Fig. 28). Also, high V_{DD} improves defect detection.

In Section VIII-B, experimental results for the set of defective TSVs are presented.

B. Experimental Measurements

In order to detect the defective TSV included in the circuit, the proposed technique consisting of evaluating the DC of an oscillating transmitted signal after nonsymmetrical inverters were applied. In this work, the digital DCD in Fig. 18 was used to determine the number of transmitted pulses, namely, NP$_{l\_th}$, NP$_{h\_th}$, and NP$_{xo}$.

The resistance values experimentally detected at nominal V_{DD} are shown in Fig. 30(a) depending on the defect location on the TSV. The detected defects are derived from the comparison between the number of transmitted pulses after one of the unbalanced inverters (NP$_{l\_th}$ or NP$_{h\_th}$) and the number of oscillations for the defect-free case. Note that in some cases, the same point may be indicated in Fig. 30(a) as detected (green circles) and nondetected (red squares). This is because the same resistance value was created with a fixed resistance and a modulated TG. In these cases, one of them is detected, and the other is not.

The number of transmitted pulses after a compensating delay (NP$_{xo}$ in Fig. 18) was added to improve the detection of
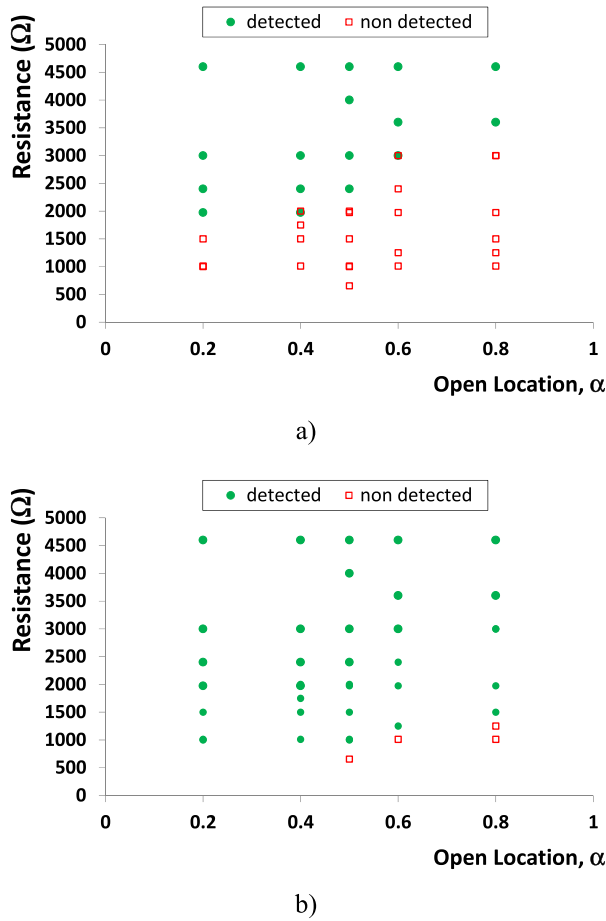
a)

b)

Fig. 30. Detected (green circles) and nondetected (red squares) experimental open resistances versus defect location at nominal $V_{DD} = 1.2$ V considering oscillation counting after (a) two unbalanced inverters NP_{l_th} or NP_{h_th} or (b) compensating delay and an XOR gate NP_{xo}.
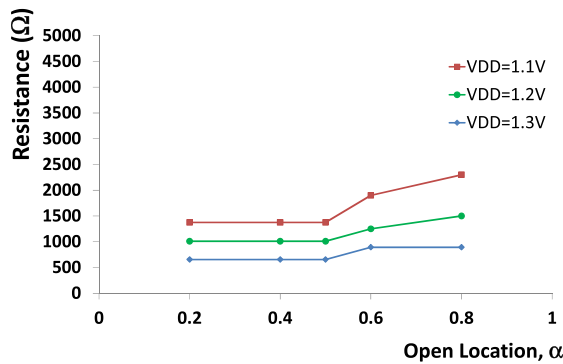

Fig. 31. Minimum experimental open resistance detected versus defect location for different power supply voltages.

resistive opens. Fig. 30(b) shows these improved results where smaller resistances are detected.

As expected from HSPICE simulations, experimental results show how open defects equal to or higher than 0.9 kΩ are detected in the first half of the TSV ($\alpha \leq 0.5$).

As stated in previous sections, lower resistive open defects can be detected by increasing V_{DD}. This was proved

experimentally by varying $V_{DD} \pm 0.1$ V with respect to the nominal value, as illustrated in Fig. 31. The higher (lower) the voltage, the lower (higher) resistance detected at a given location.

IX. CONCLUSION

A BIST technique to detect weak open defects in TSVs where the TSV under test is excited by a periodical oscillating signal and its output response is evaluated through unbalanced inverters was presented. The relationship between the DC at the output of the inverters was used for detecting weak resistive open defects. HSPICE simulations carried out with a 65-nm STMicroelectronics technology, and including process variability showed that open defect resistances on the order of 1 kΩ or higher can be detected by the proposed technique. Experimental measurements on a designed circuit with eight emulated defective TSVs and the inclusion of a digital DCD corroborate the efficiency of the proposal. Times on the order of tens of ns and an area overhead of 11.72 μm² per via are needed to evaluate each TSV.

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