# Efficient Sparse Code Multiple Access Decoder Based on Deterministic Message Passing Algorithm

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Abstract—Being an effective non-orthogonal multiple access (NOMA) technique, sparse code multiple access (SCMA) is promising for future wireless communication. Compared with orthogonal techniques, SCMA enjoys higher overloading tolerance and lower complexity because of its sparsity. In this paper, based on deterministic message passing algorithm (DMPA), algorithmic simplifications such as domain changing and probability approximation are applied for SCMA decoding. Early termination, adaptive decoding, and initial noise reduction are also employed for faster convergence and better performance. Numerical results show that the proposed optimizations benefit both decoding complexity and speed. Furthermore, efficient hardware architectures based on folding and retiming are proposed. VLSI implementation is also given in this paper. Comparison with the state-of-the-art have shown the proposed decoder's advantages in both latency and throughput (multi-Gbps).

Index Terms—Sparse code multiple access (SCMA), deterministic message passing algorithm (DMPA), folding, retiming, VLSI.

### I. INTRODUCTION

**THE** fifth generation of cellular network (5G) is put forward to meet the ever-increasing demand of wireless communication. Enabling techniques of 5G include massive multiple-input multiple-output (MIMO), advanced coding, new multiple access (MA), full spectrum access, new network architectures, etc [1]. In the past decades, MAs such as time division multiple access (TDMA) [2], frequency division multiple access (FDMA) [3], and code division multiple access (CDMA) [4], became part of wireless standards. However, those orthogonal MAs can hardly meet the 5G's capacity requirement ( $10^3$  times of LTE), due to limitations on multiplexing approaches towards physical resources [5]. According to 3GPP white book, in the enhanced Mobile Broadband (eMBB) scenario, the peak data rate should be 20 Gbps (10 to  $10^2$  times of LTE), the peak spectral efficiency should be 30 bps/Hz (3 to 5 times of LTE), and the latency should be less than 1 ms (10% of LTE) [6, 7]. Thus, ideas of non-orthogonal MA (NOMA) [8] are proposed to alleviate these bottlenecks.

#### A. Challenges for Existing NOMA

Compared to orthogonal MAs, NOMA techniques refer to those allowing multiple users overlap in time, frequency, or code domain, in other words, sharing the same physical resources [9]. NOMA is able to distinguish different users via successive interference cancellation (SIC) [10] or multiple user decoding (MUD) [11]. Besides the very first version [12], the state-of-the-art (SOA) NOMA includes multiuser shared access (MUSA) [13], pattern division multiple access (PDMA) [14], sparse code multiple access (SCMA) [15], etc. SIC was employed in [12–14] and has practical challenges:

- Computational complexity: SIC implies that each user can be decoded only when all the prior users are properly decoded. Therefore, its computational complexity scales with the in-cell user number.
- Error propagation: For SIC, if an error occurs, all users afterward are likely to be decoded incorrectly.
- Decoding latency: User power sorting is involved in SIC, and causes good overhead latency compared to other methods. Since the data with the lowest power is decoded last, the latency will even higher.

Therefore, SCMA employs MUD instead of SIC. Thanks to its sparsity, message passing algorithm (MPA) can be applied for better decoding performance.

# B. Sparse Code Multiple Access

SCMA was proposed in 2013 [15], trying to increase user scale via a new perspective: enabling more efficient multiple access by non-orthogonal sparse spreading codes of users.

1) Properties of SCMA: As a promising MA, SCMA has the properties: i) multiplexing in frequency domain; ii) codebook based on both mapping and spreading; iii) multidimensional constellation for shaping gain and spectral efficiency; iv) non-orthogonality ensuring more accessed users; v) spreading which reduces noise interference and enhances system robustness; and vi) sparsity which reduces decoding complexity. Thanks to these properties, SCMA is more physically realizable and overloading tolerant, compared to other MAs [16]. Details of SCMA can be found in Section II.

- 2) Challenges of SCMA:
- Throughput: Though the throughput of SCMA outperforms other MAs, especially orthogonal ones, it is hard to

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achieve the eMBB peak rate with acceptable complexity. Admittedly, such throughput can be achieved with a larger overloading factor, leading to prohibitive hardware complexity and performance degradation.

- Latency: On one hand, utilizing MUD, SCMA avoids the sorting latency required by SIC. On the other hand, for imperfect channels the iterative MPA tends to cost more iterations, which will counteract its latency advantage.
- Implementation: Though VLSI techniques ensure that complexity is no longer a bottleneck for SCMA implementation when the overloading factor is not extremely large, existing iterative algorithms are not hardware friendly. Second, the noise power density  $N_0$  results in large data range, leading to unbearable quantization length, or otherwise poor error performance.

# C. Relevant Prior Art

Regarding SCMA decoding, existing literature mainly focus on three aspects: i) stochastic computing, ii) tree structure approximation, and iii) efficient hardware implementation.

1) Stochastic Computing: In [17], a stochastic MPA (SMPA) decoder was proposed, where beliefs are given by weights of bit streams. Multiplication and addition are implemented by AND and MUX, respectively. Though it work effectively reduces the complexity per iteration, problems are:

- Accuracy: Stochastic computing suffers from low accuracy, due to randomness loss. Beliefs in MPA usually require precision of 10<sup>-5</sup>, which length-limited could not give. Performance degradation is observed.
- Latency: For SMPA, the calculation of a single value requires a large number (10<sup>5</sup> to 10<sup>6</sup>) of bit-level operations. Considerable iterations make the latency even larger and not suitable for practice.
- Complexity: Though SMPA helps to reduce hardware of a single operation, the amount of bit-operations in one decoding is around 10<sup>7</sup>. Thus, the total complexity may be even larger than deterministic MPA (DMPA).

A VLSI architecture of SMPA was discussed in [18]. The throughput for a 6-user decoder is 57 Mbps and far from 3GPP requirements. Though the hardware cost is low, the latency is not suitable for eMBB.

2) Tree Structure Approximation: In [19], a pruned tree approximation was proposed. The decoder accurately represents values with high probabilities, whereas approximates ones with low probabilities [20]. Squares are replaced by additions, multiplications, and comparisons. Though complexity is expected to reduce, search breadth must be larger than 2 for performance, which increases the complexity again.

3) Efficient Hardware Architecture: In [21], a stage-level folded architecture for DMPA was proposed with consideration of both speed and efficiency, which is our prior work. However, only theoretical analysis and simple architecture were given. The real VLSI implementation is missing.

#### D. Contributions

This paper emphasises on iteration reduction, convergence speedup, computation simplification, and implementation of SCMA decoder. Compared to SOA, our contributions are:

- We propose early termination scheme based on the convergence behavior of DMPA, which significantly reduces the required iteration number.
- We propose adaptive decoder, which adjusts beliefs according to the variation trend, accelerates the convergence, and compensates the performance loss. Results show that it outperforms the ones in [17, 18] in terms of latency and throughput, satisfying the 3GPP requirements.
- We perform numerical analysis for conditional probability approximation (over 60% computation is for conditional probabilities in MPA) in *Initialization*, which is squarefree and division-free, and suffers from little performance loss. Computational complexity and hardware implementation have been greatly benefitted.
- We propose distributed matrix scheme for prior noise reduction of DMPA decoder, which compensates the approximation loss with negligible extra complexity.
- We improve our stage-level folded decoder with the proposed algorithms, achieve higher hardware efficiency with eMBB requirements on throughput and latency.
- We implement the proposed DMPA decoder on Xilinx Virtex-7 XC7VX690T FPGA to demonstrate its advantages for real applications.

#### E. Notations

Lowercase and uppercase boldface letters designate column vectors and matrices, respectively. Matrix **A**'s transpose and conjugate are  $\mathbf{A}^T$  and  $\mathbf{A}^H$ . The  $M \times M$  identity matrix is  $\mathbf{I}_M$  and the  $M \times N$  all-zeros matrix is  $\mathbf{0}_{M \times N}$ . Sets are denoted by uppercase calligraphic letters  $\mathcal{A}$ , with cardinality  $|\mathcal{A}|$ .

# F. Paper Outline

The remainder of this paper is organized as follows. Section II reviews the preliminaries of SCMA. DMPA and its optimized versions are discussed in Section III. Numerical results and analysis are given in Section IV. Hardware architecture is described in Section V. VLSI implementation is given in Section VI. Section VII concludes the entire paper.

# **II. PRELIMINARIES**

Preliminaries of SCMA are given in this section. A 6-user system in Fig. 1 is used as a running example.

# A. SCMA Encoder

Suppose codeword set, constellation set, and information set are  $\mathcal{X}$ ,  $\mathcal{C}$ , and  $\mathcal{B}$ , respectively. Define  $\mathbf{x} \in \mathcal{X}$ ,  $\mathbf{c} \in \mathcal{C}$ , and  $\mathbf{b} \in \mathcal{B}$ .  $|\mathcal{B}| = M$ ,  $|\mathcal{X}| = K$ , and  $|\mathcal{C}| = N$ . The SCMA encoding is given by two rounds of mapping [15]. The first round of mapping is:

$$g: \mathcal{B} \to \mathcal{C}, \ \mathbf{c} = g(\mathbf{b}),$$
 (1)

where  $\mathcal{B} \subset \mathbb{B}^{\log_2 M}$ ,  $\mathcal{C} \subset \mathbb{C}^N$ , and g is a constellation mapping function. The second round of mapping is:

$$\mathbf{V}: \ \mathcal{C} \to \mathcal{X}, \ \mathbf{x} = \mathbf{V}\mathbf{c}, \tag{2}$$



Fig. 1. A 6-user SCMA system.

where  $\mathcal{X} \subset \mathbb{C}^{K}$ , and  $\mathbf{V} \in \mathbb{B}^{K \times N}$  is the mapping matrix.

Suppose the entire mapping function of SCMA encoding is f. Then we have

$$f: \mathcal{B} \to \mathcal{X}, \ \mathbf{x} = f(\mathbf{b}), \ f = \mathbf{V}g.$$
 (3)

An *M*-size SCMA codebook consisting of *K* complex values is constructed. Note that **V** contains (K - N) all-zero rows. Mapping matrix is generated by inserting (K - N) all-zero rows into an  $N \times N$  identity matrix  $\mathbf{I}_N$  randomly. So when the SCMA system is regular, it supports  $C_K^N = C_K^{K-N}$  different layers (users).

#### B. SCMA Multiplexing

Consider a *K*-dimensional SCMA encoder with *J* separated layers. Each layer is defined by  $(\mathbf{V}_j, \mathbf{g}_j, \mathbf{M}_j, \mathbf{N}_j)$ , where j = 1, ..., J. If  $i \neq j$ ,  $\mathbf{V}_i \neq \mathbf{V}_j$  and  $\mathbf{g}_i \neq \mathbf{g}_j$ , in order to distinguish one layer from another. In general,  $\mathbf{M}_j$  and  $\mathbf{N}_j$ can be either the same or different for different layers. Without loss of generality, for  $\forall j$  we set  $\mathbf{M}_j = M$ ,  $\mathbf{N}_j = N$ .

We call this SCMA system semi-regular because J is not necessarily  $C_K^N$  (The regular system will be discussed later). The SCMA codewords are multiplexed over K shared orthogonal resources, e.g. OFDMA tones or MIMO spatial layers [16]. With this semi-regular system, the received signal after synchronous layer multiplexing can be expressed as

$$\mathbf{y} = \sum_{j=1}^{J} diag(\mathbf{h}_j) \mathbf{x}_j + \mathbf{n},\tag{4}$$

where  $\mathbf{h}_j$  and  $\mathbf{x}_j$  are the *K*-dimensional channel vector and SCMA codeword of layer *j*. Suppose signals of all layers are from the same transmit point, for a specific receiver, the channel vectors of all layers are identical that for  $\forall j$ ,  $\mathbf{h}_j = \mathbf{h}$ . Now Eq. (4) reduces to

$$\mathbf{y} = diag(\mathbf{h})\Sigma_{j=1}^{J}\mathbf{x}_{j} + \mathbf{n}.$$
 (5)

Define overloading factor as  $\lambda = J/K$ , which indicates the overloading tolerance or access ability of a SCMA system. Fig. 2 illustrates a 6-user SCMA multiplexing.



Fig. 2. SCMA multiplexing example.

#### C. Factor Graph Representation

Define the binary indicator vector as  $\mathbf{f}_j = diag(\mathbf{V}_j \mathbf{V}_j^T)$ . Then the factor graph matrix is  $\mathbf{F} = (\mathbf{f}_1, ..., \mathbf{f}_J)$ . Then the factor graph representation can be obtained like how we do with LDPC codes. Each column of  $\mathbf{F}$  associates a layer node, and each row a resource node. Degree of each resource node is defined as  $\mathbf{d}_f = (d_{f1}, ..., d_{fK})^T = \sum_{j=1}^J \mathbf{f}_j$ . For more details, please refer to [15].

Take K = 4 and N = 2 as an example. The factor graph is in Fig. 3 and  $J = C_4^2 = 6$ . Degree  $\mathbf{d}_f = (d_{f1}, ..., d_{fK})^T = (3, 3, 3, 3, 3, 3)^T$  and the overloading factor  $\lambda = J/K = 1.5$ . The  $4 \times 6$  factor graph matrix of this system is in Eq. (6).



Fig. 3. Factor graph representation of an SCMA with K = 4 and J = 6.

$$\mathbf{F} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix}$$
(6)

#### III. OPTIMIZATIONS ON SCMA DECODING

#### A. Regular Form of SCMA

Regular SCMA refers to the absolute-regular form [22, 23], where number of layers J equals to  $C_K^N$ . In other words, it employs all the available layers (users). Eq. (6) is an example of regular form. The definition is as follows.

**Definition 1.** SCMA with K complex-dimension and weight of N which satisfies the following requirements is called regular (absolute-regular) SCMA.

Requirement 1: Owning  $J = C_K^N$  layers (users) in total. Requirement 2: The columns of factor graph matrix must be listed in the sequential permutation order, with weight  $\lambda$ .

#### B. DMPA Decoding

The DMPA decoding for SCMA mainly includes 4 steps.

1) Initialization: Calculate conditional probability with extrinsic information to get prepared for the belief propagation.

$$P_k(y_k|x_{k,1}, x_{k,2}, x_{k,3}, N_0) = e^{-\|y_k - (x_{k,1} + x_{k,2} + x_{k,3})\|^2 / N_0},$$
(7)

where  $y_k$  denotes the k-th bit of the received signal y.  $x_{k,1}$ ,  $x_{k,2}$ , and  $x_{k,3}$  denote overlapped bits of the 3 layers which are connected to the k-th resource node separately, and  $N_0$  is the noise power density.

2) *Resource Node Updating:* The updating formulation of resource node is in the sum-product form which is an approximation of marginal probability:

$$I_{R_k \to L_1}(m_1) = \sum_{m_2=1}^M \sum_{m_3=1}^M P_k I_{L_2 \to R_k}(m_2) I_{L_3 \to R_k}(m_3), \quad (8)$$

$$I_{R_k \to L_2}(m_2) = \sum_{m_1=1}^{M} \sum_{m_3=1}^{M} P_k I_{L_1 \to R_k}(m_1) I_{L_3 \to R_k}(m_3), \quad (9)$$

$$I_{R_k \to L_3}(m_3) = \sum_{m_1=1}^{M} \sum_{m_2=1}^{M} P_k I_{L_1 \to R_k}(m_1) I_{L_2 \to R_k}(m_2), \quad (10)$$

where  $R_k$  is the k-th resource node,  $m_{1,2,3} = 1, ..., M$  are transmitted symbols.  $I_{R_k \to L_{1,2,3}}$  denotes the belief propagated to the k-th resource node from the neighboring layer nodes.  $I_{L_{1,2,3} \to R_k}$  is the belief passing in the opposite direction.

3) Layer Node Updating: The normalization makes sure belief falls in [0, 1].

$$I_{L_j \to R_1}(m) = normalize(I_{R_2 \to L_j}(m)), \qquad (11)$$

$$I_{L_j \to R_2}(m) = normalize(I_{R_1 \to L_j}(m)), \qquad (12)$$

where m = 1, ..., M corresponds different symbols.

4) Probability Calculating and Symbol Judging: After iterations, the final probability of each symbol is

$$Q_{L_j}(m) = I_{R_1 \to L_j}(m) \cdot I_{R_2 \to L_j}(m).$$
(13)

where  $L_j$  denotes the *j*-th layer. The symbol with the highest probability becomes the estimated symbol  $\hat{l}$  for each layer.

# C. Max-Log Algorithm

Decoder in probability domain suffers from huge complexity and relatively high latency. Therefore, its Max-Log version is considered [24] with the Jacobi's logarithm formula [25]:

$$\log\left(\sum_{i=1}^{N} \exp(f_i)\right) \approx \max_{i=1,...,N} \{f_1, f_2, ..., f_N\}.$$
 (14)

Updating steps now become:

1) Initialization:

$$P_k^{\log}(y_k|x_{k,1}, x_{k,2}, x_{k,3}, N_0) = -\frac{1}{N_0} \parallel y_k - (x_{k,1} + x_{k,2} + x_{k,3}) \parallel^2,$$
(15)

2) Resource Node Updating:

$$I_{R_k \to L_1}^{\log}(m_1) = \max\left\{P_k^{\log} + I_{L_2 \to R_k}^{\log}(m_2) + I_{L_3 \to R_k}^{\log}(m_3)\right\}, (16)$$

$$I_{R_k \to L_2}^{\log}(m_2) = \max\left\{ P_k^{\log} + I_{L_1 \to R_k}^{\log}(m_1) + I_{L_3 \to R_k}^{\log}(m_3) \right\}, \quad (17)$$

$$I_{R_k \to L_3}^{\log}(m_3) = \max\left\{P_k^{\log} + I_{L_1 \to R_k}^{\log}(m_1) + I_{L_2 \to R_k}^{\log}(m_2)\right\},$$
(18)

3) Layer Node Updating:

$$I_{L_j \to R_1}^{\log}(m) = I_{R_2 \to L_j}^{\log}(m),$$
(19)

$$I_{L_j \to R_2}^{\log}(m) = I_{R_1 \to L_j}^{\log}(m),$$
(20)

4) Probability Calculating and Symbol Judging:

$$Q_{L_j}^{\log}(m) = I_{R_1 \to L_j}^{\log}(m) + I_{R_2 \to L_j}^{\log}(m).$$
(21)

# D. Early Termination

Early termination is based on the belief judgement for each layer node and resource node [26]. Our judgement steps are:

- 1) Create a zero-matrix to record the stability condition of beliefs, which denotes all the beliefs are unstable.
- 2) Judge the stability of all beliefs per iteration. If  $\left|\frac{V-V_{\text{temp}}}{V_{\text{temp}}}\right| \leq \epsilon, (\epsilon > 0)$ , the beliefs are stable, and the corresponding value in the matrix is set as "1".
- 3) When the stability matrix become a all-ones matrix, beliefs of all layer nodes and resource nodes are stable, and the convergence is achieved. Then, the iterative decoding terminates.

Here,  $V_{\text{temp}}$  and V are the belief values in the previous and present iteration, respectively.  $\epsilon$  is a judgment constant. The DMPA with early termination is shown in Alg. 1. The Max-Log version is similar and omitted.

Algorithm 1 DMPA with Early Termination						
<b>Input:</b> y, $I_{\max}$ , and $\epsilon$						
1: Iteration:						
2: <b>for</b> $t = 1 : I_{\max}$						
3: Set stability matrix $\mathbf{S} = 0$						
4: Update beliefs $V$						
5: <b>for</b> $j = 1 : N$						
6: $temp = \left  V_i^{(t)} - V_i^{(t-1)} / V_i^{(t-1)} \right $						
7: <b>if</b> $temp \leq \epsilon$						
8: $S_j = 1$						
9: end if						
10: <b>end for</b>						
11: <b>if</b> $\mathbf{S} = 1$						
12: break						
13: <b>end if</b>						
14: end for						
15: Judgement <sup>early</sup> :						
16: Compute beliefs						
17: Decide $\hat{\mathbf{u}}$						
<b>Output:</b> $\hat{\mathbf{u}} = \{\hat{u}_1, \hat{u}_2,, \hat{u}_6\}$						

#### E. Self-Adaption Algorithm

Self-adaption [27, 28] is also based on stability judgement. Compared to the one in early termination, the judgement in self-adaption requires an extra step between 2) and 3):

"Forecast and adjust the belief of next iteration based on the convergence trend. If  $\frac{V-V_{\text{temp}}}{V_{\text{temp}}} \ge \epsilon$ ,  $V \Leftarrow \alpha V$  with  $\alpha > 1$ , since the convergence trend makes values larger. Otherwise, if  $\frac{V-V_{\text{temp}}}{V_{\text{temp}}} \le -\epsilon$ ,  $V \Leftarrow \beta V$  with  $\beta < 1$ ."

Now the DMPA with self-adaption is shown in Alg. 2. The Max-Log version is omitted.

## Algorithm 2 DMPA with Self-Adaption

	1
Input: y, $I_{max}$ , and	$l \epsilon$
1: Iteration:	
2: <b>for</b> $t = 1 : I_n$	nax
3: Set stabili	ty matrix $\mathbf{S} = 0$
4: Update be	liefs V
5: <b>for</b> $j = 1$	: N
6: $temp$ :	$=V_{i}^{(t)}-V_{i}^{(t-1)}/V_{i}^{(t-1)}$
7: <b>if</b> <i>tem</i>	$p \ge \epsilon$
8: $V_i^{(t)}$	$\leftarrow \alpha \cdot V_i^{(t)}$
9: elseif	$temp \leq -\epsilon$
10: $V_i^{(t)}$	$\leftarrow \beta \cdot V_i^{(t)}$
11: <b>else</b>	, j
12: $S_i =$	= 1
13: end if	
14: end for	
15: <b>if</b> $S = 1$	
16: break	
17: end if	
18: end for	
19: Judgement <sup>adapt</sup>	•
20: Compute beli	efs
21: Decide û	
<b>Output:</b> $\hat{\bf{u}} = \{\hat{u}_1, \hat{u}\}$	$\hat{u}_2,,\hat{u}_6\}$



Fig. 4. Procedure of initial noise reduction.

# F. Initial Noise Reduction

"Distributed matrix" **D** is to reduce random error, enhance accuracy of initial value [29], and speed up the convergence.

For the SCMA system in Fig. 4, we have the overlapped signals: a, b, c, and d after multiplexing. Random error of these signals can be either positive or negative, which depends on the environment noise. Therefore, we can regroup signals and assign them to 4 resource nodes. At the receiver, we can first recover the original signals according to the inverse of "distributed matrix" and then start the decoding. Compared to original transmitting scheme, each signal of specific resource node has a great chance to be added with both positive and negative random noises, which increases the accuracy of initial value. It is noted that **D** is not constant and can be adjusted according to the codebook and channel condition.

# G. Initial Probability Approximation

Discussed above, the calculation of initial probability results in high computational complexity, which is obvious in Max-Log decoding. Thus, suitable approximations in Initialization are expected to improve calculation efficiency and reduce latency with little performance loss. For SCMA decoding, the purpose of iterative updating is to find the symbol with the largest probability. Hence, the absolute value is not that critical to make a decision. We can still ensure the detection correctness even with relative beliefs. The relative magnitude is determined by the initial probability and the initial value of different users in Initialization. Now, we carry out the approximation in steps: i) simplify the initial probability calculation by reducing operations with large complexity; ii) adjust the initial value of different users according to the relative magnitude determined by initial probabilities; iii) update beliefs iteratively based on the relative values. The formulae of initial probabilities in DMPA become:

$$P_k(y_k|x_{k,1}, x_{k,2}, x_{k,3}, N_0) = e^{-\|y_k - (x_{k,1} + x_{k,2} + x_{k,3})\|^2/N_0},$$
(22)

For square and division, which are of higher complexity, DMPA approximations 1 to 3 are proposed:

 $P_k(y_k|x_{k,1}, x_{k,2}, x_{k,3}, N_0) = e^{-\|y_k - (x_{k,1} + x_{k,2} + x_{k,3})\|/N_0},$ (23)

$$P_k(y_k|x_{k,1}, x_{k,2}, x_{k,3}, N_0) = e^{-\|y_k - (x_{k,1} + x_{k,2} + x_{k,3})\|^2},$$
(24)

$$P_k(y_k|x_{k,1}, x_{k,2}, x_{k,3}, N_0) = e^{-\|y_k - (x_{k,1} + x_{k,2} + x_{k,3})\|},$$
(25)

Similarly, we have Max-Log approximations 1 to 3 as follows.

$$P_k^{\log}(y_k|x_{k,1}, x_{k,2}, x_{k,3}, N_0) = -\frac{1}{N_0} \| y_k - (x_{k,1} + x_{k,2} + x_{k,3}) \|, (26)$$

$$P_k^{\log}(y_k|x_{k,1}, x_{k,2}, x_{k,3}, N_0) = - \parallel y_k - (x_{k,1} + x_{k,2} + x_{k,3}) \parallel^2,$$
(27)

$$P_k^{\log}(y_k|x_{k,1}, x_{k,2}, x_{k,3}, N_0) = - \| y_k - (x_{k,1} + x_{k,2} + x_{k,3}) \|, \quad (28)$$

Analysis below will show these approximations have different effects on error performance and computational complexity.

#### IV. RESULTS AND ANALYSIS

### A. Error-Rate Performance

The 6-user SCMA system is simulated. Additional white Gaussian noise (AWGN) is assumed. The maximum iteration number is 5. Results are give in Fig. 5.

Fig. 5(a) shows the BLER performance of DMPA algorithm with different approximations, different iterations, early termination, self-adaption, and initial noise reduction. Fig. 5(b) shows the curves of Max-Log algorithm. According to Fig. 5, we see

- DMPA/Max-Log with more iterations enjoys better performance, but the improvement is limited when iteration number is sufficiently large. Shown by numerical results, DMPA/Max-Log with 3 iterations is a good choice in real implementation.
- 2) The average iteration number of early termination or adaptive scheme is around 3, but the performance is similar DMPA with 5 iterations. Results with different parameters reveal that self-adaption performs better in



(b) Error-rate performance of Max-Log with different approximation.

Fig. 5. Error-rate performance of SCMA with different detecting methods.

high SNR. Thus, the adjusting factor in self-adaption is supposed to be smaller at higher SNR.

3) DMPA and Max-Log have similar performance without approximation. However, since DMPA heavily depends on  $N_0$ , approximations without precise  $N_0$  will cause unbearable performance loss. On the other hand, Max-Log algorithm is not sensitive to  $N_0$ , and its approximations without exact  $N_0$  can still achieve good performance. Therefore, Max-Log is preferred.

Now, we figure out that suitable configurations for hardware implementation are: i) Max-Log approach; ii) 3 iterations; iii) early termination and self-adaption; iv) Approximation 2 or 3, and v) initial noise reduction.

# B. Computational Complexity

Suppose the symbol set size for each user is M, the number of physical resources is N, the user number is K, and the maximum iteration number is I. Then, we summarize the computational complexity of different decoding methods in Table I. Compared with other methods, the proposed method has the lowest computational complexity, while maintaining the error performance. In fact, the proposed method is similar to Max-Log, but has lower complexity in Initialization due to the approximation. For a real system, M and N are usually large, the number of multiplications and divisions will makes other methods not suitable for implementation. However, as discussed above, the proposed algorithm is multiplication/division-free with Approximation 3. Therefore, it can intensively improve the computational efficiency and reduce the latency, making it more applicable for hardware implementation in Section VI. The VLSI implementation results in Table IV will further verify that the proposed decoder's hardware efficiency over the SOA design.

# C. Performance/Complexity Trade-Off Analysis

Fig. 6 illustrates the trade-off between error performance and computational complexity of proposed methods. The minimum required SNR to achieve 1% BER is employed as a metric. The complexity is given by Timing (TM) complexity, which is in term of iteration number. Fig. 6 shows the trade-off of DMPA with approximations. It is clear that Max-Log with Approximation 3 provides the best performance/complexity trade-off.



Fig. 6. Performance/complexity trade-off analysis of DMPA algorithm.

#### V. HARDWARE ARCHITECTURE

The hardware architecture of the Max-Log DMPA is discussed. Timing optimization and folding technique are introduced for higer efficiency.

#### A. Overall Architecture

The overall architecture is shown in Fig. 7. It has 4 units and 2 memory networks, which are RN-to-LN and LN-to-RN networks for  $I_{R\to L}$  and  $I_{L\to R}$ , respectively. The elementary units are *Initialization Unit*, *Resource Node Update Unit*, *Layer Node Update Unit*, and *Probability Calculating Unit*, which execute steps indicated by Eq. (15) to Eq. (21), respectively. The iterative calculation is done by *Resource Node* 

	b DMPA [21]	Max-Log [30]	Drupod DMDA [21]
Procedure Uneration This woi			FILLIEU DMPA [51]
The operation This wor	[APCCAS '17]	[China Comm. Dec. '15]	[DSP '16]
Initial probability ADD $2M^3N/$	$T_{\rm adp} = 3M^3N/T_{\rm MPA}$	$3M^3N/T_{\text{Max-Log}}$	$3M^3N/T_{\rm tree}$
miliar probability multip MUL 0	$3M^3N/T_{\rm MPA}$	$3M^3N/T_{\text{Max-Log}}$	$3M^3N/T_{\rm tree}$
EXP 0	$M^3 N/T_{\rm MPA}$	0	$M^3 N/T_{\rm tree}$
ADD $2 \cdot 3M^3$	$N = 3M^3N$	$2 \cdot 3M^3N$	$3M^3N$
MUL 0	$2 \cdot 3M^3N$	0	$2 \cdot 3M^3N$
MAX $3M^3N$	0	$3M^3N$	0
ADD 0	2MK	0	2MK
undeting MUL 0	2MK	0	2MK
SWOP $2MK$	2MK	2MK	2MK
ADD MK	0	MK	0
iudgement MUL 0	MK	0	MK
MAX 0	MK	0	MK

 TABLE I

 COMPARISON OF COMPUTATIONAL COMPLEXITY FOR DIFFERENT DECODING ALGORITHMS



Fig. 7. Overall architecture of DMPA.

*Update Unit* and *Layer Node Update Unit*, both of which could not start current propagation unless all previous data have been calculated. We call this data updating interval a "step". Optimization details of this scheduling will be discussed below.

## B. Stage-Level Scheduling Optimization



Fig. 8. Stage-level scheduling.

The proposed stage-level scheduling is a finer-grained optimization over the step-level scheduling. With this stagelevel scheduling, it is convenient to insert deep pipelines to achieve a higher throughput [32–34]. Compared with steplevel scheduling, updating of stage-level scheduling does not have to wait for the completion of data computation from the previous unit, which therefore avoids low hardwareefficiency and long processing-latency. In sum, stage-level scheduling enjoys faster processing speed and higher hardware efficiency than the step-level one. Fig. 8 shows the stage-level scheduling. It details each computing step to achieve a deeper pipelined structure.

# C. Folding

The architecture of stage-level DMPA turns out to be very complicated in form of data factor graph (DFG). To achieve an efficient architecture, folding technique is employed for further optimization. Since folding operation based on fine-grained architecture is difficult to be carried out, a folding scheme based on unit is considered. Fig.s 13 and 14 in appendix shows the entire step- and stage-level algorithms, respectively. Due to the page constraint, we only take a branch of *Initialization Unit*, which is fully-paralleled in DFG, as an example to show proposed folding details. Folding transform of other units can be conducted in the similar fashion. The DFG of the branch in *Initialization Unit* is shown in Fig. 9.



Fig. 9. Original hardware of Step 1 before folding.

The folding includes 3 steps: i) construct folding sets and folding equations, ii) analysis life span, and iii) allocate registers. More details of this method are explained by [35].

1) Folding Sets and Folding Equations: Set the folding factor to 7, we can obtain the following folding sets:

$$\begin{cases} S_{in} = \{1, 2, \phi, \phi, \phi, \phi, \phi\}, \\ S_A = \{3, 4, 5, 6, 7, 8, 9\}, \\ S_M = \{10, 11, 12, \phi, \phi, \phi, \phi\}, \end{cases}$$
(29)

where  $S_{in}$ ,  $S_A$ , and  $S_M$  denote the folding sets for inputs, adders, and multipliers, respectively.

Then, folding equations can be derived based on the given folding sets

$$\begin{cases} D_F(1 \to 3) = 0, D_F(3 \to 4) = 7, D_F(4 \to 5) = 7, \\ D_F(2 \to 7) = 3, D_F(7 \to 8) = 7, D_F(8 \to 9) = 7, \\ D_F(5 \to 10) = 4, D_F(10 \to 6) = 8, D_F(6 \to 11) = 4, \\ D_F(9 \to 12) = 2, D_F(12 \to 6) = 6, \end{cases}$$
(30)

where  $D_F(x \to y)$  denotes the number of delays on the path from x to y.



Fig. 10. Life time figure.

2) Life Time Analysis: Life span analysis is demonstrated in the form of life time figure as shown in Fig. 10. It is achieved from folding equations. One thick line in the figure represents survival time of certain data. Activated number shows number of data in use at the moment [36]. According to Fig. 10, we see that this folding architecture requires at least 8 registers.

*3) Register Allocation:* The forward-backward scheme of register allocation is employed based on life span analysis [37]. The specific allocation process is displayed in Fig. 11.

Cycle	Input	$R_1$	$R_2$	$R_3$	$R_4$	$R_5$	$R_6$	$R_7$	$R_8$	Output
0										
1	$n_{2}, n_{3}$									
2	$n_4, n_{10}$	<i>n</i> <sub>3</sub>	$n_2$							
3	$n_5$		$n_3$	$n_2$	$n_4$	<i>n</i> <sub>10</sub>				
4	$n_{6}, n_{12}$	$n_5$		<i>n</i> <sub>3</sub>	$\binom{n_2}{n_2}$	$n_4$	<i>n</i> <sub>10</sub>			<i>n</i> <sub>2</sub>
5	<i>n</i> <sub>7</sub>	<i>n</i> <sub>12</sub>	$n_5$	$n_6$	$n_3$		$n_4$	<i>n</i> <sub>10</sub>		
6	$n_8$	$n_7$	<i>n</i> <sub>12</sub>	$n_5$	$n_6$	<i>n</i> <sub>3</sub>		$n_4$	<i>n</i> <sub>10</sub>	
7	$n_9$	$n_8$	$n_7$	<i>n</i> <sub>12</sub>	$(n_5)$	$n_6$	$n_3$	<i>n</i> <sub>10</sub>	$n_4$	<i>n</i> <sub>5</sub>
8		$n_9$	$n_8$	$n_7$	<i>n</i> <sub>12</sub>	$n_4$	$(n_6)$	n <sub>3</sub>	$n_{10}$	$n_{3}, n_{6}$
9			$(n_9)$	n <sub>8</sub>	$n_{\gamma}$	n <sub>12</sub>	$\binom{n_4}{1}$	( <i>n</i> <sub>10</sub> )		$n_{4}, n_{9}$
10					$n_8$	$n_{\gamma}$	(n <sub>12</sub> )	<	$n_{10}$	$n_{10}$ , $n_{12}$
11						$n_8$	$n_{\gamma}$			
12							$n_8$	$(n_{\gamma})$		$n_7$
13								$(n_8)$		n <sub>8</sub>

Fig. 11. Register allocation table of folding architecture.

After all the steps, we can finally obtain the folded architecture of the branch in *Initialization Unit*.

#### D. Hardware Architecture and Loop Analysis

The final stage-level folded architecture of DMPA, which is illustrated at module-level in Fig. 12. Lower hardware cost and reasonable processing speed become its main advantages.

The loop bound analysis [38, 39] of this folded architecture is also given here. Suppose the processing time of an adder, a



Fig. 12. Hardware architecture of DMPA.

TABLE II Cost of Different Architectures for "J = 6"

Different architectures	Cycles	Hardware cost (main untis)			
		Adders (Comparators)	Multipliers		
Original	80	52	12		
Stage-level folded	300	4	2		

comparator, and a swopper are  $T_A, T_C$ , and  $T_S$ , respectively. We can obtain the results listed by Table III.

TABLE III Loop Bound Analysis

Loop	ADD	CMP	SWOP	Delay	Loop bound
1	1	1	0	3	$(T_A + T_C)/3$
2	2	1	0	4	$(2T_A + T_C)/4$
3	1	1	1	4	$(T_A + T_C + T_S)/4$
4	2	1	1	5	$(2T_A + T_C + T_S)/5$

Thus, the iteration bound is calculated as follows:

$$T_{\infty} = \max\left\{\frac{T_A + T_C}{3}, \frac{2T_A + T_C}{4}, \frac{T_A + T_C + T_S}{4}, \frac{2T_A + T_C + T_S}{5}\right\} (31)$$

# VI. VLSI IMPLEMENTATION

The proposed decoder's VLSI implementation is given and compared to two SOA baselines. The first is the DMPA decoder [21], and the second is the SMPA decoder [18]. As both baselines do not consider folding, the proposed decoder does not either for fair comparison. But if all designs are folded, the proposed decoder's advantages remain. Discussed previously, the proposed decoder is based on: i) Max-Log approach; ii) early termination and self-adaption; iii) Approximation 3, and iv) initial noise reduction. Since the SMPA decoder employed 5 iterations, 1 up to 5 iterations are considered, though 3 turns out to be efficient per our analysis. Both the proposed decoder and DMPA decoder are implemented with Xilinx Virtex-7 XC7VX690T FPGA. The results of SMPA decoder is scribed from [18], since it is implemented with ASIC. The frequency is 500 MHz. The input quantization is 8-bit for both real and imaginary parts, and the intermediate quantization is 16.

## A. Module Details of Proposed Decoder

The proposed decoder consists of four basic parts as shown in Fig. 7: initialization module, layer node updating network, resource node updating network, and symbol judging module. The design details are presented as follows.

1) Initialization Module: It calculates initial belief of each user with the received signal and inner codebook. The received signal is made up of 4 complex resource nodes, thus the input is 8-parallel. Each of them has the quantization length of 8. It is noted that the output belief has the quantization length of 16, due to multiplication. The codebook is restored in memories, which costs 96 memory blocks of 8-bit length each. 2) Resource Node Updating Network: It calculates the sum of belief and outputs the largest, based on the approximated Jacobi's formula. It is made up of resource node updating units, where the input data are initial beliefs and layer node beliefs, and the output data are the 4 resource node beliefs. The largest value is selected from 16 intermediate beliefs, in 3 steps of comparison with 14 buffers. Thus, 56 buffers are required by each unit, and 672 by the entire network.

3) Layer Node Updating Network: It is made up of layer node updating units, which normalize the input value and swop it by the inner connection. In each unit, the input data are resource node beliefs only, and the output data are the corresponding 4 layer node beliefs. Four 16-bit dividers are required per unit with 28 clocks' delay. Hence, the whole network needs 48 dividers. Besides, layer node beliefs would also be reset at the start of each frame of the received signals in layer node updating network.

4) Symbol Judging Module: It finds the largest belief and maps it to original source code according to the codebook of each user. Also, this module consists of 6 smaller judging units, which perform the basic function for each user. In each unit, 4 beliefs are compared with each other. Thus 2 steps of comparison and 3 buffers are required. Then, the entire module needs 18 buffers.

The implementation comparison with the DMPA decoder is listed in Table IV. It shows the proposed decoder's advantages in both complexity and throughput, thanks to the log-domain processing and approximation approaches.

TABLE IV FPGA RESULTS FOR DIFFERENT DECODERS WITH J/K = 6/4

SCMA decoders	DMPA decoder [21]	This work
LUTs	139,205~(36%)	82,909 (19%)
Registers	248,217 (28%)	109,997~(12%)
LUT-FF pairs	103, 127 (36%)	52,203 (18%)
DSP48E1s	436 (12%)	436 (12%)
Maximum frequency	167.6 MHz	359.1 MHz

Since speed is the main focus of our design, comparison results of throughput and latency with baselines are shown in Table V, where "L" for latency and "T" for throughput. As we can see from the table, the proposed SCMA decoder outperforms the SOA in both throughput and latency, and also meets the multi-Gbps and millisecond requirements of 3GPP. Though, SMPA decoder has complexity advantage, the proposed decoder's complexity can be further reduced with folding techniques.

# VII. CONCLUSION

In this paper, simplifications such as log-domain calculation and probability approximation have been introduced to lower the complexity of SCMA's DMPA decoder. Early termination, adaptive decoding, and initial noise reduction are also proposed for faster convergence and better performance. Hardware optimizations with folding and retiming are introduced. VLSI implementation results have confirmed the advantages of the proposed SCMA decoder for high-speed applications over the SOA designs. Future research will be directed towards further improvements on both algorithm and implementation.

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TABLE VLatency (L) in [ $\mu$ s] and Throughput (T) in [Mb/s] for Different Decoders (Frequency: 500 MHz)

User $\#(J)$	6	12	24	48	96	192		
Resource $\#(K)$	4	8	16	32	64	128		
Iteration # $(I_{max})$	L / T	L / T	L / T	L / T	L / T	L / T		
This work								
1	3.50 / 857.14	3.70 / 1628.57	3.96 / 3012.85	4.26 / 5423.13	4.58 / 9490.48	4.95 / 16133.81		
2	5.50 / 547.69	5.84 / 1040.62	6.22 / 1925.14	6.66 / 3465.25	7.16 / 6064.20	7.74 / 10309.14		
3	8.62 / 349.96	9.14 / 664.93	9.74 / 1230.12	10.42 / 2208.46	11.22 / 3874.88	12.12 / 6587.30		
4	13.48 / 223.62	14.28/ 424.88	15.22 / 786.02	16.32 / 1411.16	17.56 / 2475.96	18.98 / 4209.14		
5	21.00 / 142.86	22.12 / 271.43	23.42 / 502.15	24.94 / 903.88	26.68 / 1581.78	28.62 / 2689.03		
C. Yang [21], [DMPA decoder, APCCAS '17]								
1	5.60 / 150.00	5.80 / 285.00	6.06 / 527.25	6.36 / 949.05	6.78 / 1660.84	7.16 / 2823.42		
2	10.92 / 76.92	11.26 / 146.148	11.64 / 270.37	12.08 / 486.67	12.58 / 851.68	13.16 / 1447.85		
3	16.24 / 51.72	16.76 / 98.27	17.36 / 181.80	18.04 / 327.23	18.84 / 572.66	19.74 / 973.52		
4	21.56 / 38.96	22.36 / 74.02	23.30 / 136.94	24.40 / 246.50	25.64 / 431.37	27.06 / 733.34		
5	26.88 / 31.25	28.00 / 59.38	29.30 / 109.84	30.82 / 197.72	32.56 / 346.01	34.50 / 588.21		
K. Han [18], [SMPA decoder, TCAS-I Oct. '17]								
5	n.a. / 57	n.a. / n.a.	n.a. / n.a.	n.a. / n.a.	n.a. / 640	n.a. / n.a.		

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Fig. 13. Data flow graph (DFG) of step-level architecture.



Fig. 14. Data flow graph (DFG) of stage-level architecture.