# Hardware-based Scheduler Implementation for Dynamic Workloads on Heterogeneous SoCs

Alexander Fusco, Sahil Hassan, Joshua Mack, Ali Akoglu Electrical and Computer Engineering, The University of Arizona Tucson, AZ, USA {afusco1,sahilhassan,jmack2545,akoglu}@email.arizona.edu

Abstract—Non-uniform performance and power consumption across the processing elements (PEs) of heterogeneous SoCs increase the computation complexity of the task scheduling problem compared to homogeneous architectures. Latency of a software-based scheduler with the increased heterogeneity level in terms of number and types of PEs creates the necessity of deploying a scheduler as an overlay processor in hardware to be able to make scheduling decisions rapidly and enable deployment of real-life applications on heterogeneous SoCs. In this study we present the design trade-offs involved for implementing and deploying the runtime variant of the heterogeneous earliest finish time algorithm (HEFT<sub>RT</sub>) on the FPGA. We conduct performance evaluations on a SoC configuration emulated over the Xilinx Zynq ZCU102 platform. In a runtime environment we demonstrate hardware-based HEFT<sub>RT</sub>'s ability to make scheduling decisions with 9.144 ns latency on average, process 26.7% more tasks per second compared to its software counterpart, and reduce the scheduling latency by up to a factor of  $183 \times$  based on workloads composed of mixture of dynamically arriving real-life signal processing applications.

*Index Terms*—Scheduling, system on chip, FPGA, hardware emulation, multiprocessor SoC.

#### I. INTRODUCTION

Heterogeneous system on chip (SoC) computing platforms composed of a pool of general-purpose processors and specialized processors offer the ability to pair each execution phase of a given application with a compute unit that matches the processing needs of that phase. Hence, they offer a large potential for performance and energy-efficiency relative to homogeneous counterparts [1]. However, from task scheduling point of view, heterogeneous SoCs pose additional challenges as they provide a variety of compute resources giving tasks varying execution times that create a larger scheduling search space to explore. When building runtime systems for heterogeneous SoCs, it is difficult to design schedulers that are capable of thoroughly exploring the space of possible schedules while still returning effective scheduling decisions within a reasonable amount of time. Effective utilization of system resources while supporting execution of multiple interleaving applications requires a dynamic scheduling policy that considers task dependencies within an application and demands on the same processing element (PE) by multiple applications. When systems are highly heterogeneous in terms of both the number and types of PEs, and when a runtime system must deal with numerous applications co-existing on the system at once, the latency of software-based schedulers can become a major bottleneck to total system throughput. As a result, there is a strong case to be made that scheduling algorithms themselves should be subject to hardware-based acceleration to enable utilization of heterogeneous SoC platforms for practical deployment under scenarios where multiple applications co-exist in domains such as autonomous vehicles and communication systems that require low Size, Weight and Power (SWaP) solutions.

In this study, we utilize the  $HEFT_{RT}$  [2] algorithm, a runtime variant of the Heterogeneous Earliest Finish Time (HEFT) [3] scheduling heuristic, implement it in hardware as an overlay processor for an SoC composed of ARM CPU cores and FFT accelerator that is emulated on the Xilinx Zynq ZCU102 board. We analyze the design trade-offs involved for implementing and deploying the HEFT<sub>RT</sub> on the FPGA. We perform this analysis with realistic hardware configurations coupled with complex signal-processing workloads that give confidence that the results seen here will generalize across other applications. We show that for a runtime system with ready queue size of up to 5 tasks, the software based scheduler should be preferred. Beyond this point we observe that the data transfer overhead to and from the hardware-based scheduler is compensated by the reduced scheduling latency. As the ready queue size increases, the gap in scheduling overhead between hardware-based HEFT<sub>RT</sub> and software-based HEFT<sub>RT</sub> grows. Previous literature has found that hardware-accelerated scheduling is beneficial in homogeneous systems. In this study, we demonstrate the ability to accelerate a high quality, heterogeneity-aware scheduling heuristic on hardware in a manner that demonstrably reduces scheduling overhead and consequently improves total system performance. We show that hardware-based HEFT<sub>RT</sub> is capable of making up to  $183 \times$  faster scheduling decisions across the ready queue sizes used in our evaluations. Before presenting our approach to implementing  $\text{HEFT}_{\text{RT}}$  in hardware, we start by exploring related work in the area of task scheduling with emphasis on hardware based dynamic task scheduling.

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## II. RELATED WORK

Previous hardware schedulers have implemented deadlinebased scheduling policies [4]–[7], with most of them relying on earliest deadline first (EDF) for real time systems that has been shown to minimize the maximum lateness and meet deadlines when a feasible solution exists [8].

The study by Tang and Bergman [4] discuss types of task queues and their benefits across scheduling policies such as EDF, deadline based least slack time, and multilevel feedback queue using static priorities. Derafshi et al. [5] expands upon Tang and Bergman's study [4] by targeting a homogeneous multi-core processor, and moving more task dependency management to hardware. The hardware scheduler by Gupta et al. [6] also targets multi-core homogeneous processors, and implements Pfair [9], a scheduling policy that uses the expected execution time to estimate when a task will finish in relation to its deadline. Kohútka et al. [7] implement a hardware scheduler that aims to improve on the EDF policy by discarding tasks when the workload becomes unfeasible.

These hardware schedulers do not consider runtime constraints regarding how the task-to-PE-mapping decision for a given application may affect the execution time of other dynamically arriving applications, and they are limited to targeting single-core [4], [7] or multi-core homogeneous architectures [5], [6]. To the best of our knowledge, the only previous work on hardware-based scheduler for heterogeneous architectures is presented by Alivev et al. [10], which implements the Heterogeneous Earliest Finish Time [3]. This implementation, unlike EDF based schedulers, is not suitable for runtime execution as it requires parsing the full directed acyclic graph (DAG) of an application, and can only perform scheduling on one application at a time. Among all the hardware schedulers, the implementation by Derafshi et al. [5] is the only one that integrates their scheduler into a runtime environment, where they perform emulation based analysis using artificial tasks. None of these studies present analysis on the quality of schedules generated by the hardware scheduler with dynamic workloads. We perform such an analysis by implementing HEFT<sub>RT</sub> in hardware and integrating with a runtime environment.

#### III. BACKGROUND

#### A. Runtime Environment

In this study, we utilize the Compiler Integrated Extensible DSSoC Runtime (CEDR) ecosystem [11] as it enables compilation and development of user applications, evaluation of resource management strategies, and validation of heterogeneous hardware configurations in a unified framework. This runtime system operates as a background *Daemon Process* in the Linux user space and allows end users to interact with the heterogeneous architecture by launching a workload composed of any number and combination of distinct applications with user specified arrival rates. CEDR launches worker threads, each tasked with managing a particular PE on the heterogeneous system in terms of sending data to its respective PE, executing its assigned tasks, and receiving their output. Meanwhile, the CEDR management thread parses the incoming application DAGs, monitors the state of tasks executing on each PE, maintains a ready queue with tasks whose dependencies are resolved, and estimates when a PE will become available. A mapping event occurs when a new task arrives in the ready queue, which invokes the scheduler. The tasks that are in the ready queue and the estimated availability times of the PEs are then passed to the "Scheduler" at each mapping event.

## B. Runtime Variant: $HEFT_{RT}$

Heterogeneous Earliest Finish Time (HEFT) [3] is a scheduling heuristic that balances runtime complexity and quality of generated schedules, and has been shown to generate competitive schedules to this date [12]. List-scheduling algorithms, such as HEFT, are typically used as purely static schedulers as they operate on DAGs with known task dependencies and application structures. The study by Mack et al. [2] introduces a methodology that lifts the barriers of list schedulers from being deployed in a runtime environment through a series of transformations. They apply this methodology and develop the runtime variant HEFT<sub>RT</sub>. At each mapping event, HEFT<sub>RT</sub> parses the ready queue, PE state, earliest availability time collected from the runtime. It sorts all tasks in the ready queue using a separate priority queue in order of highest average runtime across all PEs. As tasks are dequeued in priority order one by one, for each task, the PE that delivers the earliest finish time is selected. This selection along with the updated availability time for that selected PE are finally sent to the runtime system. In the following section we discuss the proposed hardware implementation of this flow.

### IV. HEFT<sub>RT</sub> HARDWARE IMPLEMENTATION

# A. AXI Stream Queuing Interface

The implementation of the HEFT<sub>RT</sub> algorithm is illustrated in Figure 1. For figure clarity, the definitions and expressions for related parameters are listed in Table I. When interfacing the hardware based HEFT<sub>RT</sub> implementation with the runtime environment and the processing elements of the emulated SoC, we use direct memory access (DMA) blocks to move data between the host CPU and the processing elements via the AXI4-Stream protocol. At each mapping event, the CEDR sends the updated availability times for each PE  $(T_{avail})$ to the scheduler, which are forwarded to its designated PE Handler. This synchronizes the availability times with the runtime environment before processing the ready queue. For each task in the ready queue, the runtime environment feeds the task information that includes a unique task identifier (TID), average execution time across the PEs ( $Avg_{TID}$ ), and execution time on each PE  $(Exec_{TID}[PE_i])$ , to the scheduler through an AXI-Stream (AXI-S). The task is assigned a counter-based queue identifier (QID) ranging from 0 to the depth of the priority queue (D). The mapping of TID to QID ensures that each task is identified within a fixed range. The QID and  $Avg_{TID}$  are injected into the priority queue. While the TID is written into the BRAM, the execution



Fig. 1: Architecture of hardware scheduler.

TABLE I: Hardware Scheduler Parameters

Parameter	Meaning
Р	Number of PEs
D	Depth of Priority Queue
$PE_i$	Identifier of a PE where $i \in [0, P)$
TID	Task identifier
QID	Queue identifier
$Avg_{TID}$	Average execution time of task across all PEs
$Exec_{TID}[PE_i]$	Task execution time for a given PE
$T_{avail}$	$T_{avail}[PE_i]$
$T_{finish}$	$T_{finish}[PE_i]$
$W(Avg_{TID})$	Bit width of $Avg_{TID}$
W(QID)	Bit width of $QID$ , which is $\lceil log_2D \rceil$

times  $(Exec_{TID}[PE_i])$  are written into the LUT-RAM, both at addresses specified by the *QID*. It takes one cycle to insert the task information into the *Priority Queue* and memory blocks once they are received from the runtime.

#### B. Priority Queue

At each mapping event, the hardware scheduler sorts the tasks that are in the *Priority Queue*. Each cell in the queue, as illustrated in Figure 2, includes the task information in terms of QID and  $Avg_{TID}$ , where average execution time represents the relative importance of each task.

The Priority Queue is implemented as a shift register priority queue that has also been used in EDF based hardware schedulers [4], [7]. Each cell in the queue swaps its task information with its neighbor when the condition of the comparator logic is satisfied. The comparison operations are carried out alternately among the odd and even indexed cells following the odd-even sorting transposition algorithm [13]. Therefore it takes two clock cycles to complete every comparison. When there are two cycles in a row without any swaps, the sorting process is terminated. Then the queue switches to right-shift register mode and starts dequeuing the cell entries until all entries have been read. In each clock cycle, the output QID is used as an index to read out execution times for each PE from the LUT-RAM to be forwarded to their corresponding PE Handler along with the TID to be forwarded to the AXI-S Scheduling Interface.

#### C. Processing Element Handler

For each PE in the target hardware configuration there is a designated *PE Handler* in the hardware scheduler. It receives the  $T_{avail}$  from the AXI-S and stores this information in the



Fig. 2: Architecture of shift register priority queue.

availability time register of the *PE Handler*. The output is the finish time  $(T_{finish})$ , which is the sum of  $Exec_{TID}[PE_i]$  and  $T_{avail}[PE_i]$ . Finish time represents the estimated time when that task will complete its execution on that PE. This finish time is written into the *availability time* register only if that PE is selected by the *EFT Selector*.

The Earliest Finish Time (EFT) Selector receives the finish time for each PE as an input, and outputs an index corresponding to the index of the PE ( $PE_i$ ) with the lowest finish time. A comparator tree is utilized to implement the selection process. The EFT Selector feeds the index to each of the PE Handlers. The handler of the selected PE then makes the calculated finish time the new availability time of that PE. During this update, the TID and the  $PE_i$  are sent to the runtime through the AXI-S Scheduling Interface.

#### V. EXPERIMENTAL SETUP

All experiments are performed on the Xilinx Zyng Ultrascale+ ZCU102 MPSoC development board. This MPSoC combines general purpose CPUs (4x Arm Cortex A53 processors) with programmable FPGA fabric. On the FPGA fabric, we add the Xilinx FFT IP accelerator for Fast Fourier Transform (FFT). We use four representative real-world applications part of the CEDR release [11] that are Radar Correlator (RC), Temporal Interference Mitigation (TM), Pulse Doppler (PD), and WiFi TX (TX). Based on average observed latencies, RC and TM are *low* latency applications, whereas relatively TX and PD are *high* latency applications. We refer to the "Frame" as the input data size needed by a single instance of each of the applications. The low workload consists of twenty Frames for RC and TM for a 1280Kb per frame. We compose a high latency workload consisting of ten instances of PD and TX applications each, with a *Frame* size of 1037 Kb per frame. We use the low-latency workload for verifying the functionality of the hardware HEFT<sub>RT</sub> with respect to its software counterpart, as low latency workloads will not stress the scheduler and in turn trends will not be affected by the hardware based scheduler making faster scheduling decisions. The high latency workloads on the other hand will allow us to compare the performance of the two schedulers when the system becomes oversubscribed. We evaluate the performance of each scheduler in this study by stressing the scheduler's ability to cope with the volume of incoming jobs. We establish this by setting a fixed "target" frame rate that defines the rate of application instances arriving in the runtime per second. Then, we monitor if the scheduler can complete jobs at that same rate or if system performance begins to suffer. We refer to the

TABLE II: Resource usage on Zynq ZCU102 FPGA along with the total including peripheral resources shown in Figure 1.

Module	Logic LUTs		LUT-RAM		Registers		BRAM	
Priority Queue	18,632	6.8%	0	0%	13,433	2.5%	0	0%
PE Handlers	404	1.5%	0	0%	128	0.5%	0	0%
EFT Selector	48	0.02%	0	0%	0	0%	0	0%
Total	19,603	7.2%	1,280	0.9%	14,534	2.7%	0.5	0.05%

empirical frame rate observed as the "achieved" frame rate, which indicates the number of applications that the runtime can process per second. For this, we use 29 different injection rates, where the injection rate defines the amount of input data arriving into the runtime per unit time.

We use three metrics for performance evaluation. The cumulative execution time of an application is the sum of execution times of its individual tasks, ignoring the overhead associated with scheduling them. Lower cumulative execution time indicates better scheduling decisions made and better exploitation of the available heterogeneity at hand. The scheduling overhead metric captures the time spent by the runtime in making scheduling decisions. The application execution time is the difference between the end of the last task and the start of the first task of an application, including the overhead of all scheduling decisions in between. Lower execution times indicate the scheduler's capability to manage the workload efficiently. To make the cumulative execution times and application execution times comparable across different runtime configurations, we normalize them with the number of applications (per application). We sweep all input configurations, repeat each experiment twenty five times, and collect performance metrics listed in the table by averaging across the twenty five runs. We then average these three metrics across twenty five repetitions.

## VI. RESULTS AND ANALYSIS

## A. Hardware Analysis

Table II shows resource usage of the  $\text{HEFT}_{\text{RT}}$  scheduler on the Zynq ZCU102 for a configuration where the system is composed of 4 PEs, priority queue depth is 512, and bit-width for representing average execution time ( $W(Avg_{TID})$ ) is set to 16. We choose 16 bits over 32 bits, since this bit-width provides sufficient dynamic range and reduces the amount of LUTs used by the datapath. The design uses 7.15% of the available LUTs and the majority of the LUTs and registers in the scheduler are consumed by the *Priority Queue*. The amount of LUT-RAM reserved for storing the execution time information of each DAG node for each PE is a product of the number of PEs and the depth of the priority queue, since it stores the execution time for each task on each PE when the priority queue is full.

The *Priority Queue* allows insertion and removal of tasks through the front of the queue, which prevents the depth of the queue from impacting the number of cycles needed to make a scheduling decision. Sorting the queue in odd-even phases allows each cell to only depend on its immediate neighbor, which makes the path delay independent of the queue depth. Therefore, the odd-even transposition based sorting prevents

TABLE III: Resource usage and path delay comparison where HEFT<sub>RT1</sub> is based on P = 16, D = 132,  $W(Avg_{T1D}) = 16$ , and HEFT<sub>RT2</sub> is based on P = 4, D = 64,  $W(Avg_{T1D}) = 32$ . [5] is based on 16 PEs with a total queue length of 132. [4] is based on 1 PE with a priority queue length of 64 and a priority bit-width of 32.

	HEFT <sub>RT1</sub>	[5]	HEFT <sub>RT2</sub>	[4]
LUTs	7,598	4,834	4,360	2,170
LUT-RAM	1,920	N/A	160	N/A
Register	6,430	3,968	3,590	1,158
Path Delay (ns)	5.91	5.001	3.035	6.122

the queue depth from impacting the critical path. Due to the minimum tree structure of the EFT Selector, the number of PEs impacts the critical path delay, while the queue depth and bit width parameters affect the LUT and register usage. The *EFT Selector* and *PE Handlers* take relatively fewer resources and the *PE Handler* is on the critical path due to the feedback loop that goes through the adder within the *PE Handler*, comparator and multiplexers in the *EFT Selector*, decoder, and finally back to the *PE Handler*. Since the *EFT Selector* inputs are fed through a comparison tree driven by the number of PEs, the *EFT Selector* contributes to the path delay but its contribution to critical path scales logarithmically with the PE count.

In Table III, we show resource usage and path delay reported by the EDF based schedulers ( [4], [5]) that are implemented with priority queue lengths of 132 and 64 respectively. We synthesize two versions of  $\text{HEFT}_{\text{RT}}$  to match the two priority queue lengths and include in the table as  $\text{HEFT}_{\text{RT1}}$  and  $\text{HEFT}_{\text{RT2}}$ . Since bit-width of 32 is used by [4] for priority, we set  $W(Avg_{TID}) = 32$  for  $\text{HEFT}_{\text{RT2}}$ . The other implementations synthesize schedulers with search [4] and heap-based [5] insertion queues that require less comparison logic compared to our shift register based queue implementation that on the other hand offers ability to insert tasks at every cycle.

The scheduler is capable of processing a ready queue of size n in 3n + 3 cycles, with a turnaround of 2n + 3 cycles for the task to PE mapping decision of the first entry in the sorted Priority Queue. The Priority Queue can be filled at a rate of one task per cycle, meaning it will take n cycles to fill the priority queue with the tasks that are received from the ready queue. The odd-even sorting implemented by the shift register queue takes n cycles to sort for the worst case [13]. Additionally, both sorting phases will need to happen with no shifts for the queue to be marked as sorted, resulting with additional two cycles. The priority queue can shift out tasks at a rate of one cycle per task while reading the execution times from the LUT-RAM. After dequeuing and reading from LUT-RAM, it takes the PE Handlers and EFT Selector one cycle to make the PE mapping decision. The time to fill the queue, complete sorting, and select the PE accumulates to 2n + 3cycles to generate the first scheduling decision. Shifting out and mapping the tasks at a rate of one task per cycle adds another n cycles, meaning the scheduler will take at most 3n+3 cycles to map a ready queue of size n to each of the PEs. The average number of cycles it takes to make a single task to PE mapping decision is then  $\frac{3n+3}{n}$ . Given that latency

TABLE IV: Hardware scheduler resource usage and path delay with respect to P and D on Zynq ZCU102 FPGA.



Fig. 3: Minimum cumulative execution time of tasks for low latency workload versus injection rate.

for the design with *Priority Queue* length of 512 over 4 PE configuration is 3.048 ns, average time to make a single task to PE mapping decision is 9.144 ns excluding the data transfer overhead to the *Priority Queue* of the scheduler.

In Table IV we first fix the number of PEs (P) on the SoC to 4 and show the hardware scheduler resource usage and path delay with respect to increase in *Priority Queue* length (D) from 64 to 512. In the same table, we fix D at 512 and increase P from 4 to 8 and 16. Increasing the D does not affect the path delay confirming our earlier complexity analysis, and as expected LUT and LUT-RAM usage increases proportionally with D. As expected path delay grows less than linearly as we increase P from 4 to 8 and 16 due to the minimum tree structure of the *EFT Selector* unit. The EDF hardware scheduler [5] that uses 16 PEs with a queue length of 134 has a critical path delay of 6.122 ns, while our design with 16 PEs and 512 queue length has a critical path delay of 6.875 ns.

#### B. Functional Verification

Figure 3 shows cumulative execution time between software and hardware versions of the HEFT<sub>RT</sub> scheduler for lowlatency workload with respect to change in job injection rate. We choose low-latency workloads for this scenario due to the fact that, as noted in Section V, they do not heavily stress the scheduler. The cumulative execution time is independent from scheduling overhead, and is completely dependent on task execution time. If the hardware scheduler were making different PE mapping decisions, we would expect to see a difference in the cumulative execution time, however the average difference across injection rates between the two schedulers is only 0.024 ms which corresponds to 0.32% difference on average between pairwise points on the plot. This negligible difference confirms that the two schedulers are making similar task to PE mapping decisions across all injection rates.



Fig. 4: Ready queue size versus scheduling overhead for  ${\rm HEFT}_{RT}$  and  ${\rm HEFT}_{RT_{\rm HW}}$ 



Fig. 5: Average execution time vs. injection rate for  $\text{HEFT}_{\text{RT}}$  and  $\text{HEFT}_{\text{RT} HW}$  schedulers over high-latency workload.

## C. Performance Analysis

In Figure 4 we show the average scheduling overhead for software (HEFT<sub>RT</sub>) and hardware (HEFT<sub>RT HW</sub>) based implementations with respect to increase in the ready queue size of the CEDR. We measure the scheduling overhead by recording the start and completion times of each mapping event. The rate of increase in scheduling overhead as the queue size grows is higher with the  $\text{HEFT}_{\text{RT}}$  compared to the HEFT<sub>RT HW</sub>. This is expected based on the 3n+3 cycle count analysis presented earlier, that offers O(n) complexity, while the software implementation relies on sorting with  $O(n \log_2 n)$ complexity. However, we note that in the plot we observe some outlier points that are not following the expected trend line for the HEFT<sub>RT HW</sub> primarily caused by the data transfer overhead on the Zynq ZCU102. In the same plot we show the ready queue size in the range of 1 to 10 in magnified form to illustrate the crossover point where HEFT<sub>RT</sub> offers less overhead for queue size of up to 5. Beyond this point, data transfer overhead to the HEFT<sub>RT HW</sub> is compensated by its ability to make faster scheduling decisions. The gap between the two schedulers grow as the queue size increases, where we observe a speed up of  $2.6 \times$  at queue size of 1330. Without the data transfer overhead, in terms of time to make scheduling decisions HEFT<sub>RT HW</sub> achieves a speedup of  $183 \times$ .

Figure 5 shows the average application execution time per application along the y-axis, with respect to varying injection rates along the x-axis, for both  $\text{HEFT}_{\text{RT}}$  and  $\text{HEFT}_{\text{RT}\_\text{HW}}$  schedulers. Here, we observe that for lower injection rates (< 250 Mbps), the application execution times for both schedulers increase linearly with increasing injection rates. This is expected as increasing injection rate grows the number



Fig. 6: Target frame rate vs. average achieved frame rate for  $\text{HEFT}_{\text{RT}}$  and  $\text{HEFT}_{\text{RT}}$  HW over high-latency workload.

of concurrent jobs in the runtime, and with these jobs sharing the same set of PEs, their execution times see a linear growth. The reduction in execution time per application with the hardware scheduler becomes more dominant as the injection rate increases. As the injection rate goes beyond a certain level (> 250 Mbps), the execution time per application starts to saturate on average, at 131.37 ms and 89.79 ms for  $\text{HEFT}_{\text{RT}}$ and  $\text{HEFT}_{\text{RT HW}}$  respectively. The saturation is caused by the runtime reaching to an oversubscribed state, where it is processing tasks on PEs at the maximum possible rate, and no further improvement is attainable. Execution time comparison between both schedulers across all injection rates show that with the HEFT<sub>RT HW</sub> this time is consistently lower than HEFT<sub>RT</sub> and results with a 31.7% reduction on average in the saturated region. The improvement in execution time is achieved due to the ability of HEFT<sub>RT HW</sub> in making faster scheduling decisions, which enhances the runtime's capability to cope with scenarios where larger number of applications may arrive. We further discuss this frame processing capability using Figure 6, where we present the trend in average achieved frame rate on y-axis with respect to target frame rate on x-axis for high latency workload.

In Figure 6, for lower values of target frame rates (<250frames/second), both the HEFT<sub>RT</sub> and HEFT<sub>RT\_HW</sub> schedulers show similar linear trend of growth in average achieved frame rate, as the target frame rate increases. For higher values of target frame rates (>250 frames/second), the average achieved frame rate saturates for both the schedulers, which indicates that the runtime has become oversubscribed and system resources are fully occupied. The saturation point on the achieved frame rate with HEFT<sub>RT\_HW</sub> scheduler is at 204.62 frames/second (on average), while HEFT<sub>RT</sub> saturates at 161.51 frames/second on average. We notice that with the HEFT<sub>RT HW</sub> scheduler, the runtime is able to achieve saturation at around 43.11 frames/second higher frame rate on average compared to the HEFT<sub>RT</sub> scheduler. The ability of the hardware scheduler to make task-to-PE mapping decisions faster, provides the runtime with a better capability to process frequently arriving jobs at a higher rate in the oversubscribed state and in turn results with 26.7% more frames/second in average achieved frame rate.

## VII. CONCLUSION

In this work, we explore the design, implementation, and evaluation of the HEFT<sub>RT</sub> [2] in hardware to accelerate the scheduling of dynamically interleaved applications across heterogeneous SoCs. We implement HEFT<sub>RT</sub> as an overlay processor on the Zynq Ultrascale+ ZCU102 FPGA and integrated it into an open source runtime system (CEDR [11]). We find that, for an SoC composed of 3 ARM cores and 1 FFT accelerator emulated on the same ZCU102 FPGA, we are able to generate competitive schedules with a 9.144 ns average latency for making a task-to-PE mapping decision. We present analysis of this hardware design by exploring the impact of queue size and number of processing elements on the latency and resource usage, and we find that our design is overall quite scalable to different system configurations. We then stress the scheduler by evaluating it in our runtime environment with realistic workloads, and we find that it can simultaneously produce high quality scheduling decisions and maintain correct application execution. As future work, we will explore acceleration of energy-aware scheduling heuristics in order to expand our evaluations beyond focusing purely on optimization of execution time.

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