A 0.2-to-2MHz BW, 50-to-86dB SNDR, 16-to-22mW Flexible 4th-Order ΣΔ Modulator with DC-to-44MHz Tunable Center Frequency in 1.2-V 90-nm CMOS

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Abstract—**This paper describes the design of a switched-capacitor fourth-order single-loop ΣΔ modulator with a 5-level embedded quantizer. The loop filter consists of a cascade of resonators with distributed feedforward (CRFF) coefficients, which can be programmed to make the zeros of the noise transfer function variable. As a result, the modulator can be reconfigured either as a lowpass or as a bandpass analog-to-digital converter with a tunable notch frequency and an optimized loop-filter zero placement. The circuit – designed and implemented in a 1.2-V 90-nm CMOS technology – incorporates diverse architecture- and circuit-level strategies to adapt its performance to different sets of specifications with a variable sampling frequency of 100 and 200MHz and scalable power consumption. Post-layout simulations (for frequency range of DC to 22MHz) and behavirol simulations (from 22 to 44MHz) show a correct operation of the circuit in steps of 1-to-2MHz, featuring an adaptive SNDR of 74-to-86, 57-to-68 and 50-to-59dB within a signal bandwidth of 200kHz, 1MHz and 2MHz, respectively, while dissipating a scalable power consumption of 16-to-22mW[1].**

I. INTRODUCTION

The efficient implementation of Software Defined Radio (SDR) demands for a nanometer CMOS System-on-Chip (SoC) implementation, in which signal processing is mostly carried out in the digital domain. One of the key building blocks enabling such an SDR SoC to be possible is the Analog-to-Digital Converter (ADC). This circuit should be ideally placed at the antenna so that Radio Frequency (RF) signals could be directly digitized, thus being processed in a flexible way by running software on a Digital Signal Processor (DSP) [1].

Unfortunately, this application scenario is still far from a consumer product deployment, mostly limited by the unfeasible *power-hungry* specifications required for the ADC [2]. However, recent advances in Sigma-Delta Modulation (ΣΔM) techniques [3][4][5][6] – fuelled by the continuous downscaling of CMOS processes – are pushing RF digitization forward, taking significant steps towards future SDR-based mobile devices.

The majority of reported RF-to-digital converters are Band-Pass (BP) ΣΔMs with a fixed center or *notch frequency* (f_n), and include diverse strategies such as frequency-translation [7], subsampling [3] and out-of-band embedded filtering [4] in order to relax the ADC specifications in a simplified mostly-digital RF receiver.

One of the problems associated to conventional BP-ΣΔMs with a fixed notch frequency is that the RF receiver requires a programmable-frequency Voltage-Controlled Oscillator (VCO) in order to place the signal band within the passband of the BP-ΣΔM. This issue has motivated the interest for reconfigurable BP-ΣΔMs with tunable notch frequency [8][9]. To the best of the authors' knowledge, the work in [8] reported the widest tuning range achieved by Switched-Capacitor (SC) BP-ΣΔMs, ranging from DC to 12MHz, while consuming 115mW. Recently, a Continuous-Time (CT) BP-ΣΔM significantly increased that frequency range up to 1GHz, at the price of consuming 550mW [9].

This paper contributes to this topic and presents the design of a fourth-order reconfigurable SC single-loop casecade of resonator with feedforward (CRFF) LP/BP-ΣΔM with 5-level quantization, intended for Intermediate-Frequency (IF) digitization. Both architecture- and circuit-level reconfiguration strategies are combined to achieve a competitive performance in terms of programmable effective resolution (8-to-14 bit), signal bandwidth (0.2-to-2MHz), notch frequency (DC-to-44MHz) and adaptive power consumption (16-to-22mW). Compared to previously reported SC-ΣΔMs, the presented circuit achieves a wider programmable frequency range with lower power consumption, while keeping a reduced number of loop-filter coefficients and a lower number of levels of the embedded quantizer, with the subsequent silicon area saving.

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II. MODULATOR ARCHITECTURE

Resonation-based ΣΔM architectures are a priori good alternatives to achieve programmable center frequency. For that reason a single-loop fourth-order CRFF topology has been selected in this work. Compared to its cascade of resonators with feedback (CRFB) counterpart, the CRFF loop-filter realization requires less number of loop-filter coefficients, what results in less area occupied by the corresponding capacitor ratios and consequently, a power saving. The modulator architecture uses a 4th-order loop filter consisting of two resonators as shown in Fig. 1 [10]. Each resonator is made up of one Forward-Euler (FE) and one Backward-Euler (BE) integrator. Two feedback coefficients (g_1 and g_2) across the resonators can be tuned to a get a desired notch in the Noise Transfer Function (NTF) of the modulator. A direct feedforward path from the input to the adder is used to implement a unity Signal Transfer Function (STF), thus relaxing the swing requirements of integrators. Coefficients c_1 to c_4 are employed for further scaling of integrators. In order to keep the required NTF and STF while varying the integrator input coefficients, feedforward coefficients a_1 to a_4 also need to be changed accordingly. Indeed, the modulator can be visualized as a cascade of two resonators. Transfer functions of the resonators involved are given by,

$$H_1(z) = \frac{c_2 z^{-1}}{1+(g_1 c_2 - 2)\, z^{-1} + z^{-2}} \tag{1}$$

$$H_2(z) = \frac{c_4 z^{-1}}{1+(g_2 c_4 - 2)\, z^{-1} + z^{-2}} \tag{2}$$

Solving for the poles of $H_1(z)$ and $H_2(z)$ in (1)-(2), the center (notch) frequencies of the resonators can be found, giving:

$$n_1 = \cos^{-1}\left(\frac{2 - c_2 g_1}{2}\right) \tag{3}$$

$$n_2 = \cos^{-1}\left(\frac{2 - c_4 g_2}{2}\right) \tag{4}$$

A. Synthesis of the Loop-Filter Coefficients

The values of the ΣΔM loop-filter coefficients have been synthesized for a programmable center frequency range of 0-22MHz, considering frequency steps of 1MHz and a sampling frequency of 100MHz. The well-known Schreier's MATLAB Delta-Sigma toolbox [11] has been employed to this purpose, resulting in 23 different sets of coefficients. The derived coefficients were optimized to maximize integrators output swing performance (below 20% of the full-scale range), while keeping feasible capacitor-ratio implementations. For each combination of integrators output swings, a different set of coefficients c_1 to c_4 is obtained, and the values of g coefficients get changed for each notch frequency according to (3) and (4). At the same time, to keep the same noise-shaping behavior, i.e. the same NTF, for all notch frequencies, feedforward coefficients (a_1 to a_4) also get modified. As an illustration, Table I shows the set of coefficients derived for a f_n of 3MHz. Note that coefficients b_1 and c_1 can be easily realized with capacitor ratios of 0.25, while g_1 =0.0625 and g_2 =0.125 in this case. Moreover it can be observed that all coefficients are multiple of either 0.0625 or 0.125. This leads to a straightforward binary-weighted implementation of the sampling capacitor with a fixed integrating capacitor. Table II summarizes the different features of the resultant coefficients for the whole range of f_n, including minimum and maximum values, and the number of bits required for implementation.

B. Ideal Modulator Performance and Behavioral Simulations

In order to check the validity of the derived coefficients, behavioral simulations have been carried out using SIMULINK elementary blocks over an input frequency range of 0 to 22MHz. Based on the derived coefficients, the tunability range can be increased if sampling rates larger than 100MHz are used. To this end, behavioral simulations have been also performed at 200MHz clock rate, thus increasing the notch frequency range up to 44MHz, with frequency steps of 2MHz. Considering these sets of sampling frequencies, the signal-to-quantization noise ratio (SQNR) achieved with the ideal modulator are in the ranges of 110dB, 90dB and 75dB, respectively for 200-kHz, 1-MHz and 2-MHz signal bandwidths.

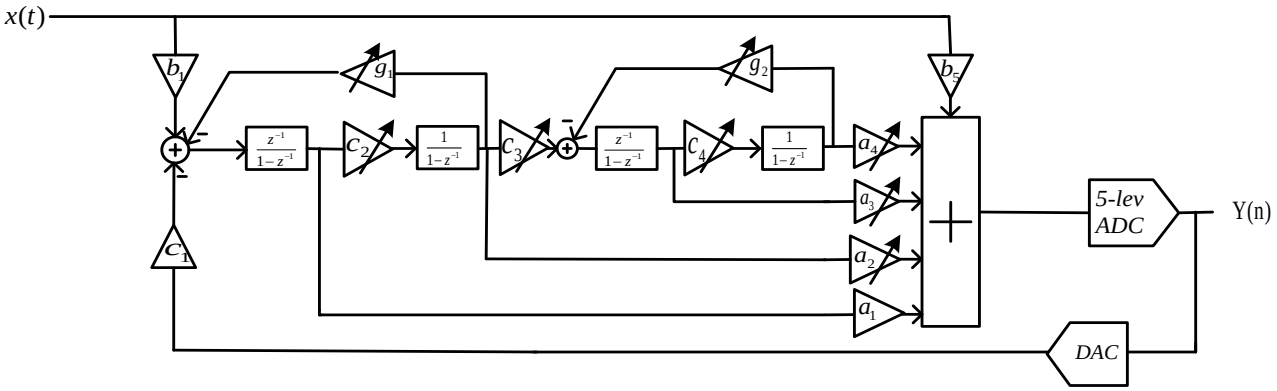


Figure 1. Reconfigurable fourth-order CRFF ΣΔM architecture.

Table I. Modulator coefficients for a 3-MHz notch frequency

Coef.	Val.	Coef.	Val.	Coef.	Val.	Coef.	Val.
b_1	0.25	a_1	3.00	c_1	0.25	g_1	0.0625
$b_2\,b_3\,b_4$	0.00	a_2	3.25	c_2	0.50	g_2	0.1250
b_5	1.00	a_3	2.75	c_3	0.50		
		a_4	1.125	c_4	0.25		

Table II. Coefficient characteristics

Coefficients	Min.	Max.	No. Of Bits
b_1	0.25	0.25	--
$b_2\,b_3\,b_4$	0	0	--
b_5	1	1	--
a_1	3	3	--
a_2	0.125	3.875	5
a_3	0.125	3.875	5
a_4	0.125	3.875	5
c_1	0.25	0.25	--
c_2	0.125	1.875	4
c_3	0.125	1.875	4
c_4	0.125	1.875	4
g_1	0.0625	1.875	5
g_2	0.0625	1.875	5

As an illustration, Fig. 2 shows the SNDR-versus-amplitude curves obtained within the whole notch frequency tuning range (0-to-44MHz) and considering a signal bandwidth of Bw=1MHz. The notch frequency reconfigurability is illustrated in Fig. 3 considering the whole tuning range.

III. Impact of Circuit Errors and High-Level Sizing

The modulator specifications described above have been mapped onto building-block specifications using SIMSIDES, a SIMULINK-based time-domain simulator for ΣΔMs [12]. The first step of this high-level sizing consisted of deriving the values of all loop-filter capacitances based on thermal-noise design considerations as described below.

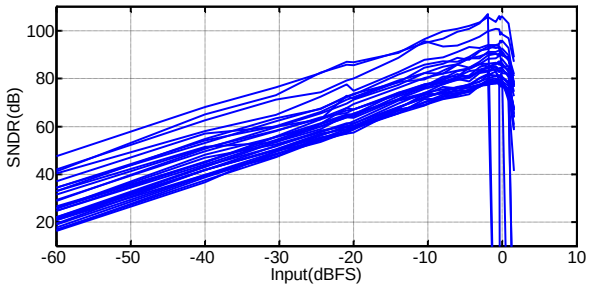


Figure 2. SNDR vs input amplitude for a bandwidth of 1MHz and frequency notches from 0 to 44MHz.

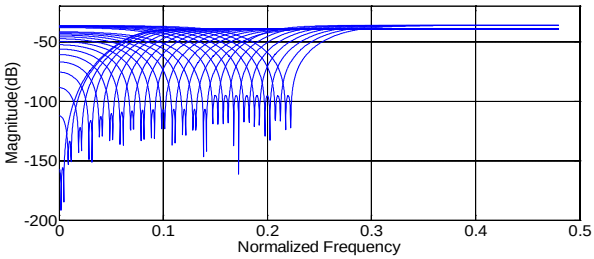


Figure 3. Noise shaping plot for different notch frequencies.

A. Thermal Noise Contribution and Capacitor Sizing

Fig. 4 shows the conceptual (single-ended) SC schematic of the modulator. The total input referred noise at f_n can be approximated by [13]

$$V_{n(rms)}^2 = \frac{4kT}{OSR}\left[\frac{1}{C_{b1}} + \frac{g_1}{b_1 C_{b1}} + \frac{\left|1-e^{(-i2\Pi f_n)}\right|^2}{b_1^2 C_{c2}}\right] \quad (5)$$

where C_{b1} and C_{c2} are the sampling capacitors of first and second integrators, respectively. Note that, as b_1 remains the

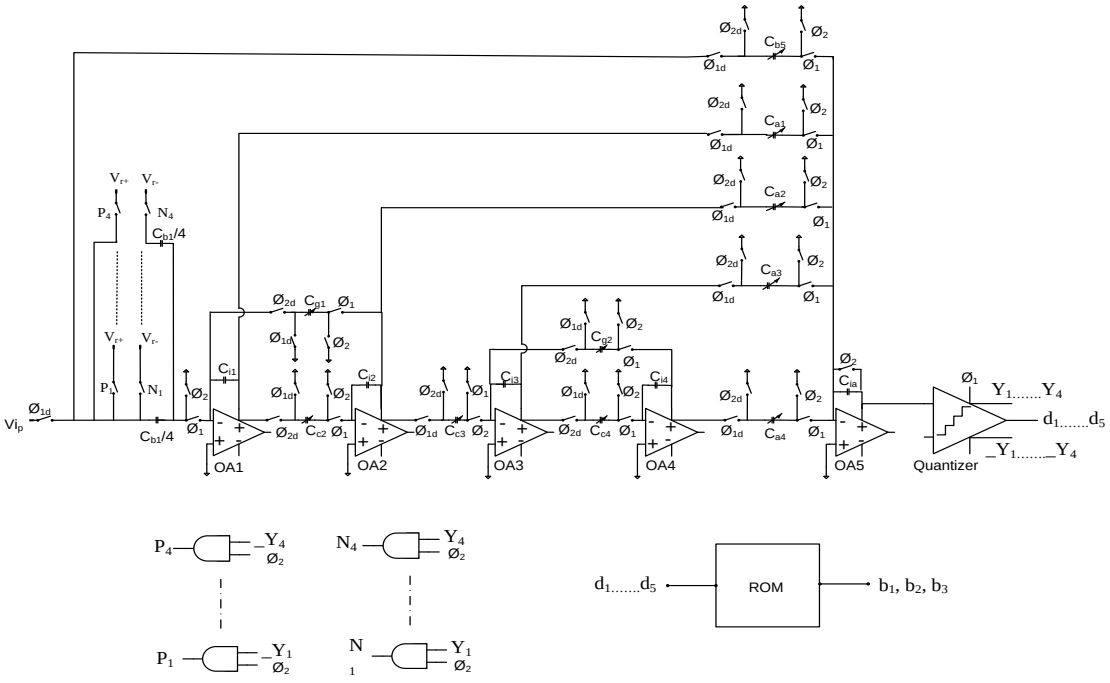


Figure 4. Conceptual (single-ended) SC schematic of the modulator.

same for whole range of frequencies (i.e. 0.25), the noise power essentially depends on two capacitor values, C_{b1} and C_{c2}. It may be observed that smaller values of the sampling capacitors and higher notch frequencies lead to larger values of the input-referred noise power. Based upon the required noise performance for given specifications, and taking the loop-filter coefficient spread into account, the final values of the modulator capacitors are derived – see Table III.

B. Building-Block Specifications

Once all modulator capacitors have been sized, a high-level sizing procedure was carried out in order to obtain the electrical parameters, i.e. finite opamp DC gain, Gain-BandWidth (GBW) product, etc, of the different modulator subcircuits (opamps, comparators, switches). To this end, a number of parametric simulations have been done, considering the different input signal conditions, i.e. notch frequency and bandwidth, as well as the sampling frequencies under consideration, i.e. 100MHz and 200MHz.

Table IV includes the outcome of the high-level sizing process, showing the main opamp specifications that satisfy the required modulator performance. These specifications – considering the worst-case signal conditions – constitute the starting point for the electrical sizing of the modulator subcircuits, which is summarized in the next section.

IV. CIRCUIT DESIGN

A. Capacitor Array Implementation

Front-end integrator coefficients except the one implementing resonance remain the same over the whole range of notch frequencies. Therefore sampling capacitors of this integrator are fixed. The remaining integrators and the active adder use the same configuration for the sampling capacitor implementation. The required reconfiguration of loop-filter coefficients is implemented by banks of switchable binary-weighted sampling capacitors, which are connected or disconnected according to the required coefficient values. As an illustration, Fig. 5 represents the single-ended schematic of the third integrator in the modulator chain (see Fig. 4). Note that digital signals $D_0 \ldots D_3$ and $\_D_0 \ldots \_D_3$ control the binary-weighted scheme.

Table III. Capacitor values (pF)

		Min.	Max.	Bits
1st Integrator	*Cb1*	0.2	0.2	--
	Cg1	0.05	1.55	5
2nd Integrator	*Ci1*	0.8	0.8	--
	Cc2	0.1	1.5	4
	Ci2	0.8	0.8	--
3rd Integrator	*Cc3*	0.1	1.5	4
	Cg2	0.05	1.55	5
	Ci3	0.8	0.8	--
4th Integrator	*Cc4*	0.05	0.75	4
	Ci4	0.4	0.4	--
	Ca1	1.5	1.5	--
	Ca2	0.05	1.55	5
Adder	*Ca3*	0.05	1.55	5
	Ca4	0.05	1.55	5
	Cia	0.4	0.4	--

Table IV. Amplifiers parameters drawn from parametric analysis

fs=100MHz				
	1st opamp	**2nd opamp**	**3rd opamp**	**4th opamp**
DC Gain (dB)	46.9	46.9	46.5	45.6
gm (mA/V)	4.7	4.5	3.2	1.5
o/p current (μA)	1000	1000	600	500
o/p swing (V)	±0.17	±0.17	±0.12	±0.16
i/p cap. (fF)	72	72	72	72
o/p cap. (fF)	32	32	32	32
Eq. input noise ($nV/Hz^{1/2}$)	4	4	5	8
fs=200MHz				
	1st opamp	**2nd opamp**	**3rd opamp**	**4th opamp**
DC Gain (dB)	46.9	46.9	46.5	45.6
gm (mA/V)	5.1	4.5	3.2	1.5
o/p current (μA)	1100	1100	900	900
o/p swing (V)	±0.18	±0.18	±0.12	±0.13
i/p cap. (fF)	72	72	72	72
o/p cap. (fF)	32	32	32	32
Eq. input noise ($nV/Hz^{1/2}$)	4	4	5	8

B. Operational Amplifier

A folded-cascode topology has been adopted for the five opamps in the modulator. Minimum-length transistors have been avoided in the input pair and in the current mirrors in order to reduce flicker (1/*f*) noise and mismatching. The amplifiers bias current is adapted to fulfill the modulator high-level requirements with adaptive power consumption. Biasing circuit is composed of two modified Wilson mirror stages which work with currents in the range of 10μA to 100μA. Table V summarizes the electrical performance of the opamps as a function of the bias current. This table illustrates how the modulator performance can be optimally adapted at circuit level to the required system-level specifications, by modifying the most important opamp metrics (transconductance, g_m, current of the output branch, etc) according to the required performances.

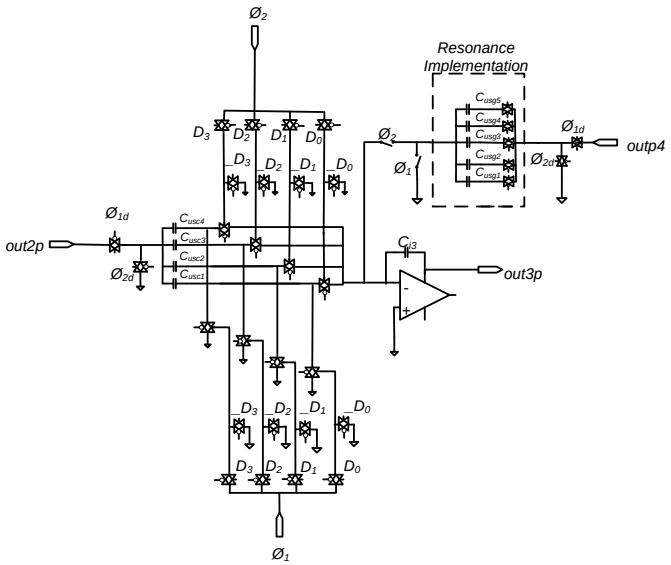


Figure 5. Single-ended schematic of the third integrator.

Table V. Performance summary of amplifiers

Bias current (μA)	30	40	50	60	65	70
DC gain (dB)	47.77	47.45	46.9	46.21	45.7	45.31
***gm* (mA/V)**	2.45	3.60	4.01	4.58	5.20	5.48
Phase margin (°)	63.55	64.10	64.20	64.40	64.50	64.60
Output current (μA)	286.60	389.60	491	590	647	698
Output swing (V)	±0.73	±0.67	±0.61	±0.56	±0.53	±0.50
Input cap. (fF)	332	343	347	354	359	362
Output cap. (fF)	23	20	18	17	16	15
Power (mW)	1.80	2.03	2.50	2.95	3.14	3.37

C. Embedded 5-level ADC

The embedded 5-level ADC consists of a flash topology and can be divided into three parts: a resistance ladder generating the voltage references, an array of comparators and a thermometric-to-binary encoder. The output binary code is stored in a ROM for collecting it off chip.

D. Serial-to-Parallel Register

Reconfiguration of coefficients and biasing requires a large number of control signals that are handled by means of an on-chip Serial-to-Parallel register. As shown in Fig. 6, 76-bit control words can be loaded to the register, which consists of D Flip-Flops in series.

V. Simulation Results

The modulator has been designed and implemented in a 90-nm 1-poly 9-metal digital CMOS technology. Fig. 7 shows the layout of the modulator highlighting its main parts. The modulator, including the pad ring, occupies an active area of 3.52mm^2. The layout floorplan considers separate analog, mixed and digital supplies, as well as guard-rings surrounding each section of the circuit.

Fig. 8(a) and (b) present the modulator output spectra for post-layout simulations corresponding to two notch frequencies (0MHz and 18MHz), while (c) represents the result of behavioral simulation of 44MHz notch, demonstrating a correct functionality of the modulator.

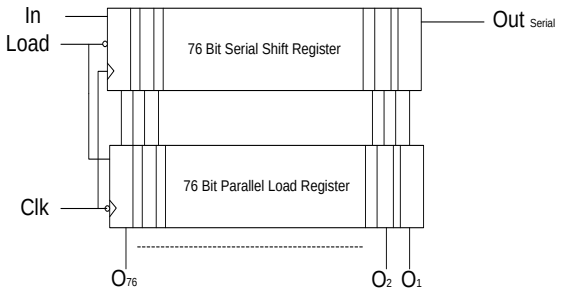


Figure 6. Block diagram of the serial-in parallel-out register.

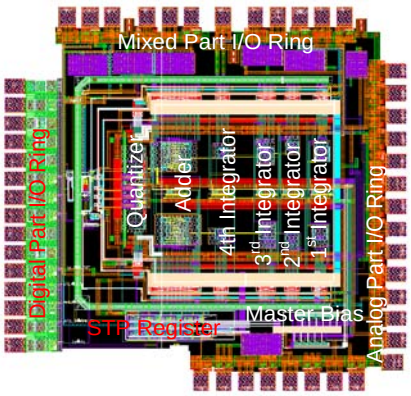
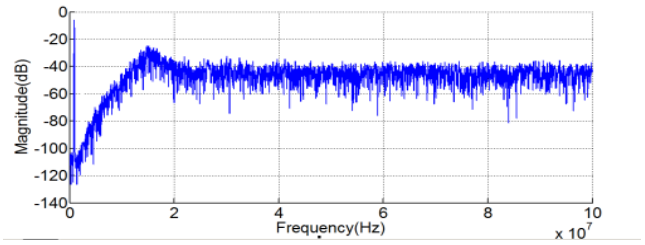
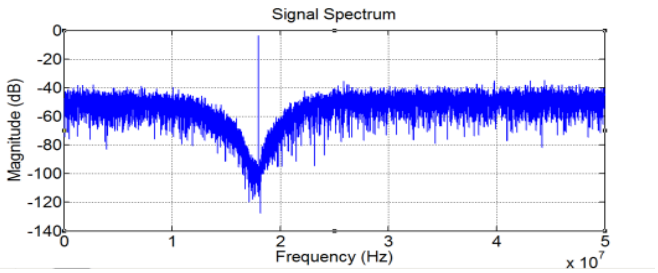


Figure 7. Layout of the modulator (STP stands for Serial-to-Parallel).

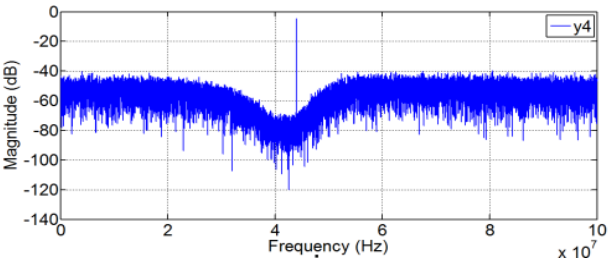
Fig. 9 shows several SNDR-versus-input level curves considering different cases of the input signal bandwidth and notch frequencies. These curves have been obtained by time-domain behavioral simulations considering the electrical performance of the opamps extracted from transistor-level simulations.



(a)

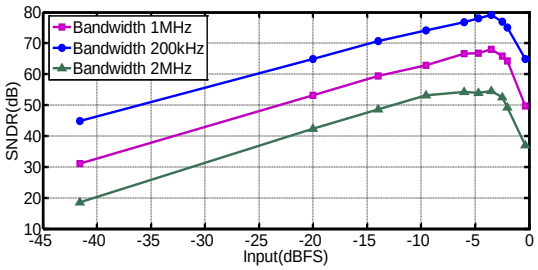


(b)

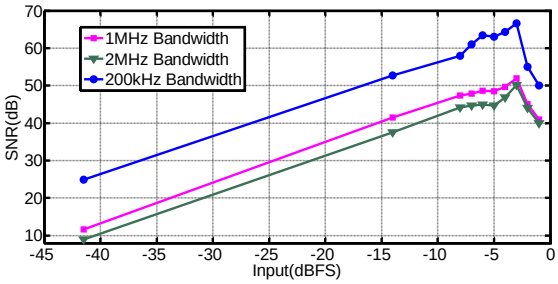


(c)

Figure 8. Output spectrum for: (a) LP (post-layout simulation), (b) 18-MHz notch (post-layout simulation), (c) 44-MHz notch (behavioral simulation).



(a)



(b)

Figure 9. SNDR curves for: (a) 12-MHz notch, (b) 44-MHz notch.

Finally, Table VI summarizes the performance of the designed modulator and compares it with state-of-the-art SC-BPΣΔM implementations[2]. Note that this modulator presents a better performance in terms of tunability and power consumption.

Table VI.Performance summary and comparison with the state of the art

	fs (MHz)	**Fin (MHz)**	**Bw (MHz)**	**SNDR (dB)**	**Power (mW)**	**FOM (pJ/conv)**
[14]	1	0.1-0.40	0.00781	61	200	13900
[8]	40	0-12.60	0.31	71-81	115	63-18
[15]	42.8	10.70	0.2	42.3	12	287
[16]	42.8/14.7	10.70	0.2/0.009	61,65	76,66	207,2500
This work	100-200	0-44	0.2/1/2	50-86	16-22	14.13-24.4

VI. CONCLUSIONS

A tunable center frequency 90-nm 1.2-V CMOS SC ΣΔM has been described. It can be reconfigured to tune to a center frequency in a range of 0-44MHz with adaptive power (16-22mW). Post-layout simulation (from DC to 22MHz) and behavioral simulations with transistor-level extracted performance metrics of opamps (from 22MHz to 44MHz) show better performance as compared with other SC BP-ΣΔMs. In the time of writing this manuscript, the chip is being fabricated. Experimental measurements are expected to be included in the final camera-ready version of the paper.

[2]Note that this table compares simulations results provided by the presented design with experimental results of the state of the art. Although this comparison is not fair, it has been included in this paper for illustration purposes and to put this work in context. The chip is currently under fabrication and it is expected that experimental results will be provided in the final version of the paper.

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