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***Abstract*—The yield optimization and radiation hardness are relevant reliability requirements as chip manufacturing advances more in-depth into the nanometer regime. One way to obtain improvements in these issues is by applying techniques to mitigate the effects of process variability and radiation-induced soft errors in the circuits. This work reports the use of three circuit-level approaches in FinFET designs as well as point out the pros and cons of adopting it.**

Keywords—reliability; FinFET technology; process variability; soft error; mitigation.

I. Introduction and Motivation

The new features to maintain the pace of performance, less power consumption and higher density results in an increase of design complexity in advanced technologies with more potential sources of variability and charge sharing due to single event transients (SET). The small geometric patterns imposed by the sub-22nm technologies intensify the process variation as well as the higher density allows that a single energetic particle affects multiple adjacent nodes [1, 2].

The process variation represents a random deviation from the typical design specifications that stimulates the circuit degradation, abnormal power consumption, and performance divergence [3]. The main sources of process variations are the wavelength adopted in the lithography step and the use of high-k dielectrics to improve the gate control on the channel region. The soft error (SE) arises from the interaction of energetic particles with the silicon where the transient pulse generated may provoke non-restorable data loss. In general, more in-depth nanometer technologies are more susceptible to SE due to low supply voltages, reduced intrinsic capacitances, and higher-frequency operation [4]. However, the 3D structure of FinFET minimizes the volume of silicon exposed to the charge collection mechanism, and consequently, it decreases the SE susceptibility on these devices [5].

In the literature, most of the works involving process variation and radiation effects in FinFET technologies have been focused on the device and electrical levels. To the best of our knowledge, much less understanding has been gained at the physical level. Although the FinFET-based circuits under the reliability issues have been extensively evaluated, none of the related works presented solutions to improve the effects of process variability or to mitigate the radiation-induced soft errors in FinFET nodes at the physical level.

II. Thesis Objectives

The parameter yield loss and critical failures on system behavior are the major consequences of process variability and radiation-induced soft errors, respectively. For these reasons, considerable research efforts should be made to understand and reduce the impacts introduced by the reliability challenges. In this regard, the main goals addressed by this thesis are to:

I. Investigate the standard FinFET design under nominal behavior, under the effects of process variation and with the presence of the soft error;
II. Apply six circuit-level approaches on each FinFET design to mitigate the effects caused by process variation and soft error;
III. Evaluate the behavior of FinFET design of different levels of variation, transistor sizing and linear energy transfer (LET);
IV. Trace a trade-off between the gains and penalties of each approach regarding performance, power, area, SET cross-section, and SET pulse width;
V. Provide an overall comparison between the all techniques applied in this work.

III. Methodology

This work adopts a free 7-nm FinFET process design kit (PDK) developed by ASU in partnership with ARM Ltd [6]. Each cell is submitted to the physical design, verification flow, and parasitic extraction. First, all these steps are executed considering the standard version of the gate, and after, inserting each technique in the FinFET designs. The work-function fluctuation (WFF) is modeled as a Gaussian function with 3-sigma of deviation. Process variability is inserted through 2000 Monte Carlo simulations carried out in Spectre from Cadence. The normalized standard deviation (σ/μ) is used to indicate the sensitivity of gates to the process variability. The SE weakness is evaluated using the MUSCA SEP3 tool developed by ONERA [7]. This prediction tool is based on a Monte Carlo method that deals both with the layout characteristics and the electrical properties of devices. This work studies heavy ion irradiation at normal incidence, room temperature, and with the supply voltage varying from 0.7V down to 0.3V. All current sources in the SET database were injected, considering the most susceptible input vector of each logic gate to obtain the SE estimations. A fault is detected if the voltage amplitude of the impacted node exceeds the gate threshold voltage ($V_{DD}/2$).

IV. Thesis Contributions

As a strategy to obtain the goals of proposed mitigation techniques, this work starts by evaluating three circuit-level methods as a manner to attenuate the effects of process variability and soft error susceptibility: transistor reordering [8, 9], the use of decoupling cells [10] and sleep transistors [11]. Transistor reordering technique consists of placing the serial transistors of a given network in different positions in the schematics keeping the same logic function. The adoption of decoupling cells in the circuit output is a capacitive approach to reduce the noise on signal lines and to increase the critical charge of the output node. The addition of sleep transistor between the pull-down network and the ground rail is a power-gating technique which acts as a supply-voltage regulator.

Fig. 1 shows the impact of process variability on power and worst-case delay of the AOI21 gate. Following most of the standard cell libraries, the standard version of this work is built with the serial transistor close to the gate output. The transistor reordering for the AOI21 gate consisted in placing the serial transistor far to the output. The adoption of far topology showed results very similar to the standard version where the variability mitigation is 2% for power and 0.5% for the worst-case delay in average, respectively. The insertion of decoupling cells in the gate output is very promising to attenuate the delay variability, independently of the level of WFF applied. The AOI21 gate can reach up to 6.7% of attenuation of delay variability using this technique. On the other hand, the use of decoupling cells to minimize the power variability is only advantageous for levels of WFF above 4%. Among the three circuit-level techniques already evaluated, the best approach to attenuate the effects of process variability is the addition of sleep transistors. The AOI21 gate can reach at least 37.3% of delay attenuation with variations of 5% from WFF. This intensifies when lower levels of WFF were investigated, obtaining 51.8% of improvements with variations of 1% from nominal WFF values. For the power variability, the mitigation is between 3.2% and 8.5% depending of the level of WFF variation. Higher levels of WFF (5%) presented the best results of power attenuation.

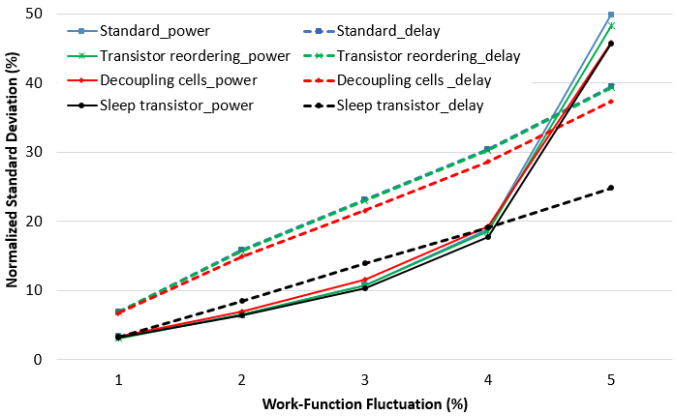

Fig. 1. Impact of different levels of WFF on the power of the AOI21 gate in the standard version and using circuit-level techniques

The circuit-level techniques were also evaluated with different transistor sizing. The process variability robustness increases when larger (4 or 5 fins) decoupling cells or sleep transistors were adopted. However, independently of the application, a trade-off always needs to be done for applying the mitigation techniques in the circuits due to power, performance, and area penalties.

The cross section was the metric chosen to estimate the soft error susceptibility in this work. The results of the AOI21 gate operating at near-threshold regime (0.3V) with the transistor reordering technique are shown in Fig. 2. The standard topology (close) shows to be less sensitive than far topology for all levels of LET investigated. The SE susceptibility keeping the close topology decreases around 20%, 37%, 24%, and 5% for LETs equal to 10, 20, 30, and 58 MeV.cm².mg^{-1}, respectively. For 0.4V, the close topology is free of faults while some faults can still be seen at the output with the far topology. None events were observed on the range from 0.5V to 0.7V due to the FinFET devices presents attractive properties to control the SE. The use of decoupling cells is also advantageous for fault mitigation, where the AOI21 gate present a decrease of SE susceptibility around 2.6%, 3.7% and 9.8% for LETs equal to 15, 20 and 58 MeV.cm².mg^{-1}, respectively.

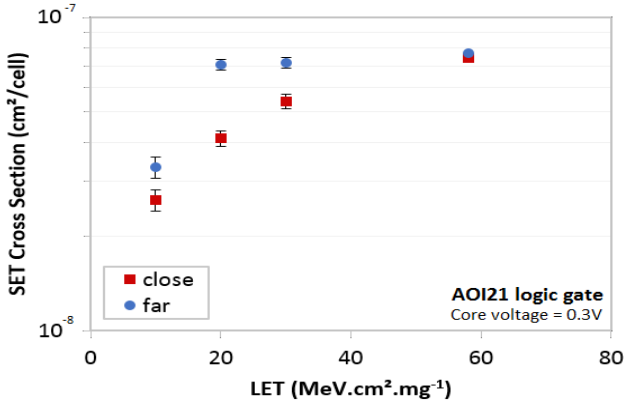

Fig. 2. SET cross section of AOI21 gate with transistor reordering technique under different LETs

This work only presented the results for the AOI21 gate, but same tendency of behavior also was seen for a set of logic gates. In addition to a more detailed analysis of the data obtained, the next step includes evaluating more three techniques: Schmitt Trigger, transistor folding, and dual gate pitch.

Acknowledgements

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