Externally Tested Scan Circuit With Built-In Activity Monitor and Adaptive Test Clock

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Abstract—We reduce the test time of external test applied from an automatic test equipment (ATE) by speeding up low activity cycles without exceeding the specified peak power budget. An activity monitor is implemented as hardware or as presimulated and stored test data for this purpose. The achieved test time reduction depends upon the input and output activity factors, α_{in} and α_{out} , of the scan chain. When on-circuit built-in hardware control is used, test time reductions of about 50% and 25% are possible for vectors with low input activity ($\alpha_{in}\approx 0$) and moderate input activity ($\alpha_{in}=0.5$), respectively, in ITC02 benchmark circuits. When stored pre-simulated test data is used, test time reduction of up to 99% is shown for vectors with low input and output activities.

I. INTRODUCTION

Reducing the time of scan testing while keeping the power consumption low is a challenging problem. A recent proposal [6], [7] suggests dynamic control of scan clock frequency in both self test and externally tested scan circuits. It is assumed that the circuit activity is proportional to the activity in the scan register. The slowest scan clock is determined under the assumption of maximum activity, i,e., every flipflop toggling at every clock. In this paper, we relax that assumption. We propose techniques to reduce test time in externally tested scan circuits through dynamic control of scan clock frequency for which peak activity factor may or may not be pre-computed. The test time reduction achieved is better than those of prior proposals [6], [7].

Section II discusses implementations of the proposed technique. Section III gives a mathematical analysis of the scheme. Section IV explains the experimental results obtained. Section V discusses the conclusions drawn from this work.

II. IMPLEMENTATION

During external test [4], an automatic test equipment (ATE) applies test patterns through scan-in pin(s) of the circuit and receives the response through scan-out pin(s). The expected response of the good circuit under test (CUT) are stored in the ATE and the CUT passes if every response matches the expected response. The clock frequency at which test patterns are scanned in can be varied based on the activity (signal transitions) the patterns produce to control the power consumption of the CUT.

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A. Using hardware control

In this technique, hardware is used to dynamically control the scan clock frequency. This hardware can be either added on-chip or kept off-chip on external test fixture mounted on the ATE. We define the *activity factor* α for a signal as the average number of transitions per clock that signal makes. Thus, for a clock signal, $\alpha=2$. For a glitch-free non-clock signal, $\alpha\leq 1.0$, attaining a peak value (α_{peak}) of 1.0.

- 1) Circuits with single scan chain and $\alpha_{peak}=1$: We consider a design with a single scan chain and assume that every pattern captured in the scan chain potentially generates the worst-case activity upon scan-out. So, the scan begins with the slowest clock. Scan-in bits are monitored and allow speed up of clock. Implementations of such a scheme for external test [6] and for self-test [7] may be found in recent papers.
- 2) Circuits with multiple scan chains and $\alpha_{peak}=1$: Here the scan-in transitions for all chains are monitored and their combined count is used to control the scan clock frequency. Details of such a scheme are available in recent documents [5], [6].
- 3) Circuits with single scan chain and $\alpha_{peak} < 1$: The two cases mentioned above work well when the captured data causes close to peak activity, $\alpha_{peak} = 1$, in the scan register. However, it is unreasonable to expect that all captures will correspond to this worst case. In general, scan clock frequency can be computed based on a peak activity factor (α_{peak}) lower than 1, which may be determined from simulation or analysis. That leads to a new type of design [5] as proposed in this paper.

Given a value of the peak scan chain activity α_{peak} due to captured values, the slowest scan clock frequency is given by [5]–[7]:

$$f_{test} = \frac{2P_{budget}}{\alpha_{peak}CV^2} \tag{1}$$

where P_{budget} is the maximum power that a good circuit can consume during test without malfunctioning, C is the total node capacitance for all gates, and V is the supply voltage. For the conventional, non-adaptive, scan test the entire testing will be done with a clock of constant frequency, f_{test} .

Figure 1 shows an adaptive clock implementation for single scan chain and peak activity factors less than 1. The activity monitor comprises of an XNOR gate connected between the input and output of the first flip-flop, and an XNOR gate

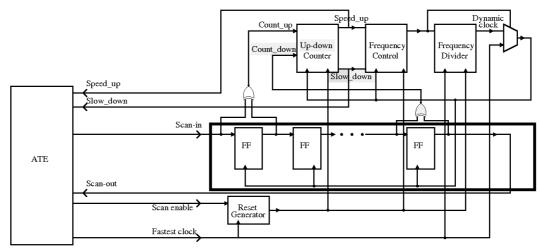


Fig. 1. Implementation in single scan chain circuits, $\alpha_{peak} < 1$.

connected between the input and output of the last flip-flop. The former monitors the number of non-transitions entering the scan chain and the latter monitors the number of non-transitions leaving the scan chain. An up-down counter keeps track of the number of non-transitions in the scan chain. Thus, the input XNOR drives the count_up signal and the output XNOR drives the count_down signal of the up-down counter. The increase in the number of non-transitions in the scan chain during scan-in is the difference between those entering the scan chain and those leaving the scan chain.

The up-down counter is reset to 0 at the start of each scanin. When a non-transition enters the scan chain, the counter counts up and when a non-transition leaves the scan chain, the counter counts down. When the counter counts up to a certain threshold value, the speed_up signal is set to 1 for one clock cycle, the frequency control block increases the frequency of scan clock and the counter is reset to 0. Similarly, when the counter counts down to 0, the slow_down signal is set to 1 for one clock cycle, the frequency control block lowers the frequency of scan clock and the counter is reset to the threshold value. Thus, whenever the number of non-transitions in the scan chain increases, the frequency is increased and when the number reduces, the frequency is decreased. The rest of the circuitry functions the same as in the scheme where the peak activity factor is 1 [5]–[7].

As shown in Figure 1, the ATE supplies a *fastest clock* whose frequency is determined from the circuit characteristics such as the functional or structural critical path delay and the fastest possible operation of the scan register. The circuit can run at this clock frequency if there were no power constraints. The adaptive scan would use this frequency when the activity drops almost to zero.

A *slowest clock* frequency is determined from power considerations according to Eq. 1. The largest frequency division ratio in the frequency divider of Figure 1 generates the slowest clock from the ATE-supplied fastest clock.

At the start of scan-in of a vector, the slowest clock is employed since the activity factor of the vector captured in the scan chain before the start of scan-in is assumed to be α_{peak} . In this design, scan clock frequency is never increased beyond the fastest clock or decreased below the slowest clock regardless of the signal from the counter.

The implementation of Figure 1 is general and can be customized for $\alpha_{peak} = 1$ by removing the XNOR gate from the flip-flop at the end of the scan chain and tying the count_down signal of the up-down counter to 0. That leads to the previous designs [6], [7].

During testing a two-way data transfer occurs between the ATE and CUT. Test inputs flow from the ATE to CUT and CUT responses flow to ATE. In synchronization with the fastest clock provided by the ATE, the CUT generates its own adaptive clock using speed_up and slow_down signals. These two signals are sent from CUT to ATE so that it can send and receive data at the adaptive clock rate.

4) Circuits with multiple scan chains and $\alpha_{peak} < 1$: When CUT has multiple scan chains, the activity of all chains must be monitored. XNOR gates are added across the input and output of the first flip-flop and across the input and output of the last flip-flop in every scan chain. The outputs of the XNOR gates at the inputs of the scan chains are fed to the count up inputs of a parallel counter [9] which counts up by the number of 1s at its count_up inputs. Similarly, the outputs of the XNOR gates at the ends of scan chains are fed to the count down inputs of the same parallel counter that counts down by the number of 1s at its count down inputs. The rest of the circuitry remains unaltered and still resembles Figure 1. When the count reaches a certain threshold value, the frequency is stepped up and the counter is reset to 0. When the count reaches 0, the frequency is stepped down and the counter is reset to the threshold value. Except for the use of the parallel counter this control scheme is similar to that of Figure 1.

The case of multiple chains with $\alpha_{peak}=1$ assumption has been discussed before [5], [7]. It requires only one XNOR per scan chain and a parallel up counter.

B. Using pre-simulated and stored test data

An alternative to the hardware control is a dynamically controlled scan clock through the use of pre-simulated and stored test data. The clock frequencies at which test patterns should be applied can be found based on activity factors of the input bits and that of the response bits. This information is then stored in the test program. Since the expected response and the input scan bits are given in the test program, the activity in the scan chain is know accurately in every clock cycle. Thus, the test time can be optimized much more effectively compared to the hardware control technique described earlier.

C. Using a combination of hardware control, and presimulated and stored test data techniques

Two techniques to reduce test time in scan circuits, one using hardware control and the other using pre-simulated and stored test data, have been described above. Though both effectively reduce test time, each has its own drawbacks. The hardware control technique has lower reduction in test time while the pre-simulated and stored test data technique increases test data volume, which now includes additional control bits, and requires regeneration of control bits every time a test pattern is modified.

To utilize the benefits of both techniques, we propose a combination. The activity factor of the captured response bits is used to determine the clock frequency with which the next test pattern scan-in should begin. This information is pre-stored with test data and is sent by ATE to the counter and frequency control block in CUT so that they are reset appropriately at the start of each scan-in. The hardware then monitors the activity in the subsequent scan-in cycles. Thus, the activity in the scan chain for every clock cycle is precisely known without tremendous increase in test data volume. If a test pattern is modified, the initial scan frequency for that pattern can be set to the lowest scan clock frequency without compromising heavily on test time reduction.

III. ANALYSIS

Let α_{peak} be the peak activity factor of the test vectors, α_{in} be the activity factor of the scan-in vector, α_{out} be the activity factor of the vector captured in the scan chain prior to scan-in, and v be the number of frequencies. The period T of the fastest scan clock is v times shorter than the slowest clock. Thus, the period of the slowest clock is vT. If the vectors were scanned in with the slowest clock, the total scan-in time per vector would be NvT, where N is the number of flip-flops in the scan chain. Some details are omitted in the following analysis due to space limitation. The reader may refer to a recent report [5].

We estimate the reduction in test time assuming that the majority of time is spent in scanning. The non-adaptive (conventional) test runs with the slowest clock giving a reference scan time per test as NvT. Thus,

Test time reduction =
$$\frac{NvT - \text{Adaptive clock scanin time}}{NvT}$$

TABLE I

SCAN-IN TIME REDUCTION VS. NUMBER OF SCAN CLOCK SPEEDS FOR ACTIVITY FACTOR $\alpha_{+-} = 0.5$

ACTIVITI FACTOR $\alpha_{in} = 0.5$.						
Number of scan	Test time reduction (%)					
clock speeds, v	Simulation	Eq. 4				
1	0.00	0.00				
2	0.34	0.00				
4	12.64	12.50				
8	18.78	18.75				
16	22.03	21.88				
32	23.56	23.44				
64	25.17	24.22				
128	27.41	24.61				

A. Using hardware control

In this technique, scan-in of vectors initially begins with the slowest clock frequency, which is gradually increased in steps based on the activity factor of the scan-in vector.

I) $\alpha_{peak} < 1$: This analysis considers uniform α_{in} and α_{out} . Thus, if $\alpha_{in} > \alpha_{out}$ the number of non-transitions in the scan chain never decreases and hence there will be no change in scan clock frequency. However, if $\alpha_{in} < \alpha_{out}$, the number of non-transitions in the scan chain increases and the scan clock frequency is continuously increased. The scanin speed of test vectors, starting at the slowest clock rate, is continuously increased. The test time reduction for this model is given by,

Test time reduction =
$$\frac{\alpha_{out} - \alpha_{in}}{2\alpha_{peak}} - \frac{1}{2v}$$
 (3)

2) $\alpha_{peak}=1$: In this model, the scan chain is assumed to be filled with most transitions prior to scan-in and hence, the scan-in vector is assumed to be the sole contributor of non-transitions in the scan chain. These non-transitions enter the scan chain at a rate of $(1-\alpha_{in})$ per cycle. The reduction in test time for this model is given by,

Test time reduction =
$$\frac{1 - \alpha_{in}}{2} - \frac{1}{2v}$$
 (4)

A C program was written to generate random vectors for a circuit with 1,000 flip-flops. The test time reduction for these vectors was estimated, and compared with the values obtained from the formula. Table I shows the test time reduction versus number of frequencies for scan-in bit activity factor $\alpha_{in}=0.5$. Table II shows the variation of test time reduction with activity factor when the number of frequencies v=8. Both tables compare the test times estimated for random vectors (column 2), with those obtained from Eq. 4 (column 3).

It can be observed from Tables I and II that for a chosen number of frequencies, vectors with lower transition densities achieve higher reduction in scan-in time. Also, the test time reduction increases as more frequencies are used. The scan-in time reduces rapidly until 8 frequencies after which the reduction becomes gradual.

B. Using pre-simulated and stored test data

If the pre-simulated and stored test data technique is used, the activity in the scan chain is precisely known in every clock

TABLE II SCAN-IN TIME REDUCTION VS. ACTIVITY FACTOR α_{in} for v=8 scan-in clock speeds.

Activity	Test time reduction (%)				
factor, α_{in}	Simulation	Eq. 4			
0	43.75	43.75			
0.1	38.63	38.75			
0.2	34.00	33.75			
0.3	28.97	28.75			
0.4	23.51	23.75			
0.5	18.78	18.75			
0.6	14.92	13.75			
0.7	9.60	8.75			
0.8	4.79	3.75			
0.9	0.00	0.00			
1	0.00	0.00			

cycle. Thus, the scan-in of every test pattern need not be started with the slowest clock frequency. Assuming that the scan-in vector has a uniform activity factor (α_{in}) that is higher than the activity (α_{out}) produced by the captured vector, the number of non-transitions entering the scan chain will be lower than that leaving it and hence the scan clock frequency is continuously decreased. However, if α_{in} lower than α_{out} , then the scan clock frequency will be continuously increased.

1) Case 1: $\alpha_{in} < \alpha_{out}$: The test time reduction is [5],

$$\frac{\left(\left(\alpha_{peak} - \alpha_{in}\right) + \left(\alpha_{peak} - \alpha_{out}\right)\right)}{2\alpha_{peak}} - \frac{1}{2v} \tag{5}$$

This formula can be extended to the implementation discussed in the previous subsection as well. If the peak activity factor is assumed to be 1, then the activity factor of the captured vector is also 1, i.e., $\alpha_{out}=\alpha_{peak}=1$. The test time reduction is,

$$\frac{(1-\alpha_{in})}{2} - \frac{1}{2v} \tag{6}$$

which is the same as that obtained earlier.

2) Case 2: $\alpha_{in} > \alpha_{out}$: The test time reduction is,

$$\frac{\left(\left(\alpha_{peak} - \alpha_{in}\right) + \left(\alpha_{peak} - \alpha_{out}\right)\right)}{2\alpha_{peak}} + \frac{1}{2v} \tag{7}$$

IV. ATE EXPERIMENTS

A. Verification of BIST

The test times for ISCAS89 benchmark circuits were examined using the Advantest T2000GS ATE. In order to dynamically control the scan clock frequency using hardware control technique, a modification in the ATE software is essential. Without this modification, test patterns cannot be applied to the CUT at a dynamically changing clock rate. To overcome this obstacle, we generated the patterns on-chip using a test-per-scan BIST scheme.

In verilog netlists of the ISCAS89 benchmark circuits flipflops were added at all primary inputs and primary outputs. All flip-flops were converted to scan types and chained together. Thus, the number of flip-flops in the circuit is the sum of the number of primary inputs, number of primary outputs and number of D-type flip-flops. A 23-bit linear feedback shift

TABLE III REDUCTION IN TEST TIME FOR ISCAS89 CIRCUITS - SINGLE SCAN CHAIN, $\alpha_{peak}=1$.

Circuit	Number of	Number of	Test time	Increase in
	scan flip-flops	frequencies, v	reduction (%)	area (%)
s27	8	2	7.49	14.72
s298	23	4	14.57	16.25
s386	20	4	15.25	15.29
s9234	286	4	14.01	5.82
s13207	852	8	19.00	3.98
s38584	1768	8	18.91	2.13

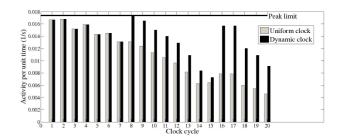


Fig. 2. Activity vs. number of clock cycle for s386 circuit.

register (LFSR), a 23-bit signature analysis register (SAR), and a test-per-scan BIST controller were implemented [1], [8]. A single bit output of the LFSR supplied the scan input and the scan output was fed into the SAR. The counter, frequency control circuitry, and frequency divider circuitry for dynamic frequency control were implemented as shown in the unshaded portion of Figure 1. The number of frequencies for each circuit was chosen according to the size of the circuit or the number of scan flip-flops. A suitable number for random patterns to achieve sufficient fault coverage for each circuit as mentioned in [3] was incorporated in the BIST controller.

The circuits were implemented with and without the dynamic frequency control circuitry on CycloneII FPGAs. The clock signal to the FPGA was supplied from the Advantest T2000GS ATE. The time required for test application with and without dynamic scan clock frequency control was recorded in each case. DesignCompiler, a synthesis tool from Synopsys, was used to analyze the area of the circuits with and without the dynamic frequency control circuitry.

Table III shows the results. The number of frequencies chosen for each circuit is shown in column 3. The percentage reduction in test time with respect to the test time for the core circuit is shown in column 4 and the percentage increase in area with respect to the area of the core circuit is shown in column 5.

Since an LFSR generates pseudo-random patterns, it is safe to assume that the input activity factor of the test patterns is around 0.5. It can be seen that the results conform to the theoretical values shown in Table I.

At any node, the capacitance and the voltage are constant. Therefore, power dissipated at the node is proportional to the product of activity and frequency. Hence, the activity per unit time is a direct measure of power dissipated in the circuit. Therefore, an analysis to find activity per unit time

was performed on the s386 benchmark circuit. The Synopsys power analysis tool, PrimeTime PX, was used. The activity per unit time in every cycle was found for the circuit for a scan vector with an activity factor of 1. The peak among these values was set as the limit for activity per unit time. The values of activity per unit time for the circuit in every cycle were found for a vector with an activity factor of 0.25 using uniform clock and dynamic clock, respectively. The results are shown in Figure 2. Notably, the activity per unit time in every cycle is closer to the peak limit when dynamic clock method is used. Also, the peak limit is never exceeded in either case. A reduction of 11.25% was observed with the dynamic clock method.

The results for multiple scan chain implementation would be very similar to that obtained for single scan chain. The test time will not vary much since the activity of the circuit will be very similar in both single and multiple chain implementations. However, there would be a marginal increase in area due to the additional XNOR gates at the first flip-flop of every scan chain and also due to the use of a parallel counter as opposed to the simple counter used for the single scan chain.

These results for reduction in test time conform to the theoretical results given in Tables I and II. Two trends are clearly observed in Table III. As circuit size increases, the area overhead drops and test time reduction improves. These circuits are not very large from today's standard and we can expect better results as predicted by the analysis.

B. External ATE Test

1) Using hardware control:

 $\alpha_{peak}=1$: In order to estimate the test time reduction for larger circuits, an accurate mathematical analysis was applied to ITC02 circuits. Test vectors with different activity factors $(\alpha_{in}\approx 0,\,\alpha_{in}=0.5$ and $\alpha_{in}\approx 1)$ were generated. Test vectors were generated randomly to achieve $\alpha_{in}=0.5$. In order to generate test vectors with low activity factors $(\alpha_{in}\approx 0)$, one transition was randomly placed per test vector. Test vectors with high activity factors $(\alpha_{in}\approx 1)$ were generated to resemble clock signals. The analysis was performed assuming that the peak activity factor (α_{peak}) was 1.

The test time reduction with the proposed implementation was computed for the generated test vectors. Table IV shows the results. The number of scan flip-flops in column 2 is the sum of number of inputs, number of outputs and number of flip-flops. The number of frequencies for circuits are shown in column 3. The test time reductions achieved for best, moderate and worst case activity factors are shown in columns 4, 5 and 6, respectively. A simulation tool was not used for these circuits due to the large sizes of the circuits. However, it is important to note that any simulation tool would produce the same results since the input activity at the scan chain was closely monitored during estimation of test time. Evidently, more test time reduction can be achieved in larger circuits. The reduction in test time varies from 0% for patterns causing very high activity to 50% for patterns with almost no activity.

TABLE IV $\label{eq:table_total} \text{Test time reduction for ITC02 circuits, } \alpha_{peak} = 1.$

Circuit	Scan	Number of	Test time reduction (%)			
	flip-flops	clock freq.	$\alpha_{in} \approx 0$	$\alpha_{in} = 0.5$	$\alpha_{in} \approx 1$	
u226	1416	8	46.68	18.75	0	
d281	3813	16	46.74	21.81	0	
h953	5586	32	48.32	23.38	0	
f2126	15593	64	49.15	24.18	0	
p34392	23005	128	49.53	24.57	0	
t512505	76714	512	49.85	24.87	0	
a586710	41411	256	49.73	24.77	0	

Table V Test time reduction for T512505 circuit, $\alpha_{peak} < 1.$

	$lpha_{out}$									
α_{in}	0	0.1	0.2	0.3	0.4	0.5	0.6	0.65		
0	0	7.59	15.29	22.98	30.67	38.36	46.06	49.9		
0.1	0	0	7.59	15.29	22.98	30.67	38.36	42.21		
0.2	0	0	0	7.59	15.29	22.98	30.67	34.52		
0.3	0	0	0	0	7.59	15.29	22.98	26.83		
0.4	0	0	0	0	0	7.59	15.29	19.13		
0.5	0	0	0	0	0	0	7.59	11.44		
0.6	0	0	0	0	0	0	0	3.75		
0.65	0	0	0	0	0	0	0	0		

 $\alpha_{peak} < 1$: In order to estimate the reduction in scan-in time achieved with the model proposed for dynamic scan clock frequency control in circuits with peak activity factors lower than 1, the t512505 ITC02 benchmark circuit was chosen. This circuit is large enough to employ 512 different scan clock frequencies because it has 76714 scan flip-flops.

The pattern sets of various large benchmark circuits were studied to analyze trends in peak activity factors. The mean value of peak activity factor (α_{peak}) in these pattern sets was found to be around 0.57 and the standard deviation (σ) was around 0.025. The value of mean + 3σ was found to be around 0.65. This indicates that the probability that the peak activity factor of the test patterns of a circuit would lie below 0.65 is 99.7%. Therefore, the peak activity factor for the t512505 circuit was set at 0.65. The pattern sets generated by TetraMAX ATPG for large benchmark circuits were analyzed and it was found that the peak activity factor in these test vectors never exceeded 0.65. The value of 0.65 for peak activity factor can be used only for large circuits having flipflop numbers in the range of a several hundred. For smaller circuits with flip-flop numbers on an order of a few tens, the peak activity factor was found to be 1.

Accurate mathematical analysis was used to estimate the reduction in scan-in time achieved for the t512505 circuit when $\alpha_{peak}=0.65$ and 512 frequency steps are used. The activity factor of the captured vector was assumed to be 0.65 and the activity was monitored at the input and output of the scan chain. Test vectors with different activity factors ranging from 0 to 0.65 were generated and the test time reduction obtained using the proposed implementation was determined for these vectors. The results are listed in Table V. It shows the variation of scan-in time reduction as a function of α_{in} and α_{out} . Table V shows that when the activity factor of the scan-out vector (α_{in}) is greater or equal to the activity factor of the captured vector (α_{out}) , there is no reduction in scan-

in time. The frequency is increased only when the number of non-transitions in the scan chain increases. However, when $\alpha_{in}>\alpha_{out}$ the number of non-transitions (as counted by the counter) never increases and hence the scan-in is carried out at the starting frequency which is the frequency employed when dynamic scan clock frequency control is not implemented. Thus, the reduction in scan-in time is 0% in such cases.

Table V indicates that scan-in time reduction is greater for smaller values of α_{in} and for higher values of α_{out} . This can be explained from the perspective of number of non-transitions in the scan chain. If α_{in} is low, the number of non-transitions entering the scan chain is high and if α_{out} is high, the number of non-transitions leaving the scan chain is low. Thus, the net number of non-transitions in the scan chain is high giving a higher reduction in scan-in time.

2) Using pre-simulated and stored test data: The reduction in scan-in time achieved in the t512505 circuit when pre-simulated and stored test data technique or a combination of hardware control, and pre-simulated and stored test data techniques is used was estimated through mathematical analysis. The results are listed in Table VI.

In Table VI, scan-in time reduction is more for smaller α_{in} and α_{out} . When α_{in} is low, more non-transitions enter the scan chain and the counter counts faster. Thus, the reduction in scan-in time is higher. When α_{out} is low, the frequency at which scan-in begins is low since the frequency is predetermined based on the activity factor of the captured vector. Thus, there is a larger reduction in scan-in time.

This technique performs well due to the availability of information about the number of transitions or non-transitions present in the scan chain in every cycle. This increases the efficiency of the dynamic scan clock frequency control technique and results in greater reduction of scan-in time.

C. Justification

When an ATPG tool is used to generate test vectors for external tests, the vectors may have very few care bits. The don't care bits can be filled in using heuristics [2] to minimize scan transitions. Then, a dynamic control of scan clock will provide a large reduction in test time. This is illustrated using the ISCAS89 benchmark s38584. The Synopsys ATPG tool TetraMAX was used to generate two sets of vectors, a set of 961 vectors with no don't care bits and another set of 14,196 vectors with don't care bits. The vector set without don't cares was found to have an activity factor around 0.5 and the vector set with don't care bits had a low activity factor around 0.01 when care bits were filled using a minimum transition heuristic [2]. Test time reductions of 18.8% and 43.14% were achieved in the circuits with and without don't care bits, respectively.

In a different scenario, a test set may initially contain few (say, 10%) high activity ($\alpha_{in}=0.5$) vectors. These resemble fully-specified random vectors and achieve about 70-75% fault coverage. The latter 90% vectors then detect about 20-25% hard-to-detect faults and contain many don't cares, which may

	1									
		$lpha_{out}$								
α_{in}	0	0.1	0.2	0.3	0.4	0.5	0.6	0.65		
0	99.8	92.2	84.5	76.8	69.1	61.4	53.8	49.9		
0.1	92.4	84.7	76.8	69.1	61.4	53.8	46.1	42.2		
0.2	84.7	77.0	69.3	61.4	53.8	46.1	38.4	34.5		
0.3	77.0	69.3	61.6	53.9	46.1	38.4	30.7	26.8		
0.4	69.3	61.6	53.9	46.3	38.6	30.7	23.0	19.1		
0.5	61.6	53.9	46.3	38.6	30.9	23.2	15.3	11.4		
0.6	53.9	46.3	38.6	30.9	23.2	15.5	7.8	3.8		
0.65	50.1	42.4	34.7	27.0	19.3	11.6	3.9	0		

be filled in for reduced ($\alpha_{in} \leq 0.05$) activity. The dynamic scan clock control technique will be potentially beneficial.

V. CONCLUSION

The adaptive test in externally tested scan circuits dynamically varies the scan clock frequency. This achieved reduction in test times on all ISCAS89 benchmark circuits. Notably, the area overhead of the built-in circuitry is low. A test time reduction of about 19% was achieved using test-per-scan BIST system tested with Advantest T2000GS tester. An analysis on ITC02 benchmark circuits with on-chip hardware showed a test time reduction of 50% when scan vectors with very low activity ($\alpha \approx 0$) were used. For scan vectors with moderate activity ($\alpha = 0.5$), a test time reduction of 25% was observed. Higher reduction in test time was observed when pre-simulated and stored test data was used.

This work points to a deficiency in the present ATE test programming systems that do not allow interactive testing. A capability allowing the ATE to dynamically change the test startegy based on feedback from CUT will be beneficial.

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