

Reconfigurable Dual Mode IEEE 802.15.4 Digital Baseband Receiver for Diverse IoT Applications

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Abstract—IEEE 802.15.4 takes a center stage in IoT as Low-Rate Wireless Personal Area Networks (LR-WPANs). The standard specifies Offset Quadrature Phase Shift Keying Physical Layer (O-QPSK PHY) with half-sine pulse shaping which can be either analyzed under the class of M-ary PSK signals (QPSK signal with offset) or as Minimum Shift Keying (MSK) signal. M-ary PSK demodulation requires perfect carrier and has minimal error. MSK signals which falls under Continuous Phase Frequency Shift Keying can be demodulated non-coherently but error performance is not as good. In our paper, this dual nature of IEEE 802.15.4 PHY is exploited to propose a dual mode receiver comprising of QPSK demodulator chain and MSK demodulator chain as a single system on chip. The mode can be configured manually depending on the type of application or based on the feedback from a Signal to Noise (SNR) indicator employed in the proposed receiver. M-ary PSK chain is selected for lower SNRs and MSK for higher SNRs. Each of these properties are analyzed in detail for both demodulator chains and we go on to prove that MSK detection can be used for low power, low complex and low latency while QPSK detection is employed for minimal error.

Index Terms—IEEE 802.15.4 PHY, OQPSK demodulation, MSK demodulation, dual mode, adaptive modulation

I. INTRODUCTION

As IoT expands its reach across the various aspects of the physical world, we are slowly witnessing its integration within our daily life. In a short period of time, IoT has found manifold and diverse applications, ranging from health care to entertainment, banking to home automation, indoor and outdoor, mobile and stationery. IoT devices in each of these applications have their own constraints. Healthcare devices, for example, need to have minimum error-tolerance while power consumption may not be a constraint. Environment monitoring devices on other hand can be more error tolerant but should survive on batteries for a long duration. This paper proposes a single system on chip with dual mode for IEEE 802.15.4 receiver. The receiver can be configured manually based on the constraints of the application or from the feedback from the built-in SNR estimator.

IEEE 802.15.4 standard specifies Offset Quadrature Phase Shift Keying Physical Layer (OQPSK PHY) with Direct Sequence Spread Spectrum (DSSS) and half-sine pulse shaping [1]. OQPSK with half-sine pulse shaping is equivalent to Minimum Shift Keying (MSK) signal [2]. Thus, IEEE 802.15.4 PHY receiver can also be realized as Continuous

Phase Frequency Shift Keying (CPFSK) demodulator. MSK, being a special case of CPFSK, is demodulated non coherently. Thus, this type of demodulator do not need carrier frequency and phase synchronization.

As an alternative, at the receiver, I component of the O-QPSK signal is delayed by half a bit duration to match with Quadrature component and then fed to the M-ary PSK demodulator. The coherent QPSK demodulator, though complex to design has excellent error performance. For an optimum performance, M-ary PSK demodulator should be chosen when channel conditions are not favorable and MSK demodulator for high SNRs. The proposed receiver employs a simple SNR indicator based on the preamble to decide when to switch between the two demodulator chains. The SNR indicator observes the extent to which the received preamble differs from the reference preamble to predict the SNR.

MSK detectors has been used for IEEE 802.15.4 earlier. [3] demonstrates a simple low cost receiver using Asynchronous Zero Crossing Detector (AZCD) as a form of MSK detector. A Maximum Likelihood Estimation (MLE) based non-coherent MSK demodulation is studied in [4]. M-ary PSK demodulators with frequency offset synchronization has also been implemented in [5] and [6]. These detectors performs better in terms of error performance than the MSK detectors. A multi mode transceiver [7] has also been proposed earlier but it is designed for three different modulation schemes for IEEE 802.15.4. In this paper, a dual mode receiver is proposed where in the receiver can switch between demodulator chains and does not need the modulation scheme of the transmitter to change. The only improvisation in the transmitter is the differential encoding of the source bit stream. This is for the reason that differential encoded bits with OQPSK modulation and half sine pulse shaping is exactly equivalent to MSK modulation. If the QPSK demodulator chain is used at the receiver, a differential decoder is used to retrieve original bit stream. MSK demodulator need not use a differential decoder.

The paper is organized as follows, the proposed system architecture is discussed in section II. The flow of both the demodulator chain is explained in section III. The simulation results is under section III and Section IV concludes the paper with future scope.

II. PROPOSED SYSTEM ARCHITECTURE

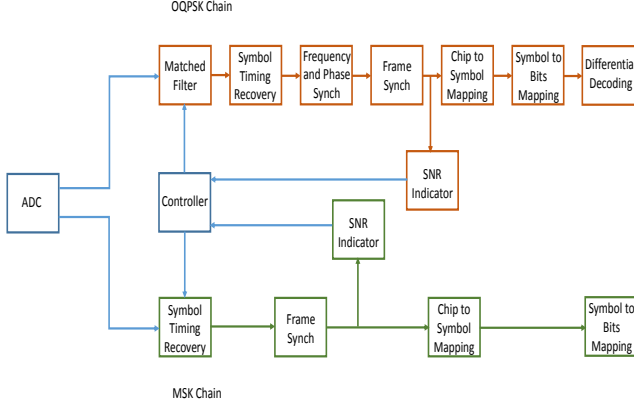


Fig. 1: Proposed IEEE 802.15.4 Dual Mode Receiver

The complete architecture of the proposed IEEE 802.15.4 receiver is shown in figure 1. Each of the chains have their own SNR Estimator that gives feedback to the controller. Based on this feedback, the controller directs the data stream from the ADC to one of the demodulator chains. The digital baseband signal with synchronization errors is given as:

$$z(t) = \exp(j(2\pi f_d t + \theta))s(t - \tau) + n(t) \quad (1)$$

where f_d is the frequency offset, θ is the phase offset, τ is the timing error, $s(t)$ is the modulated signal and $n(t)$ is Additive White Gaussian Noise (AWGN). As apparent from (1), the offsets and timing error should be compensated before decoding and decision.

The algorithms used in each of the demodulator chains is explained in the following sub sections.

A. IEEE 802.15.4 OQPSK Demodulator

The offset between In-phase and Quadrature-phase components of the OQPSK signal is removed by delaying the I component to align with Q component in the Symbol Timing Recovery block. The signal is then be fed to the QPSK demodulator.

1) *Matched Filter and Symbol Timing Recovery:* A discrete matched filter, $h[n]$ with coefficients equivalent to that of half-sine pulse shape is used to smoothen the pulse of both I and Q signals.

$$h[n] = \sin\left(\frac{\pi n}{NT_s}\right) \quad (2)$$

Since, the half-sine pulse is symmetric, $h^*[-n] = h[n]$.

Early Late Gate (ELG) Algorithm [8] is then applied for symbol timing recovery. ELG is a feedback synchronizer

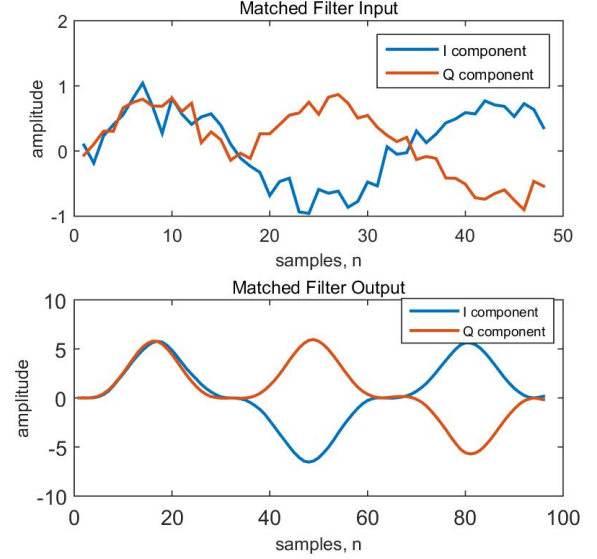


Fig. 2: Matched Filter Operation

and is usually carried on for a fixed number of pulses till an approximate timing interval is achieved. Two additional samples with the main sample is taken, namely early sample and late sample, E and L as shown in figure 3. The samples are shifted towards left or right in the next pulse till the main sample is found to be of greater amplitude than both E and L. If L is greater, samples are shifted right, else towards left.

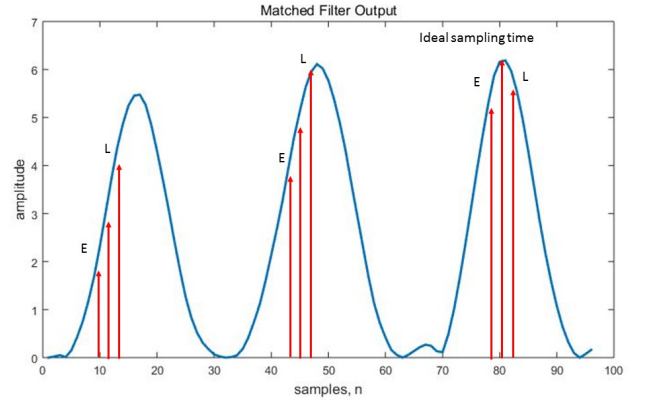


Fig. 3: Illustration of Early Late Gate Algorithm

2) *Carrier Frequency and Phase Synchronizer:* An excellent tutorial of Digital frequency offset estimators for M-ary PSK modulation is given in [9]. Both the Data Aided (DA) and Non Data Aided (NDA) estimators are explained. We have used NDA estimator because the frequency offset estimation is performed before frame synchronization in our receiver and hence preamble cannot be used before that. As discussed in the tutorial, R and B algorithm [10] is the most powerful estimator

even at low SNRs. Log likelihood function of NDA model of R and B algorithm is given by :

$$\Lambda_l = e^{-j\theta} \sum_{n=0}^{N_{fft}-1} z[n] e^{-j2\pi n f_d T} \quad (3)$$

where, $z[n] = e^{jM(2\pi n f_d T + \theta + \eta_n)}$

$M = 4$ in case of OQPSK and η_n is the phase of Gaussian noise, as stated in [9]

The estimates of frequency offset and phase offset is then evaluated as:

$$\hat{f}_d = \max \left\{ \left| \sum_{n=0}^{N_{fft}-1} z[n] e^{-j2\pi n f_d T} \right| \right\} \quad (4)$$

$$\hat{\theta} = \max \left\{ e^{-j\theta} \Delta(\hat{f}_d) \right\} \quad (5)$$

where, $\Delta(\hat{f}_d) = \sum_{n=0}^{N_{fft}-1} z[n] e^{-j2\pi n \hat{f}_d T}$

The performance of the estimator increases with high values of N_{fft} as shown in figure 4.

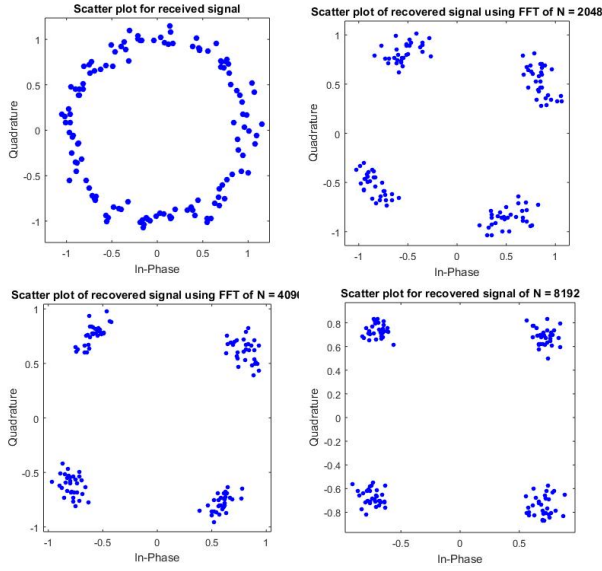


Fig. 4: Frequency and phase offset compensation for increasing values of N_{fft}

3) *Frame Synchronization*: As per the standard, IEEE 802.15.4 PHY layer packet has 32 zeros as a preamble. This 32 length preamble is converted to 8 symbols from bit to symbol mapping. Each of these symbols is then mapped to 32 bit chip sequence by DSSS, thus giving us a known preamble sequence of 256 bits or 128 QPSK symbols. A 128 symbol correlator is used to detect the preamble and synchronize the frame. The payload is then extracted and sent to *chip to symbol mapping* and then to *symbol to bit mapping*.

B. IEEE 802.15.4 MSK Demodulator

The MSK form of IEEE 802.15.4 baseband signal can be considered as :

$$z(t) = e^{j(\phi(t-\tau) + 2\pi f_d t + \theta)} \quad (6)$$

$$\phi(t) = 2\pi h \sum_k b_k q(t - kT) \quad (7)$$

$h = 0.5$ for MSK, b_k are symbols -1,1 derived from bits from I and Q components of OQPSK signal and $q(t)$ is given by:

$$q(t) = \begin{cases} 0, & t < 0 \\ t/2T, & 0 < t < T \\ 1/2, & t > T \end{cases} \quad (8)$$

The continuous phase of MSK signal, $\phi(t)$ can be seen in 5. The noisy received version is also shown. As discussed extensively in [2], the phase changes by $\pi/2$ or $-\pi/2$ for every transition of b_k .

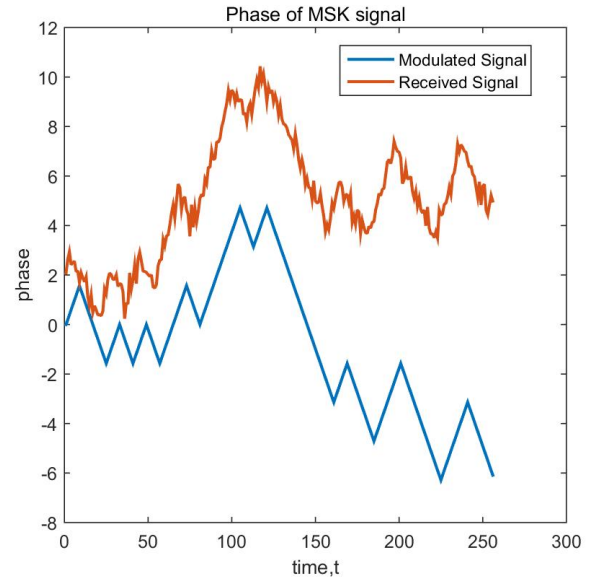


Fig. 5: Continuous phase of MSK

1) *Symbol Timing Recovery*: The algorithm proposed in [11] is used for timing correction. The non-linear transformation of received signal is taken and then averaged over large number of samples to evaluate the timing error, τ .

$$c_{n,i} = [z_{n,i} z_{n-1,i}^*]^2 \quad (9)$$

$$v_{n,i} = E\{c_{n,i}\} \quad (10)$$

The minimum timing error will occur at that value of i which gives maximum $|v_{n,i}|$

$$\hat{\tau} = \max_i \{|v_{n,i}|\} \quad (11)$$

where z_n is the discrete version of (7) and n is n^{th} symbol and i is the number of samples in one symbol.

2) *MSK Detection*: Differential Detection of MSK is performed to eliminate the effects of frequency and phase offsets. This approach was given by Tatsuro et. al in [12]. The sine of difference of $\phi(t)$ and $\phi(t - T)$ is evaluated and decision is made by checking the sample just before each transition. If the sample is above 0, the bit is taken to be 1, else it is taken to be 0. This is shown in figure 6. The bit stream is then sent to *chip to symbol* and *symbol to bit* mapping.

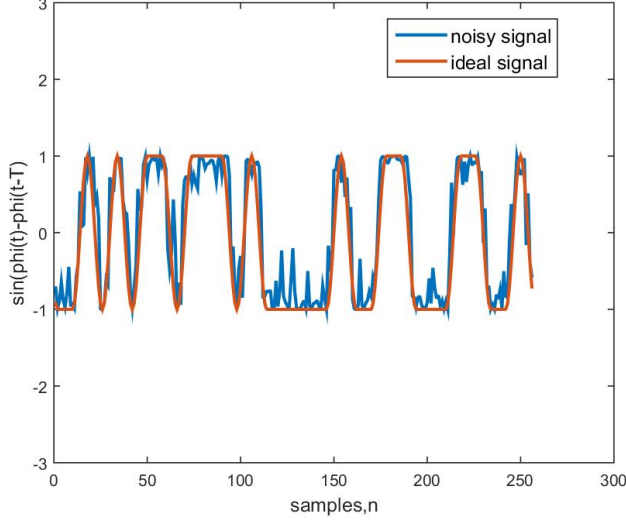


Fig. 6: Differential Detection of MSK

C. SNR Indicator

As a novel approach, Frame Synchronizer can be used as a crude indicator of SNR. Both the receiver chains need to match the chip sequence corresponding to 32 zeros for preamble detection. After the preamble is detected, a 256-bit comparator can be employed to match the received preamble sequence with original preamble sequence. A higher SNR will yield in more number of matching bits while lower SNRs degrade the comparator output. A threshold is set, output above the threshold indicates a good SNR and output below the threshold indicates a lower SNRs. QPSK demodulator is selected for lower SNRs and MSK demodulator for good SNRs. While one chain is processing, the other will sleep. This adaptive switching between the demodulator chains optimizes the performance of the receiver.

III. PERFORMANCE ANALYSIS AND SIMULATION RESULTS

A. Bit Error Rate Performance

As shown in figure 7, the QPSK demodulator clearly outperforms MSK demodulator. At bit error rate of 10^{-3} , there

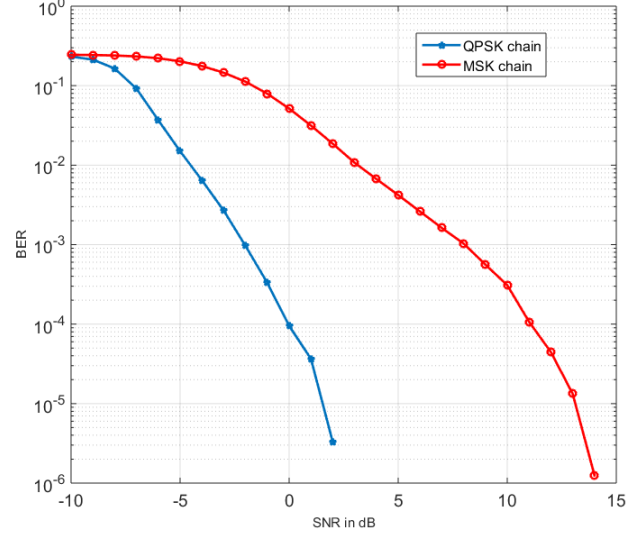


Fig. 7: BER performance of both the demodulators

is a huge difference of 16 dB between the two. High BER till $-10dB$ is observed due to the inability of demodulators to detect the preamble and synchronize the frame. Hence no further processing takes place and the packet is missed.

B. Complexity Analysis

The computational complexity of algorithms used in both the demodulator chains is given in the tables I and II.

L is the number of symbol pulses used for symbol timing recovery, N_{sample} is the number of samples per symbol pulse, $N_{preamble}$ is the number of preamble symbols considered, maximum of $N_{preamble}$ is 128 for QPSK and 256 for MSK, N_{bits} is the length of the transmitted bit stream and N_{fft} is the length of FFT performed in frequency offset estimation of QPSK signal.

As it is apparent from the tables that QPSK chain has higher complexity. For the values, $L = 32$, $N_{sample} = 16$, $N_{preamble} = 64$, $N_{bits} = 200$ and $N_{fft} = 2048$, MSK demodulator needs 29,793 additions and 6,144 multiplications while QPSK demodulator requires 104,617 additions and 40,695 multiplications.

Also, the operations like FFT and Matched Filter can't be implemented on-the-fly and needs sufficient memory for storage and processing. The read and write operations of the memory introduces large latency in the system. Power consumption also rises with usage of memory and more number of adders and multipliers.

Thus, MSK chain can be termed as low complex, low power and low latency demodulator while the QPSK chain can be seen as highly efficient and minimal error demodulator.

¹Cooley and Tukey Algorithm with radix-2

Algorithm	Mathematical Functions	Additions	Multiplications	Other Operations
Symbol Timing Recovery	Complex Multiplications & Complex number squaring	$L * N_{sample}/2 * 4$	$L * N_{sample}/2 * 8$	$N_{sample}/2 - 1$
Frame Synchronization	Real Cross Correlation	$(N_{preamble} - 1)^2$	$(N_{preamble})^2$	Nil
Chip to Symbol Mapping	XOR Operation	$(N_{bits}/4) * 31 * 16$	Nil	$N_{bits} * 128$ XOR & $(N_{bits}/4) * 15$ comparisons
Bit Detection	Nil	Nil	Nil	N_{bits} comparisons

TABLE I: Complexity Analysis of MSK Demodulator

Algorithm	Mathematical Functions	Additions	Multiplications	Other Operations
Matched Filter and Symbol Timing Recovery	Convolution	$L * 2 * (N_{sample} - 1)^2$	$L * 2 * (N_{sample})^2$	$L * 3$ comparisons
Frequency and Phase Synchronization	Fast Fourier Transform ¹	$7 \frac{N_{fft}}{2} \log(\frac{N_{fft}}{2}) - 5N_{fft} + 8$ [13]	$3 \frac{N_{fft}}{2} \log(\frac{N_{fft}}{2}) - 5N_{fft} + 8$ [13]	$1 * \arctan$
Frame Synchronization	Real Cross Correlation	$(N_{preamble} - 1)^2$	$(N_{preamble})^2$	Nil
Chip to Symbol Mapping	XOR Operation	$(N_{bits}/4) * 31 * 16$	Nil	$N_{bits} * 128$ XOR & $(N_{bits}/4) * 15$ comparisons
Bit Detection	Nil	Nil	Nil	N_{bits} comparisons

TABLE II: Complexity Analysis of QPSK Demodulator

IV. CONCLUSION AND FUTURE SCOPE

We have proposed a dual mode receiver for IEEE 802.15.4 and have shown that it can adapt to any application. The MSK detector can be selected for applications that needs to be in the network for a long duration and can compensate for few errors. Applications where latency is also a constraint can use this chain. On the other hand, QPSK detector gives efficient performance in terms of bit error rate. IoT applications where errors cannot be tolerated can be operated in this mode. Also, the receiver itself can switch between the modes using the SNR Indicator to optimize the performance and balance between power consumption, latency and error performance. The proposed receiver design can be implemented as a single system on chip and can deliver optimum performance for universal IoT applications.

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