Low-power high-accuracy micro-digital sun sensor by means of a CMOS image sensor

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Abstract. *A micro-digital sun sensor (μDSS) is a sun detector which senses a satellite's instant attitude angle with respect to the sun. The core of this sensor is a system-on-chip imaging chip which is referred to as APS+. The APS+ integrates a CMOS active pixel sensor (APS) array of* 368 × 368 pixels*, a 12-bit analog-to-digital converter, and digital signal processing circuits. The μDSS is designed particularly for microsatellite applications, thus low power consumption is the major design consideration. The APS+ reduces power consumption mainly with profiling and windowing methods which are facilitated by the specific active-pixel design. A prototype of the APS+ which is designed in a standard 0.18-μm CMOS process is presented. The APS+ consumes 21 mW at 10 fps, which is 10 times less than the state of the art. In order to improve noise performance, a reset noise reduction method, quadruple sampling (QS), is implemented. QS reduces the effect of the reset noise compared to the conventional delta double sampling method, even in a 3-transistor active pixel structure. The APS+ obtains an accuracy of 0.01 deg with the QS method. © 2013 SPIE and IS&T [DOI: 10.1117/1.JEI.22.3.033030]*

1 Introduction

Attitude sensors are widely used in the detection of an aircraft's orientation with respect to a frame of reference in space. They are classified into different categories according to the reference vectors they use, e.g., gyrocompasses, magnetometers, star trackers, and sun sensors.[1] Among these attitude sensors, sun sensors are characterized by their simple structure, low cost, and low power consumption. These characteristics make sun sensors attractive for microsatellite applications.

A microsatellite usually has a wet mass between 10 and 100 kg. The major design challenge for sun sensors used by a microsatellite is miniaturization. First of all, a system-on-chip (SoC) design for sun sensors is required in order to reduce mass and weight so that less additional firmware is needed. Second, since solar cells carried by microsatellites are relatively small, sun sensors should also consume low power due to the rigid power budget.

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Sun sensors can be classified as either analog or digital sun sensors.[2] A digital sun sensor usually has an imaging chip as the detector and determines the sun's incident angle based on the centroid of the projected image on the detector plane.[3] Digital sun sensors are intrinsically better than analog sun sensors in resolution, miniaturization, and immunity to the earth's albedo effect.[4,5,6] They can achieve an accuracy of several arc-minutes or better.

In this article, a micro-digital sun sensor (μDSS) specifically designed for microsatellite application is proposed. It achieves miniaturization by using an SoC sensor chip called APS+. The high performance of the APS+ enables the μDSS to satisfy all functional specifications such as resolution accuracy and the field of view (FOV) with very low power consumption. The design specifications of the APS+ are listed in Table 1.

1.1 *Working Principle of the μDSS*

The working principle of the μDSS is illustrated in Fig. 1. This sun sensor works as a pinhole camera: a lensless camera with an aperture simplified as a pinhole. To detect the respective angle between the satellite and the sun, the APS+ CMOS image sensor chip is used, and the sun is the point light source. The APS+ is placed on a substrate with a membrane above its focal plane. At the center of this membrane is a pinhole. The sunlight passes through the pinhole and projects an image on the image sensor pixel array. The sunlight incident angle (θ) can be obtained from the centroid position of the projected image on the focal plane of the sensor. Furthermore, the satellite's attitude can also be determined from the sunlight incident angle. The incident angle can be derived from the equation:

$$l = \tan\theta \times F \Rightarrow \theta = \arctan\left(\frac{l}{F}\right), \tag{1}$$

where l is the distance between the center of the pixel array and the sun spot centroid, and F is the focal length. Equation (1) shows that the accuracy of the incident angle is proportional to the accuracy of the sun spot centroid calculation. Thus, the sensor chip of the APS+, which is capable

Table 1 Design specifications of the APS+.

Specification	Number	Unit
Pixel pitch	6.5	μm
Pixel array	368 × 368	pixel
Power	<100	mW
Field of view	±50	deg
Accuracy	0.1 (3σ)	deg

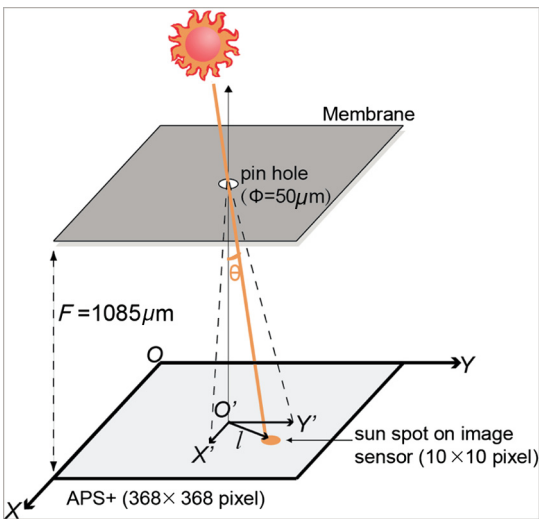

Fig. 1 System sketch of the micro-digital sun sensor (μDSS).

of accurately determining the sun spot's centroid, is a critical component of the sun sensor system.

1.2 *System Architecture*

The final goal of the μDSS is to have a fully autonomous and a wireless sun sensor in a package, integrated with a power supply unit and a communication unit. The μDSS consists of three major functional blocks as shown in Fig. 2:

1. A solar cell which supplies power to the μDSS system.
2. An radio frequency (RF) communication unit which communicates between the μDSS and the processors on the satellite.
3. An active pixel sensor (APS) imaging chip, referred to as APS+, which captures the image of the sun spot and outputs the centroid coordinates.

The μDSS system was developed by Delft University of Technology (TU Delft) in cooperation with TNO (Nederlandse Organisatie voor Toegepast Natuurwetenschappelijk Onderzoek or Netherlands Organization for Applied Scientific Research), which is a not-for-profit organization in the Netherlands that focuses on applied science.) (Delft, the Netherlands). TU Delft designed the sensor chip APS+ and TNO designed the sensor system

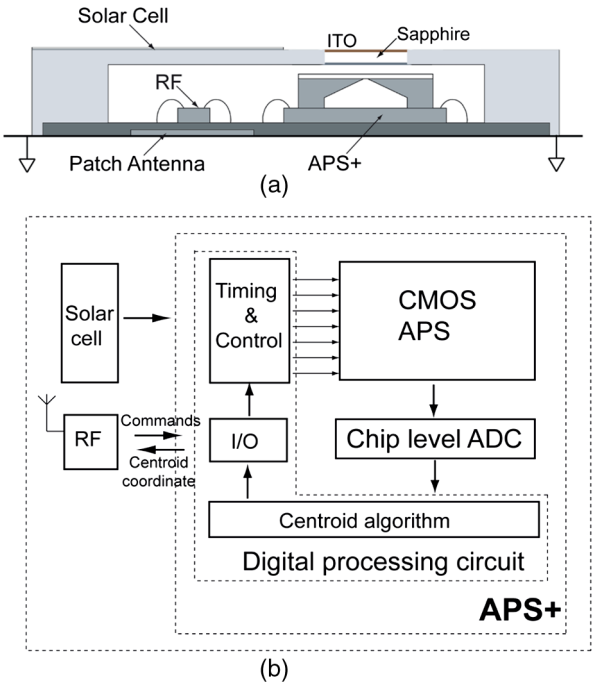

Fig. 2 (a) Cross-section of the μDSS system and (b) block diagram.

architecture. Thus, this article will focus on the design of the APS+.

The APS+, which is the imaging component in the defined system, is comprised of three blocks, as shown in Fig. 2:

1. An APS.
2. A chip-level ADC.
3. A digital processing circuit that contains the centroid algorithm circuit, the I/O interface circuit, and the timing and control circuit. The centroid algorithm determines the centroid coordinates of the sun spot on the focal plane based on the APS outputs. The timing and control unit generates the timing and control signals for the APS.

The planar dimensions of the μDSS are dictated by the size of the solar cell, which has to be large enough to provide enough power to the complete system. Thus to reduce the size of the μDSS, the power consumption of the system has to be reduced. This requires an optimal APS+ in terms of power, which is a big design challenge. Besides low power consumption, high resolution is also required. The resolution in the APS+ is enhanced by a noise reduction method called quadruple sampling (QS).

This article is organized as follows: in Sec. 2, the low-power oriented acquisition-tracking operational modes of the APS+ are briefly introduced. In Secs. 3 and 4, the designs in the acquisition and tracking mode are discussed, respectively, in detail. The radiation hardness considerations are introduced in Sec. 5. The chip performance and conclusion are presented at the end.

2 Low-Power-Oriented Operational Modes

As shown in Fig. 1, in the μDSS system the size of the sun spot is approximately 10 × 10 pixels, whereas the size of the

image sensor pixel array is 368×368 pixels. Thus, only a "window" of the complete pixel array is required to detect the sun spot.

Based on windowing, some digital sun sensors adopt a two-step acquisition-tracking (coarse-fine) readout method for power reduction.[4,7] After the sensor is powered on, it first works in sun acquisition mode and then estimates the coarse sun image coordinate. A pixel window, or region of interest (ROI), is addressed around the estimated coordinate at the end of this mode. Afterwards the sensor works in sun-tracking mode. The final centroid coordinate of the sun image is determined based on the readout result in the previously determined ROI. By "windowing," the power consumption of the sensor can be reduced to several hundreds of milliwatts.[7] However, as a consequence, the power consumption in acquisition mode is usually more than 1.5 times higher than in the tracking mode. The reason is that during the acquisition mode, the ROI is defined by comparing the amplitude of each pixel with a predefined threshold level. Since the complete frame needs to be scanned, the bandwidth of the readout circuit and ADC must be much higher than the frame rate. The power consumption in acquisition mode could be reduced by decreasing the readout bandwidth.

The developed APS+ also adopts the two-step acquisition-tracking readout method, but its operating principle is further optimized for low power.

First, in the acquisition mode, the APS+ estimates the coarse coordinate of the sun spot image. Unlike the other existing digital sun sensors, the APS+ determines the ROI based on the image profiling, as illustrated in Fig. 3. The profiling is achieved by a fast, low-power "winner-take-all (WTA)" principle, which is enabled by a specific pixel design.[8–10] At the end of the acquisition mode, the profiling of both rows and columns is achieved by the WTA principle; the summit of the row/column profiling indicates the centroid on the row/column direction. Thus the ROI is decided accordingly. The APS+ estimates the coarse sun spot center within an equivalent readout time for two rows. This fast process achieves a significant power reduction. The pixel design and the WTA principle will be discussed in Sec. 3.

After the ROI is determined in the acquisition mode, the APS+ switches to tracking mode. During this mode,

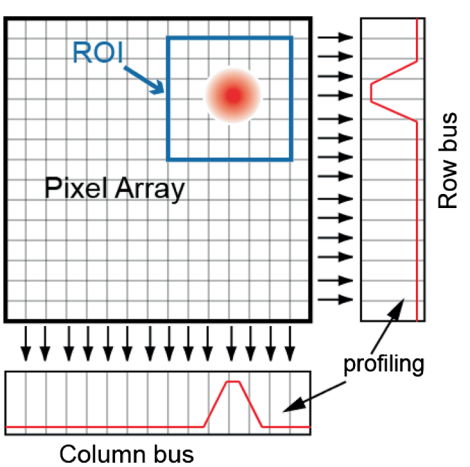

Fig. 3 Illustration of profiling by the "winner-take-all" (WTA).

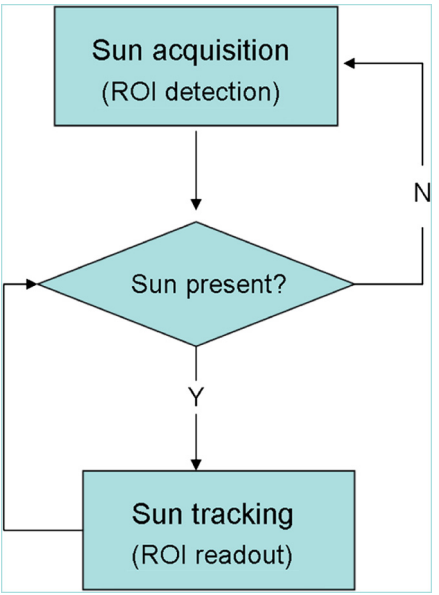

Fig. 4 Working flow of the APS+.

the APS+ reads out the ROI as in a conventional image sensor. The size of the ROI is defined as 25×25 pixels. At the end of the tracking mode, the final centroid is determined based on the readout results.

The complete working flow of the APS+ is illustrated in Fig. 4. First, in the sun acquisition mode, the ROI is determined if a sun spot is present in the image; afterwards, as long as the sun spot is present in the focal plane, the APS+ will continuously work in the tracking mode for fine coordinates. Once the sun spot moves out of the ROI, the APS+ is switched back to acquisition mode for a new ROI detection. The centroid decision process requires the readout load of two rows (sun acquisition) plus 25×25 pixels (sun tracking). Compared to the size of the complete pixel array, the APS+ dramatically reduces the readout load. The readout strategy significantly contributes to lowering the power consumption.

3 Low-Power Design in the Acquisition Mode

3.1 *Introduction to the WTA Principle*

The goal in the sun acquisition mode is to determine an ROI. In some position-sensitive devices, the ROI is detected by an image projection technique.[11] In the APS+, the ROI is decided based on the image profiling, which is achieved by the WTA principle as illustrated in Fig. 3. The WTA is a computational principle which selects the largest input in magnitude from a set of inputs.[12] Many WTA circuits were implemented in current mode.[13,14] Since the pixel architecture of the APS+ is 3-Transistor (3-T) APS, the WTA needs to be in a voltage mode. A voltage WTA circuit is proposed in Ref. 15; however, this WTA circuit is implemented by complex structures: it requires three extra transistors in each pixel, a current source and a readout circuit on every x-axis, y-axis, and global line.

The intended application of the APS+ is in microsatellites, where power and space budgets are rigid, thus the WTA circuit has to be simple to achieve space and power efficiency. In the APS+, a voltage WTA circuit with a simple

pixel structure is proposed, with no additional readout circuit or current source required.

3.2 *WTA Process*

In the APS+, the WTA implies that at the end of the integration, every column or row bus holds the amplitude of the most highly illuminated pixel (the "winner") on the corresponding column or row. In this way, the sun spot profiling can be obtained, as illustrated in Fig. 3. The pixel design with the WTA principle implemented is shown in Fig. 5. The pixel is similar to a typical 3-T APS, but it has two major differences: first, the pixel is composed of only p-MOS transistors to execute the WTA principle; second, in each pixel, an extra column select (CS) transistor is added besides the conventional row select (RS) transistor in order to enable row profiling. During the column profiling process, the RS transistors are active, whereas during the row profiling the CS transistors are active.

Figure 5 shows an example of three pixels on a column. This figure illustrates the WTA working principle. During column profiling, the CS transistors are not active (indicated in gray in Fig. 5). The process is explained as follows (assuming the first photodiode is the most highly illuminated):

1. At first all the pixels are reset at the same time. The voltage on the column bus (V_C) is high.
2. At the end of the integration, the voltage at the first photodiode $V1$ will be the lowest among the three because it is the most highly illuminated.
3. All the RS transistors (1:3) are turned on simultaneously; hence, all the source followers (SFs) in the pixels are turned on. Since $V1$ is the lowest, the SF of the first pixel (SF1) will have the highest source-gate voltage, thus the largest current. At the beginning, all the SFs (1:3) are active, so the level of V_C drops due to the source follower current. V_C will be stabilized after the column current source (I_D) is completely sunk by SF1, whereas all the other SFs are completely turned off. In this case, V_C is independently decided by $V1$, which is the output of the brightest or the winner pixel. The column profiling is achieved by applying the WTA principle on each column in the pixel array.

The WTA process described above can be implemented concurrently on all columns. Thus, the readout for the column profiling requires only one equivalent row time. In comparison, with the conventional readout method, the column profiling can only be available after the complete frame is read out, which requires 368 row times. Thus, the APS+ significantly reduces the power consumption by reducing the readout bandwidth.

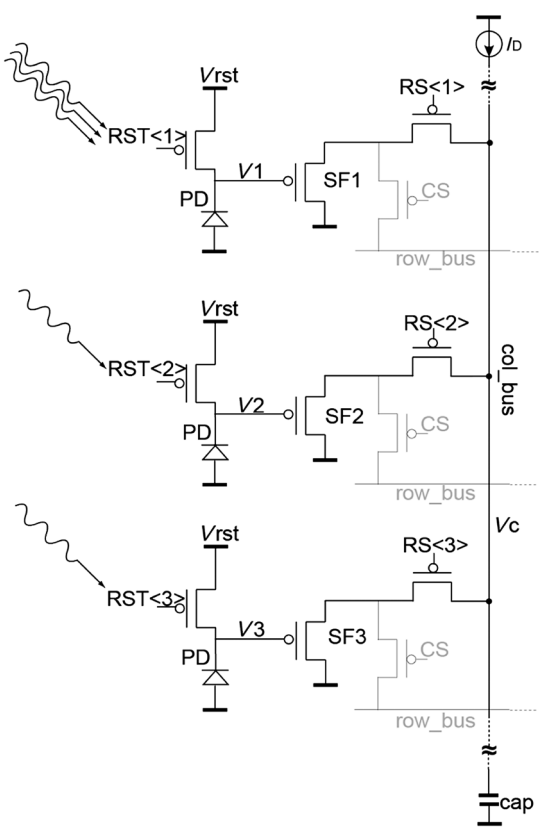

Fig. 5 WTA implemented by the specific pixel structure.

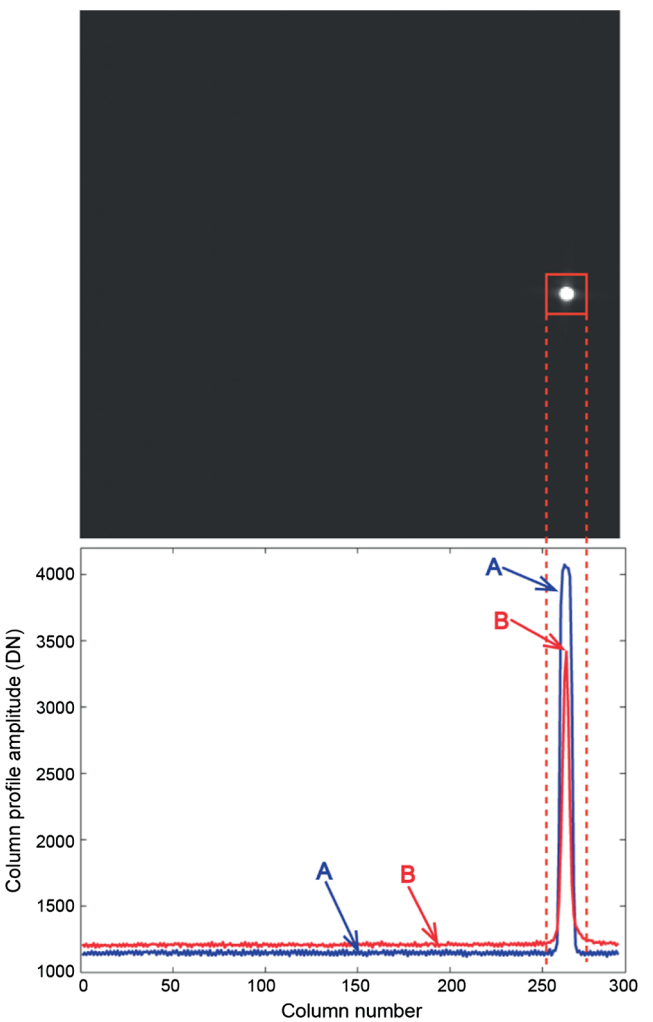

Fig. 6 Column profiling achieved by the WTA principle (indicated as A) and by direct readout result of the brightest row (indicated as B).

In Fig. 6, the image of the sun spot and the column profiling achieved by both the WTA principle (indicated as A) and a direct readout method (indicated as B) are shown. It shows that the profiling results using the two methods are able to indicate the coarse location of the sun image, but with different slopes. The difference in slope is due to the resolution of the WTA, which will be discussed in the next section.

3.3 *Resolution of the WTA*

3.3.1 *Qualitative analysis*

In the ideal case, the column current source I_D is exclusively sunk by the winner SF while all the other SFs are completely turned off. However, in practice when several photodiodes are illuminated by similar intensities, more than one SF is active and the I_D is shared among them. The winner SFs current is lower than the ideal, thus leads to a lower source–gate voltage. In this case, V_C is stabilized at a lower level than in the case of a single winner. V_C is exclusively decided by the winner only when the voltage difference between the winner and "second winner" is higher than a minimum value. This minimum voltage value is defined as the resolution of a WTA circuit.

The area illuminated by the sunlight is approximately 10×10 pixels. Thus, the columns and rows in this region may have more than one pixel with very similar outputs, with a difference in voltage smaller than the resolution value. A certain number of active pixels with the same photodiode voltage level on the same column could be a simple example. Figure 7 shows that the V_C level decreases when the number of active pixels increases. The pixels have the same photodiode voltage of 1.3 V in this case. The higher the number of active pixels, the lower the current is through each in-pixel SF, thus resulting in a lower V_C level.

When a couple of pixels are active, the current on the column bus is sunk by several SFs operating in saturation mode, thus lowering the SFs current and the level of V_C. This V_C level is lower compared to when only one winner pixel sinks the current. In other words, the V_C level is not only decided by the brightest pixel but also by the number of active pixels.

The readout circuit reads out the difference between a reference voltage level and the V_C. A lower V_C value indicates a higher output amplitude. Since the number of bright pixels increases in the center region of the spot, the profiling output amplitude also increases accordingly. This explains the results in Fig. 6 in the bright section of the profiling,

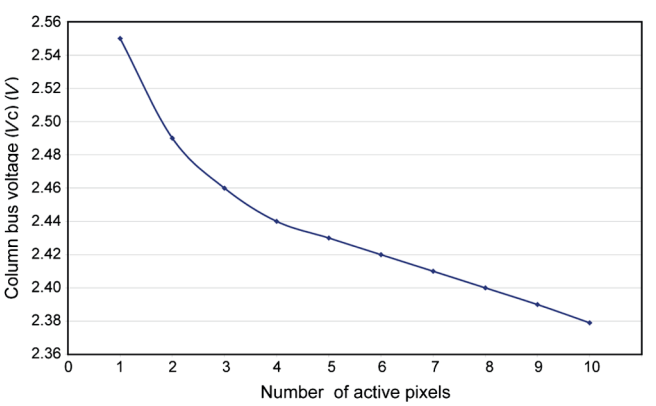

Fig. 7 Column bus voltage as a function of the number of active pixels.

where the WTA outputs a steeper slope than the direct readout result. Curve A is the profiling by the WTA, and Curve B is the readout output of the row which is located in the center of the sun spot. The WTA profiling successfully indicates the approximate location of the sun spot centroid.

In the dark region of the image, only dark pixels are presented on a column or row, in other words, there is no winner in this case. Thus, the column current is sunk by all the in-pixel SFs, and the current in each SF is very low so that all the SFs are pushed into the subthreshold region.

3.3.2 *Quantitative analysis*

In an ideal case as in Fig. 5, the first photodiode is so heavily illuminated that only SF1 is active and completely sinks I_D. The value of I_D is the maximum current that flows through SF1 in the saturation region. I_D is given by

$$I_D = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_C - V1 - |V_{TH}|)^2, \tag{2}$$

where μ is the mobility coefficient of the holes for the p-MOS transistor, C_{OX} is the gate oxide capacitance per unit area, W and L are the width and length of the SF, respectively, and $|V_{TH}|$ is the absolute value of the threshold voltage. For simplicity, only a first-order approximation is considered in Eq. (2), and the body effect is neglected. The value of V_C can be derived using Eq. (2):

$$V_C = V1 + |V_{TH}| + \sqrt{\frac{2I_D}{\mu C_{OX}\frac{W}{L}}}. \tag{3}$$

Since only SF1 is active, SF2 (as well as SF3) should be turned off, thus we reach another relationship:

$$V_C - V2 < |V_{TH}|. \tag{4}$$

Combining Eqs. (3) and (4), we can obtain the relationship between $V1$ and $V2$:

$$V2 - V1 > \sqrt{\frac{2I_D}{\mu C_{OX}\frac{W}{L}}}. \tag{5}$$

Equation (5) shows the minimum required difference between $V2$ and $V1$, so that only SF1 is active. In fact, this value is a parameter called V_{dsat}, which indicates how much the gate-source voltage has to exceed the threshold voltage in order to produce a certain current level in the saturation mode. For a WTA circuit, as shown in Fig. 5, this value is the minimum voltage difference required for the winner to "beat" all the other competitors and exclusively sink the current on the respective column bus. Thus, this value is defined as the resolution of this WTA circuit. If several competitors have similar outputs and the voltage difference is smaller than the resolution value, then there is no winner anymore. Moreover, the column current is shared among several SFs.

The calculations above are based on the assumption that the SFs work in the saturation mode. However, considering a column with only nonilluminated pixels, the column current source is uniformly divided among all SFs because there is no winner. The current flowing through each SF is very low

so that every SF operates in the subthreshold region. Thus the source-gate voltage is very low.

In the APS+, the total column current source of 6 μA is shared by 368 in-pixel SFs, resulting in ~16 nA of current in each SF if they are all turned on. The relation between the column bus voltage (V_C as shown in Fig. 5) and the current flowing through the active in-pixel SFs (I_{SF}) is shown in Fig. 8. The three curves illustrate different photodiode voltages: 1.8 V (reset level), 1.75 V, and 1.7 V. The graph clearly shows that when the current is lower than 1 μA, the SFs are in the subthreshold region. On the contrary, the SF works in the saturation region when the current is increased.

The readout circuit samples the column bus voltage (V_C) twice: when the photodiode is reset and after integration. The readout output V_{sig} is the difference between the two samples of the V_C. For the dark part of an image, the in-pixel SFs work in the subthreshold region with the WTA principle, while they work in the saturation region with a conventional readout method. Figure 8 shows that when an SF works in different operation regions, the V_{sig} has different values. For example, when the photodiode's reset level and video level are 1.8 and 1.75 V, respectively, V_{sig1} is the value when the SF is in the saturation region, and V_{sig2} is the value in subthreshold region. V_{sig2} decides the dark level of the profiling result.

3.3.3 *WTA resolution improvement*

The WTA resolution, shown by Eq. (5), is $\sqrt{2I_D/[\mu C_{OX}(W/L)]}$. The resolution is proportional to the square root of I_D. If the pixel design is not changed, a better resolution can be achieved by lowering the column current I_D. However, the settling time of the sample/hold array in the readout circuit will be increased by a lower current. A compromise has to be made between the WTA resolution and the settling time.

In the APS+, the column-level sample/hold capacitors are 2 pF, and the settling time with a 6 μA current source is 1 μs. The WTA resolution is about 250 mV with the same current source.

3.4 *Design Consideration for Row Profiling*

The above analysis explains the column profiling. However, row profiling cannot be implemented directly with the pixel design in Fig. 5. During row profiling, the CS switches in the pixels of a specific row and are activated simultaneously to implement the WTA. However, as there is no current source on the row bus, the WTA cannot work. In addition, if row profiling needs to be read out directly from row buses, an extra row readout circuit is necessary in addition to the conventional column readout circuit.

These two problems can be solved by modifying the pixel structure: an additional connection between the column bus and the row bus in the pixels is made on the diagonal of the pixel array. This is shown in Fig. 9. With these extra connections, every row bus in the pixel array is shorted to a corresponding column bus. During row profiling, a row bus uses the current source of a column bus, and the WTA results are available on the corresponding column bus; thus, the column readout circuit can be used to read the row profile information as well.

3.5 *Timing Diagram in the Acquisition Mode and the Profiling Measurement Results*

The timing diagram of the acquisition mode is shown in Fig. 10. When "all row reset," "column profile," or "row profile" is active, all the rows in the pixel array are selected. During the column profile pulse, the RS transistors of all the pixels are active and pixels on the same column are shorted; during the row profile pulse, the CS transistors are active and the pixels on the same row are shorted.

At the end of the integration time, each column bus holds the information of the most highly illuminated pixel (the winner) on each particular column, which allows the column profiling. After the column profiling, the same process is implemented on the row direction. The complete profiling measurement results are presented in Fig. 11. At the end of the acquisition mode, an algorithm circuit defines the ROI from the profiling by means of a threshold method and outputs the coarse centroid coordinates. The ROI is a subpixel array of 25×25 pixels. The APS+ is then automatically switched into tracking mode. The tracking mode is discussed in the next section.

4 Low Noise Approach in the Sun Tracking Mode

In the sun tracking mode, the APS+ reads out the pixels in the ROI to calculate the final centroid coordinates, as shown in Fig. 11. At the end of the tracking mode, the APS+ outputs

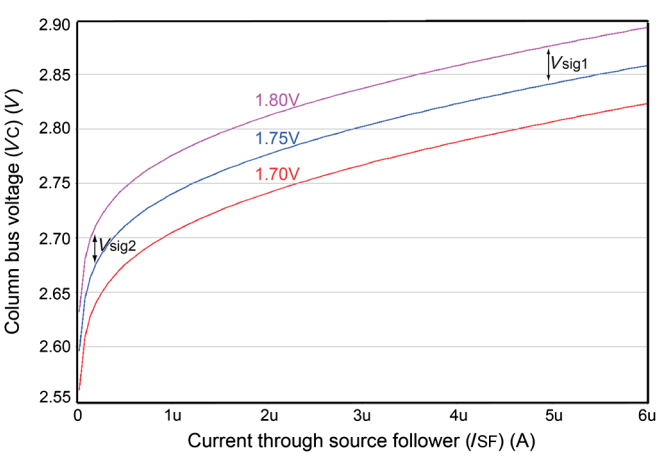

Fig. 8 Column bus voltage (V_C) as a function of the in-pixel SF current (I_{SF}) at different photodiode voltages.

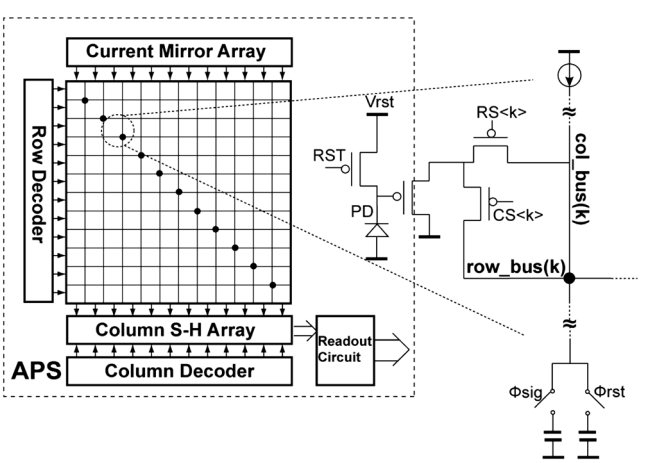

Fig. 9 System structure and pixel design of APS+.

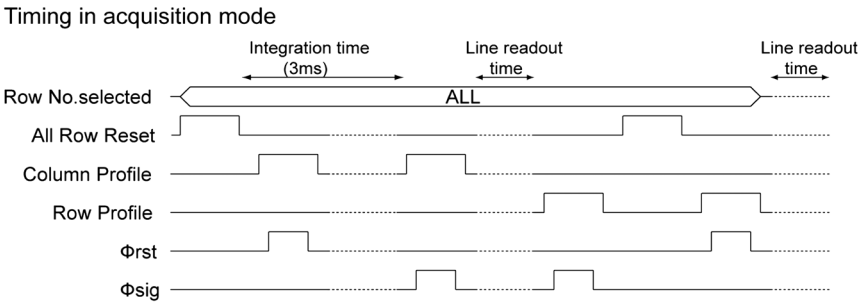

Fig. 10 Timing diagram in the acquisition mode.

the accurate centroid. The position resolution of the APS+ is a $1/64$-pixel pitch.

The subpixel position resolution requires a very low noise image sensor. The noise sources in an image sensor include: the ADC noise, the photon shot noise, reset noise (kT/C) and $1/f$ noise. The APS+ implements a QS method, which is a low noise readout approach to reduce the reset noise and $1/f$ noise.

4.1 *Conventional Readout Method*

The 3-T APS pixel structure is employed in the APS+ for the WTA implementation because at the beginning of this project, pMOS transistors were not available in a pinned photodiode process yet. The conventional readout method for a 3-T APS pixel is delta double sampling (DDS). The timing diagram of DDS is illustrated in Fig. 12(a).[16] In DDS, a pixel is sampled twice: at the end of the integration period (S1) and after the following reset (S2). The output of the DDS action is the difference between the two samples

$$V_{\mathrm{DDS}} = \mathrm{S2} - \mathrm{S1}. \tag{6}$$

With DDS, the pixel fixed pattern noise is cancelled by subtraction, and $1/f$ is greatly reduced if the interval between the two samples is short enough. The major

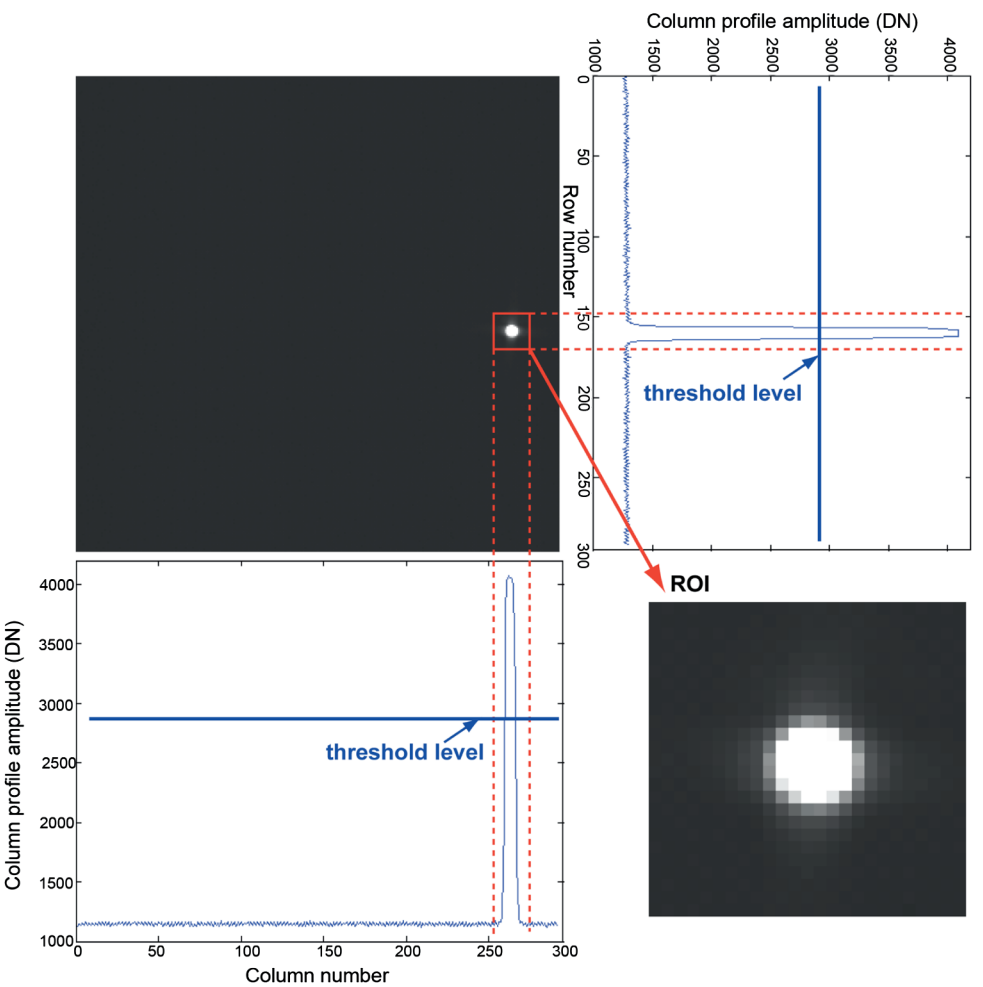

Fig. 11 Measurement results from the acquisition and tracking mode.

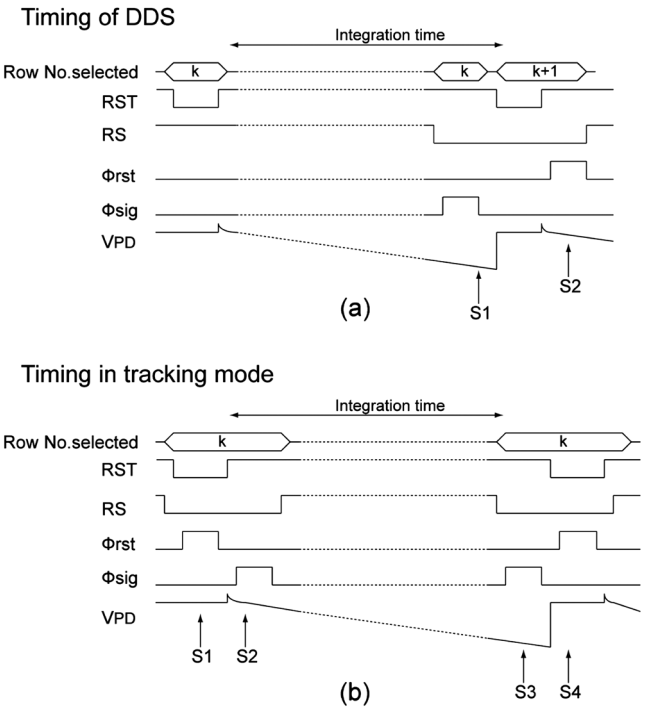

Fig. 12 (a) Timing diagram of delta double sampling (DDS) and (b) timing diagram of quadruple sampling (QS).

disadvantage of DDS is that it suffers from reset noise (kT/C noise).[17–19] In fact, the reset noise increases since the reset noise components in the two samples are not correlated. After the two samples are subtracted, the result is digitized by the ADC; thus, noise is introduced by ADC conversion as well as extra sources on the readout chain. The digital output of the subtraction result of Eq. (7) is

$$DV_{DDS} = V_{sig} + \sqrt{n_{rst,1}^2 + n_{rst,2}^2} + \sqrt{n_{amp,1}^2 + n_{amp,2}^2} + n_{ADC} + n_{ex} + (|V_{TH,2}| - |V_{TH,1}|), \quad (7)$$

where V_{sig} is the video signal; $n_{rst,1}$ and $n_{rst,2}$ are the reset noise components at the two samplings, which are uncorrelated; $n_{amp,1}$ and $n_{amp,2}$ are the thermal noise components of the DDS amplifier during S1 and S2, respectively; n_{ADC} is the noise due to ADC conversion; n_{ex} is the total thermal noise introduced by other extra noise sources, and $|V_{TH,1}|$ and $|V_{TH,2}|$ are the absolute values of the p-MOS SF threshold voltages during S1 and S2, respectively; they are different due to the body effect.

Equation (8) shows that the main sources of noise are reset noise, thermal noise of the amplifier, extra noise sources, and the ADC quantization. The threshold variation also has an effect on the final result, as indicated by Eq. (8).

4.2 *QS Method*

A correlated triple sampling method was proposed in Ref. 20. It has the same sampling principle as the QS implemented in the APS+. Correlated triple sampling was initially addressed for $1/f$ noise cancellation in long integration time applications. QS mainly focuses on both $1/f$ noise and reset noise reduction. The QS method reduces the reset noise, whereas the readout noise is increased due to multiple samplings and subtractions. Thus, it improves the noise performance when reset noise is the dominant noise source.

The timing diagram of the QS implemented in the APS+ is shown in Fig. 12(b) for the pixel schematic of Fig. 9. In QS, four samples are taken in a readout cycle. Samples S1 and S4 are taken when RST is active; S2 and S3 are taken at the beginning and at the end of the integration time, respectively. The reset noise components in S2 and S3 can be cancelled at the end by subtraction because they are correlated in this case.

4.3 *Qualitative Analysis*

A complete QS cycle involves three subtractions: twice in the analog domain and once in the digital domain (in the developed APS+). After the pixel is reset, S1 and S2 are taken and the subtraction of S1–S2 is processed in the analog domain; after the integration, S3 and S4 are taken and S4–S3 is again processed in the analog domain. As in DDS, the subtractions of S1–S2 and S4–S3 reduce the pixel fixed pattern noise and $1/f$ noise components. These subtraction results are digitally stored on-chip. Next, the digital outputs of the previous results are subtracted in order to cancel the reset noise. In the final result, the pixel fixed pattern noises, $1/f$ noise as well as reset noise, are all cancelled.

4.4 *Quantitative Analysis*

The subtractions of S1–S2 and S4–S3 are processed in the analog domain and are converted digitally by the ADC. If the noises introduced by the ADC conversion and other sources on the readout chain are taken into consideration, the digital results of the double subtractions will be

$$\text{Result1} = \text{S1} - \text{S2} = n_{rst,2} + \sqrt{n_{amp,1}^2 + n_{amp,2}^2} + (|V_{TH,1}| - |V_{TH,2}|) + n_{ADC,1} + n_{ex,1} \quad (8)$$

and

$$\text{Result2} = \text{S4} - \text{S3} = V_{sig} + n_{rst,3} + \sqrt{n_{amp,3}^2 + V_{amp,4}^2} + (|V_{TH,4}| - |V_{TH,3}|) + n_{ADC,2} + n_{ex,2}. \quad (9)$$

In the above expressions, V_{sig} is the video signal; $n_{rst,2}$ and $n_{rst,3}$ are the reset noise at the corresponding samples, which are correlated; $n_{amp,1}$ to $n_{amp,4}$ are the thermal noises of the QS amplifier during the four samples; $|V_{TH,1}|$ to $|V_{TH,4}|$ are the absolute values of the SF threshold voltages during the four samples; $n_{ADC,1}$ and $n_{ADC,2}$ are the total noise introduced by the ADC during the two conversions; and $n_{ex,1}$ and $n_{ex,2}$ are noises from all the other sources on the readout chain.

Two statements concerning these signals can be made:

1. $n_{rst,2}$ and $n_{rst,3}$ are reset noises in the same frame: $n_{rst,2} = n_{rst,3}$.
2. The photodiode voltage in sample 1 and sample 4 are the same, which leads to the same body effect in the two samplings, thus $|V_{TH,1}| = |V_{TH,4}|$.

Considering the facts above, the final result of the digital subtraction of Result 2−Result 1 will be:

$$DV_{QS} = V_{sig} + \sqrt{n_{amp,1}^2+n_{amp,2}^2+n_{amp,3}^2+n_{amp,4}^2} + (|V_{TH,2}| - |V_{TH,3}|) + \sqrt{n_{ADC,1}^2+n_{ADC,2}^2} + \sqrt{n_{ex,1}^2+n_{ex,2}^2}. \quad (10)$$

The result of QS in Eq. (10) is compared with that of the DDS in Eq. (8), which leads to the removal of the reset noise component, while the effect from the threshold variation remains the same; however, the other thermal noise components are increased due to the multiple samplings and subtractions. Thus, the noise improvement by QS depends on whether the reset noise or readout noise is dominant.

4.5 *Measurement Results*

The photodiode capacity of the APS+ pixel is about 8 fF. Thus, the estimated value of the reset noise is 700 μV.[17] The thermal noise introduced by the QS amplifier is 67 μV; this number is extracted from simulations.[21] The on-chip ADC has an input-referred readout noise of 377 μV.[22]

In the measurements which are shown in Fig. 13, the APS+ dark random noise is measured by both QS and DDS. In this measurement, the threshold variation due to the body effect can be neglected because the reset and video signals are approximately equal in a dark measurement. In addition, the thermal noise n_{ex} can be derived from the measurements, which is ~250 μV. The measured total thermal noise is 1650 μV with the DDS method and 1250 μV with the QS method. These numbers are well matched with Eqs. (8) and (10). However, the relatively high noise from the ADC conversion and the external environment hampers the noise improvement with QS. The thermal noise measured with QS is 24% better than with DDS. The QS method is suitable for a system with low readout noise.

5 Chip Performance

The APS+ chip micrograph is presented in Fig. 14. During the centroiding accuracy measurement, the APS+ was measured at room temperature (25 deg). A 100-μm (diameter) pinhole was applied prior to the optical lens, resulting in a light spot on the pixel array. The light source was a laser pointer. A 90% attenuation filter was placed between the laser pointer and the pinhole in this measurement. This measurement result shows that the APS+ achieves a sun position accuracy of 0.01 deg (3σ). The working temperature range of the μDSS is between −40°C and +80°C. At 25°C, the power consumption of the APS+ is 21 mW. Of this 21 mW, the on-chip ADC consumes 13 mW, the digital processing circuit consumes ~3.6 mW, and the focal pixel array and analog chain consume <5 mW. Figure 15 shows the power consumption of the APS+ from room temperature (25 deg) up to 80 deg. The measurement results show that the power consumption is increased as a function of the temperature. At 80 deg, the power consumption is 23.2 mW, which is ~1.8 mW higher than the value at 25 deg. Over this temperature range, the power consumption of the ADC increases from 13 mW at 25 deg to 14.8 mW at 80 deg, the power of the digital processing circuit increases from 3.6 to 3.8 mW, and the power by the pixel array remains approximately the same. Thus, the increase in power consumption mainly stems from the ADC. Despite slight increases, the power consumption of the APS+ is roughly stable in its operation over this temperature range. Over this temperature range, the power consumption of the on-chip ADC increases from 13 mW at 25 deg to 14.8 mW at 80 deg, the power of the on-chip digital processing circuit increases from 3.6 to 3.8 mW. Despite slight increases, the power consumption of the APS is roughly stable in its operation temperature range.

A summary of the APS+ sensor characteristics and a comparison between the presented work and other recently reported sun sensors are listed in Table 2. The APS+ has achieved a better measured performance than the specifications in Table 1. Compared with other sun sensors, the μDSS

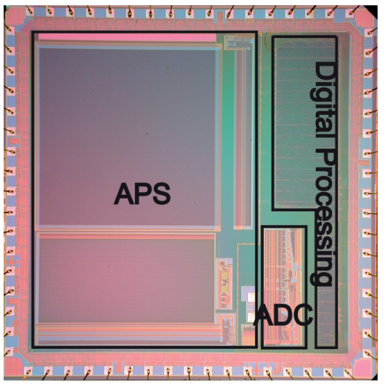

Fig. 14 Micrograph of APS+.

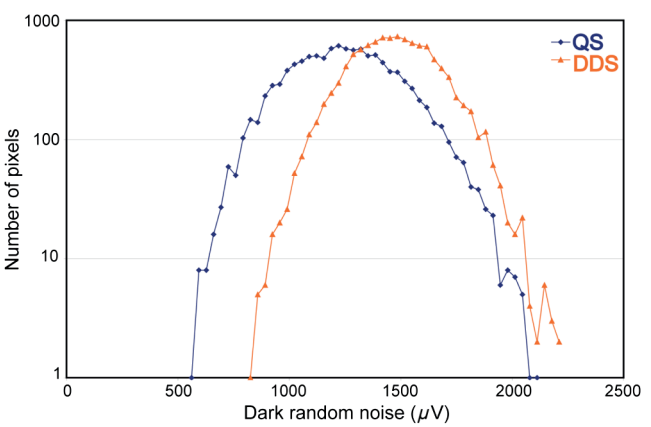

Fig. 13 Histogram of the dark random noise with QS and DDS.

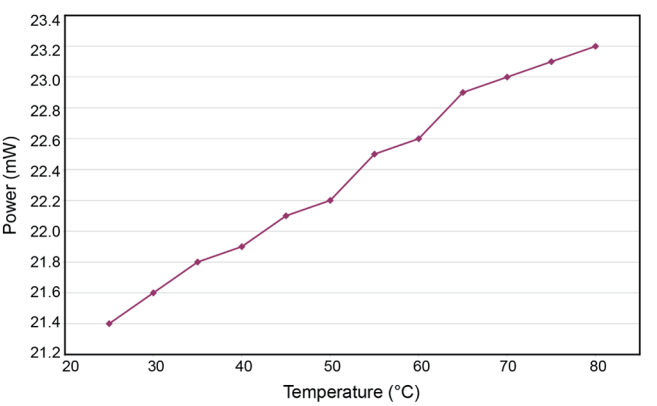

Fig. 15 Power consumption as a function of the temperature.

Table 2 Characteristics of the APS+ and comparison with the state of the art.

	Process technology	0.18 μm 1P4M		
APS+	Pixel pitch	$6.5 \times 6.5\ \mu m^2$		
	Fill factor	30%		
	Effective pixels	368×368		
	Conversion gain	$20\ \mu V/e^-$		
	Full well capacity	$50,000\ e^-$		
	Characteristics	**μDSS (this work)**	**Galileo (ESA) Ref. 7**	**SS-411 Ref. 23**
μDSS versus counterparts	Year	2010	2010	2009
	Chip size	$5 \times 5\ mm^2$	$11 \times 11\ mm^2$	Not available
	Pixel array	368×368	512×512	Not available
	Integration	SoC	SoC	Multichip
	Power consumption	21.34 mW at acquisition 21.39 mW at tracking	327 mW at acquisition 193 mW at tracking	75 mW
	Power supply	3.3 V for analog 1.8 V for digital	3.3 V for analog 1.8 V for digital	5 V
	FOV	±50 deg	±64 deg	±70 deg
	Operating temperature	−40 × deg to +80 deg	−40 deg to +70 deg	−25 deg to +70 deg
	Accuracy	0.01 deg (3σ)	0.024 deg (3σ)	0.11 deg (2σ)
	Resolution	0.004 deg	<0.005 deg	Not available
	Detection principle	Single pin hole	Single pin hole	Multiple apertures

is superior in power consumption, chip size, accuracy, and integration density.

6 Conclusion

In summary, the APS+ is a fully autonomous sun sensor chip. It consumes 21 mW of power at 10 fps, which is 10 times less than prior state of the art SoCs. This is realized by using a two-step acquisition-tracking operation mode and a fast and low power profiling method, which is implemented by means of the profiling method. The proposed pixel design not only facilitates the profiling by the WTA principle, but it also eliminates the need for an extra row readout circuit. Furthermore, in the tracking mode, the QS reduces the thermal noise by 24% compared to DDS. The APS+ high-performance image sensor and smart algorithm enable the μDSS to achieve a resolution of 0.01 deg in its FOV of ±50 deg.

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