# A Memristive Based Design of a Core Digital Circuit for Elliptic Curve Cryptography

Khalid Alammari<sup>1</sup>, Majid Ahmadi<sup>1</sup>, and Arash Ahmadi<sup>2</sup>

Department of Electrical and Computer Engineering, University of Windsor, Windsor, Canada
Department of Electronics Engineering, Carleton University, Ottawa, Canada

alammar@uwindsor.ca; ahmadi@uwindsor.ca; aahmadi@doe.carleton.ca;

Abstract— The new emerging non-volatile memory (NVM) devices known as memristors could be the promising candidate for future digital architecture, owing to their nanoscale size and its ability to integrate with the exciting CMOS technology. In this paper, a combination of memristor devices and CMOS transistors are working together to form a hybrid CMOS-memristor circuit for XAX- Module, a core element for the finite field multiplier. The proposed design was implemented using Pt /TaOx/Ta memristor device and simulated in Cadence Virtuoso. The simulation results demonstrate the design functionality. The proposed module appears to be efficient in terms of layout area, delay and power consumption since the design utilizes the hybrid CMOS/memristor gates.

**Keywords**: Memristor, Memristor Ratioed Logic, CMOS technology, Memristance, Logic gate Design, XAX- Module

### **1. INTRODUCTION**

Memristor devices have drowned much of attention since they were first introduced by Leon Chua [1]. The new emerging device [2] is two terminal resistive components with non-volatile memory capable of holding data at low area usage by varying its resistance under certain condition. This unique behavior makes this device very appealing, not only for memory design [3], but also to many other applications such as analog circuit design [4], signal processing [5], neural network [6] and logic design [7], alongside all other memristor-based applications. The memristor-based logic design is an ambitious step towards future VLSI technology. Hence, there has been intensive research covering the field of logical design involving memristor devices. Only-memristor based method is one of the memristor-based logic designs whereas the logical states ('0' and '1') are defined by the value of the resistance of the output Memristor known as Memristance 'M'. Memristance values can swing between two resistance states. High resistance state R<sub>OFF</sub> and low resistance state R<sub>ON</sub> based on the magnitude, direction, and duration of the applied voltage. Material Implication Logic (IMPLY) [8] and Memristor Aided Logic (MAGIC) [9] are well-known logic for this method. Memristor Ratioed Logic (MRL) [10] is another memristor-based logic design method. In this method, both memristor devices and CMOS transistors can be combined in an integrated platform due to the similarity in their logical state. Although, CMOS is a mature technology, the integrated structure of CMOS-Memristors will provide CMOS with an opportunity to address the challenges it faces with respect to any further scaling-down [11]. The MRL logical states ('0' and '1') are defined by the level of the output voltage. In this work, we present more efficient design for XAX- Module using the memristor device. The building block XAX- Module or a multiple copy of the module is involved in different multiplier architecture reported in [12-14]. The main improvement in this design is using the MRL- based gates instead of standard CMOS gates since current CMOS technology is reaching its limit in term of transistors size. The organization of this paper is as follows: Section 2 provides a brief introduction to the Pt/TaOx/Ta memristor device and their modeling along with explanation on the design of memristor Ratioed Logic (MRL) method. Section 3 includes information about the implementation of hybrid CMOS- Memristor XAX-Module. In Section 4, simulation results and discussion on MRL- based XAX-Module. Finally, remarks and conclusion are presented in Section 5.

#### 2. MEMRISTOR AND DESIGN METHOD

#### 2.1. Memristor Modelling

Resistive random-access memory (ReRAM) is intended to be used in a wide range of nonvolatile memory application. In this paper, the device Pt / TaOx / Ta has been employed in the proposed XAX- module to deliver the memristive behavior. Thus, the electronic resistance of the device is changing to represent the logical state of the device. High resistance state ROFF represents logic '0'. While low resistance state RON represents logic '1' The resistance switching mechanism results from the concentration of oxygen vacancy in the disc, which is sandwiched between the plug zone and top electrode Pt zone [15]. The oxygen vacancy in the disc zone is considered as the state variable of the device N Which is determined by [15]. While low resistance state RON represents logic '1' The resistance switching mechanism results from the concentration of oxygen vacancy in the disc, which is determined by [15]. While low resistance state RON represents logic '1' The resistance switching mechanism results from the concentration of oxygen vacancy in the disc, which is concentration of oxygen vacancy in the disc, which is concentration of oxygen vacancy in the disc, which is concentration of oxygen vacancy in the disc, which is sandwiched between the plug zone and top electrode Pt zone [15]. The oxygen vacancy in the disc zone is considered as the state variable of the device N Which is determined by [15].

$$\frac{dN}{dt} = -\frac{1}{[e. Z_{\text{vo.}} A. L_{\text{Disc}}]} \cdot I_{\text{ion}}(t)$$
(1)

where, A is the device cross-sectional area, e is the elementary charge,  $Z_{V0}$  is the charge number of the oxygen vacancies and  $I_{ion}$  is the ionic current which is responsible for the change of the state variable. The ReRAM device Verilog-A model used in the design is presented in [15]. The parameters found in table I. were applied to simulate the device in Cadence Virtuoso. The I-V curve shown in Fig. 1 represents the *Pt / Ta0x /Ta* device true memristive behavior. whilst Fig.2 [15] depicts the device equivalent circuit.

TABLE I. PT/TAOX/TA PARAMETERS FOR SIMULATION

*Pt/TaOx/Ta* Device

Parameter	<b>L<sub>Dis</sub></b>	<b>L<sub>таОх</sub></b>	<b>N<sub>min</sub></b>	<b>N<sub>max</sub></b>	<b>C</b> <sub>31</sub>	<b>A</b>
	(nm)	(nm)	(m⁻²)	(m <sup>-2</sup> )	(Am/V)	(nm²)
Value	04	11	05	05	6e-12	3.14e4

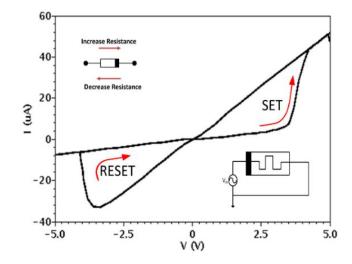


Fig.1. The I-V curve for the Pt/TaOx/Ta device. Current flows through the device from the bar side, the resistance of the device decreases  $R_{ON}$ . Current enters from the non-bar side the device resistance increases  $R_{OFF}$ .

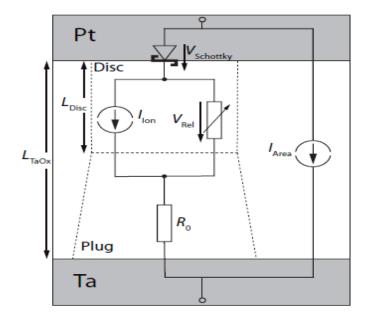


Fig.2.The equivalent circuit for Pt / TaOx / Ta device

#### 2.2. Memristor Design Method

Integrating memristor devices with conventional CMOS is a very promising tool for digital architecture implementation. In this work. The integrated platform is COMS compatible, unlike other logic designs such as IMPLY logic and MAGIC logic, which they attended to function in a pure memristive style based on the resistance of the output Memristor. The MRL logic offers the ability to perform all logic gates utilizing memristors and stack them in between CMOS upper layers [16]. While the requirement of more than one voltage level with read/ write circuit in IMPLY logic and the complication of joining more than two circuits in MAGIC logic put more restraints on their implementation. The MRL logic method was exploited to implement the proposed design. The logical state of this method is defined based on the level of the output voltage. Thus, low voltage and high voltage are representing logical states ('0' and '1') respectively. MRL-based AND gate and OR gate implementation requires only two memristors. V<sub>1</sub>, V<sub>2</sub> denotes the voltage applied to both memristors which change their

resistance state based on the voltage level.  $V_{OUT}$  denotes the output voltage of the logic circuit which is determined by the voltage divider across both memristive devices as follow: In MRL- AND gate when  $V_1$ = 0,  $V_2$ = 0.  $V_{OUT}$ , in this case, is therefore:

$$V_{OUT,AND} = \frac{R_{ON}}{R_{ON} + R_{OFF}} \times V_{CC} \cong 0$$
(2)

While in MRL- OR gate when  $V_1=1$ ,  $V_2=0$ . $V_{OUT}$ , in this case, is therefore:

$$V_{OUT,OR} = \frac{R_{OFF}}{R_{ON} + R_{OFF}} \times V_{CC} \cong 1$$
(3)

The schematics circuit for MRL-based basic gates AND, OR, NAND and NOR are displayed in Fig. 3. The MRL based NAND and NOR gates are similar to MRL-based AND and OR gates except each one of them needs a CMOS inverter to facilitate the circuits with the interface and control operation [17] which eliminates the effect of signal degradation associated with MRL-based AND and OR gates.

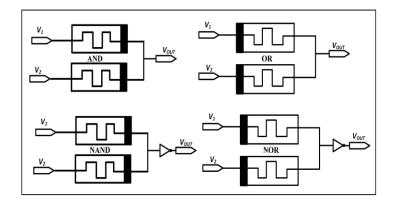


Fig.3.The schematic of MRL based basic gates

### 3. PROPOSED CIRCUIT

Applying varieties of MRL-based logic gates shown in Fig. 3 to current CMOS architecture is efficient way in terms of reducing the number of devices and increases logic density. In this paper a proposal for XAX- Module [12-14] has been presented

based on the MRL-based logic gates. The XAX- module shown in Fig.4 is consists of one AND gate, two XOR gates and three flip-flops. The MRL-based AND requires 2 memristor devices. The memristors are combined in series and offered the appropriate polarities. While MRL-based XOR gate requires 6 memristor devices and 2 MOSFETs

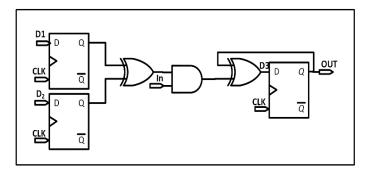


Fig.4. The XAX- module schematic

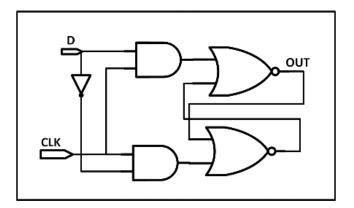


Fig.5. The gate level schematic of D latch

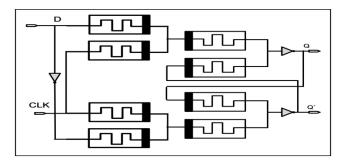


Fig.4. The MRL-based D-latch schematic

In addition, the D flip-flop DFF circuit used in the module comprises of two D- latch circuits serially interconnected. A clock signal CLK is connected directly to the first latch and to the second latch via inverter. This structure is known as master-slave. Fig .5. shows the gate level schematic of D latch. The MRL based- D-latch is implemented using two MRL based- AND gates and two MRL based- OR gates. The MRL based- D-latch shown in Fig.6. utilizes 8 memristor devices and 6 MOSFETs which makes the total number of devices involved in the MRL-based DFF are 16 memristor devices and 14 MOSFETs.

# 4. RESULTS AND COMPARISON

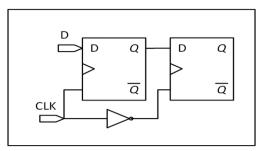


Fig.7. The structure of master-slave for DFF

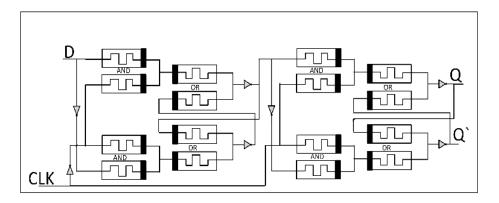


Fig.8. The MRL- based DFF schematic

The proposed XAX- module has been implemented based on the hybrid CMOS-Memristor method. The Cadence Spectre circuit-level simulation has been used to evaluate the proposed XAX-module. The parameters presented in table I. are considered for the Pt / TaOx / Ta device to provide the design with the memristive behavior. The design of MRL- based XAX-module is made up of simple blocks of the DFF circuit together with the XOR-AND-XOR function based on the schematic shown in Fig. 4. The MRL- based DFF is the main component in the module in terms of devices numbers. The MRL- based DFF has been realized based on the schematic diagram shown in Fig. 7.

The MRL- based DFF presented in Fig.8. utilizes 16 memristor devices and 14 MOSFETs. Because of this, the MRL- based DFF consumes less area as compared to different DFF designs reported in [14] and [18]. The XOR-AND-XOR function is another block that participates in the XAX-module. The XOR-AND-XOR function involves two MRL-based -XOR gates combined with one MRL-based AND gate. MRL- based AND gate requires only two memristor devices while MRL-based XOR gate requires 6 memristor devices and 2 MOSFETs. The MRL-based XOR gate used in this proposed is utilizing a smaller number of MOSFET devices compared to other XOR designs reported in [14] and [19]. Therefore, the total number of devices in the XOR-AND-XOR function is 12 memristor devices and 4 MOSFETs. Whereas the same CMOS-based design employs 24 MOSFET devices. In this work, it is proven that utilizing MRL- based gates in the blocks that made up the XAX structure implies a significant reduction in the number of transistors. The memristors can be fabricated on the upper layers of CMOS inverter as explained in [20,21]. This Combination has led to almost 15% in area saving compared to the same CMOS-based-XAX module presented in [12-13]. This is mainly because of the layout area estimate of the design was carried out based on the size of CMOS inverter occupied each cell. From the performance point of view, the design power consumption and delay were also examined and compared against other same The consumed power in the design was calculated by CMOS-based designs. connecting two zero-DC supplies, one to Vdd and the other to the ground. The current flowing in this branch represents the amount of energy consumed by the design due to the logic transition inside the design. The current is measured and integrated over every alteration time by Cadence Virtuoso calculator. Equation 4 is used to calculate the design dynamic power consumption.

$$P_{Dyn} = \alpha C f V_{dd}^2 \qquad (4)$$

Here,  $\alpha$  is the switching activity factor, C is the capacitance value, *f* is the design frequency and V<sub>dd</sub> is the source voltage. While the transition time at each cell in the design contributes to the whole design propagation delay. Therefore, the delay was calculated by measuring the time interval between the input slew and output slew. The slew is defined as the time when the signal rises from 30% to 70% and falls from 70% to 30% of its Vdd. Table II. presents a comparison between the proposed design and several different CMOS-based XAX-module.

# TABLE II. COMPARISON BETWEEN NUMBERS OF DIFFERENT CMOS BASED XAX-MODULE AND PROPOSED DESIGN

Design	XAX-module [12]	XAX-module [13]	MRL_ based XAX
CMOS	27	27	23
Memristor	-	-	62
Delay (Ps)	57	83	54
Power (µW)	49.45	41.00	40.32

The proposed design has shown that it performs much faster and consumed less power because of the fewer numbers of deployed transistors. The validation of the module has been confirmed by the simulation results in Fig.9.

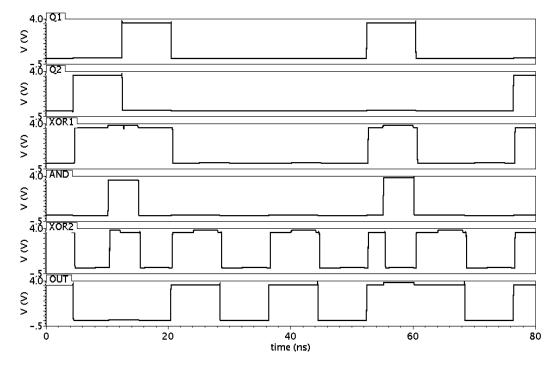


Fig.9. The behavior of the proposed CMOS-Memristor XAX module.

## 5. CONCLUSION

The XAX-module using logic-based design suffers from power and area overheads due to the number of involved MOSFET devise. One way used to reduce these effects is by considering MRL-based gate design. The MRL design indicates that it has the potential to attract modern CMOS design and could be a practical solution to ever-growing concern regarding CMOS transistor downsize. In this work, the building blocks of XAX-module has been implemented based on the hybrid CMOS-Memristor method. The memristor device of Pt / TaOx / Ta has been used to provide the design with the memristive behavior. The proposed MRL- based XAX-module employs fewer numbers of transistors. Thus, the design has a small layout area and consumes a considerable low power which makes this design is more efficient compared to other CMOS design. The design implemented and verified in Cadence Virtuoso at each stage to confirm its functionality.

# DATA AVAILABILITY

Data sharing not applicable to this article as no datasets were generated or analyzed during the current study.

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