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HOPF BIFURCATION AS AN INTERMEDIATE-SCALE INSTABILITY IN SINGLE-STAGE POWER-FACTOR-CORRECTION POWER SUPPLIES: ANALYSIS, SIMULATIONS AND EXPERIMENTAL VERIFICATION

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This paper reports intermediate-scale instability in a single-stage power-factor-correction (PFC) power supply that employs a cascade configuration of a boost stage operating in discontinuous conduction mode (DCM) and a forward stage operating in continuous conduction mode (CCM). The two stages combine into a single stage by sharing one main switch and one control loop to achieve input PFC and tight output regulation. The main results are given by "exact" cycle-by-cycle circuit simulations. The effect of the intermediate-scale instability on the attainable power factor is illustrated in terms of total harmonic distortion (THD) which is found by taking the Fast Fourier Transform (FFT) of the input current. The intermediate-scale instability usually manifests itself as local oscillations within a line cycle. Based on the stability analysis of a buck converter operating in CCM, the underlying mechanism of such instability can be attributed to the Hopf bifurcation that occurred in CCM forward stage. Finally, experimental results are presented for verification purposes.

Keywords: Power factor correction (PFC); single-stage PFC power supply; intermediate-scale instability; Hopf bifurcation.

1. Introduction

Nowadays, power factor correction (PFC) techniques have been widely used in switching power supplies to meet the increasingly stringent demand for very low line current harmonics [Dixon, 1990; Redl, 1994]. A typical configuration of power supply with PFC is the so-called two-stage PFC power supply which consists of a preregulator for PFC cascading with a dc/dc converter for output regulation. Here, "two-stage" means that both the preregulator and the dc/dc converter are separate systems. For low power applications (below 200 W), however, a "single-stage" configuration is more preferred than the "two-stage" one. A typical example is the single-stage isolated power-factor-correction power supply (SSIPP), which was first proposed by Redl *et al.* [1994]. This circuit consists of a PFC preregulator stage cascaded with an output stage for output voltage regulation. The preregulator stage is usually the boost converter, whereas the output stage

can be any dc/dc converter, e.g. flyback converter or forward converter. Moreover, the SSIPP shares one active switch and mandatorily operates the boost preregulator stage in discontinuous conduction mode (DCM) to achieve automatic PFC function. This means that the preregulator stage and the output stage do not work separately and must be taken as a whole system. Thanks to the special control strategy, the SSIPP has some obvious advantages (see [Redl *et al.*, 1994]) over the two-stage PFC power supply, especially for low-to-medium power applications. In the past decade [Chow *et al.*, 1998; Chow *et al.*, 2000; Siu *et al.*, 1997], much attention has been devoted to the steady-state design and control aspects of the SSIPP. However, the detailed dynamical behavior as well as its potential influence on the system's performance have seldom been investigated.

Recently, studies of nonlinear dynamics of switching power converter circuits have identified various kinds of bifurcation behaviors in a number of simple dc-dc converters under some typical control configurations (see [Banerjee & Verghese, 2000; Tse, 2003; Tse & Di Bernardo, 2002], and references therein). Such studies have also been extended to the PFC converters, which are actually ac-dc converters with a near unity input power factor. For the boost PFC preregulators operating in CCM, it has been found that both fast-scale and slow-scale instabilities can occur in some selected parameter regions [Dranga *et al.*, 2003; Iu *et al.*, 2003; Orabi & Ninomiya, 2003; Wong *et al.*, 2006]. For the SSIPP operating with DCM boost stage and DCM (or CCM) forward stage, it has also been reported that fast-scale instability may occur if the system parameters are chosen inappropriately [Wu *et al.*, 2006a; Wu *et al.*, 2006b]. It has also been shown previously that the slow-scale instability problem may worsen the harmonic distortion of the input current, whereas the fast-scale instability problem may impose higher current stresses on the switching devices. Thus, the study of instability in PFC converters will be useful for practical design considerations.

Slow-scale and fast-scale instabilities have been used to describe low-frequency oscillation and period-doubling bifurcation a voltage-mode buck converter operating in CCM, respectively [Mazumder *et al.*, 2001]. For dc/dc converters, there is only one type of time scale, i.e. the time scale with respect to switching frequency. In PFC converters, however, it is slightly different since there exist two types of time scale, i.e. the time scales of line frequency and switching frequency. Particularly, the line frequency is much lower than the switching frequency in practical applications. Thus, in PFC converters, fast-scale instability usually means period-doubling bifurcation of the time scale related to switching frequency [Dranga *et al.*, 2003; Iu *et al.*, 2003; Wu *et al.*, 2006a; Wu *et al.*, 2006b]. Intuitively, it is natural to regard period-doubling bifurcation with respect to input line frequency as slow-scale instability [Orabi & Ninomiya, 2003; Wong *et al.*, 2006]. In this paper, we report a totally different type of instability observed in the complete single-stage PFC power supply, in which the PFC boost preregulator and the forward output regulator are originally designed to operate in DCM and CCM, respectively. The instability reported in this paper usually manifests itself as a local oscillation within a line cycle. Hence, the observed instability seems to be "faster" than line-frequency instability, but "slower" than fast-scale instability. To avoid confusion from the instabilities observed in other time scales, we comply with the convention on time scale given in the previous studies, and name the instability observed here as *intermediate-scale instability*.

We will present our main findings as follows. First, through "exact" cycle-by-cycle simulations, we will show that power factor can be drastically degraded when intermediate-scale instability occurs. This is very important in practice because it will seriously affect the performance of the circuit. We will then investigate the underlying mechanism of the degradation of power factor along with the occurrence of intermediate-scale instability. We find that the intermediate-scale instability is essentially caused by Hopf bifurcation of the forward output regulator. From the analysis, we can derive the boundary of normal operation in any suitably chosen parameter space. Finally, we will show some experimental results to verify our findings from simulations.

2. System Description

The simplified schematic of the SSIPP under study is shown in its original form in Fig. 1 [Redl *et al.*, 1994]. The front-end boost converter serves as a PFC converter whose output is connected across the storage capacitor C_1, which in turn serves as the input to a standard forward converter. Moreover, the boost PFC converter and the forward converter

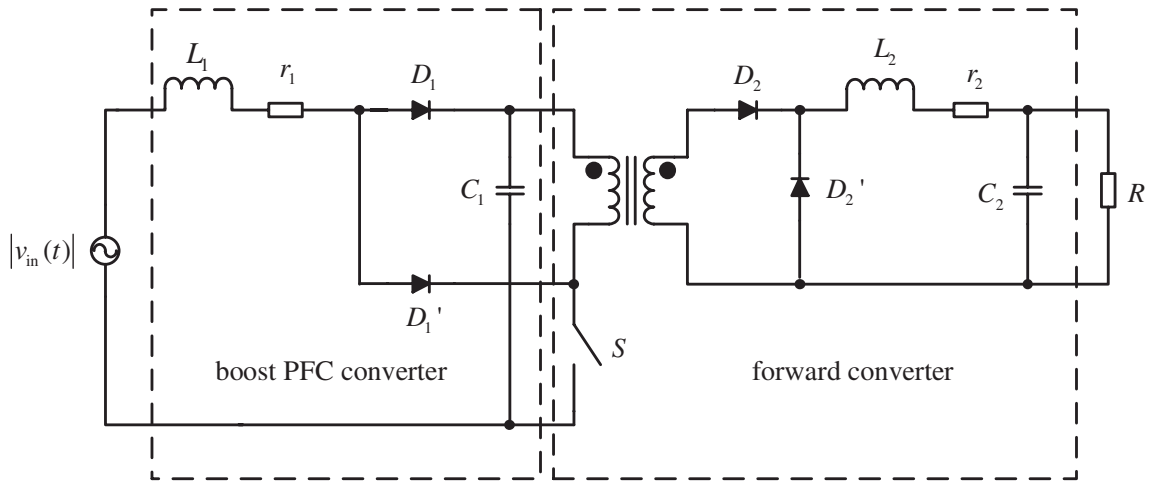


Fig. 1. Single-stage isolated PFC power supply (SSIPP). This circuit consists of a boost front-end PFC converter and a forward converter. Transformer isolation allows sharing of active switch by the two cascading stages. For the sake of simplicity, the core reset arrangement is not shown in this figure.

share the same active switch S, as shown in Fig. 1. Thus, this circuit can be modeled as a cascade connection of a boost converter and a buck converter, which are *driven synchronously* under one switching pulse-width-modulation (PWM) signal, as shown in Fig. 2. The control of the circuit takes on the voltage feedback control, in which a control voltage $v_{\rm con}$ is compared with a ramp signal to generate a PWM signal to drive the switch. The ramp signal is given by

$$V_{\rm ramp} = V_L + (V_U - V_L)\left(\frac{t}{T} \bmod 1\right) \qquad (1)$$

where V_L and V_U are the lower and upper thresholds of the ramp, and T is the switching period. The output of the comparator is "high" when $v_{\rm con} > V_{\rm ramp}$, and is "low" otherwise. Different from the proportional control used in [Wu *et al.*, 2006a] and [Wu *et al.*, 2006b], the control voltage $v_{\rm con}$ here is derived from a proportional-integral (PI) feedback control loop, which is more typical in industrial applications.

When the boost stage operates in DCM and the buck stage operates in CCM, three switch states are possible during a switching cycle:

State A: S_1 and S_2 are on, D_1 and D_2' are off;
State B: S_1 and S_2 are off, D_1 and D_2' are on;
State C: S_1 and S_2 are off, D_1 is off and D_2' is on.

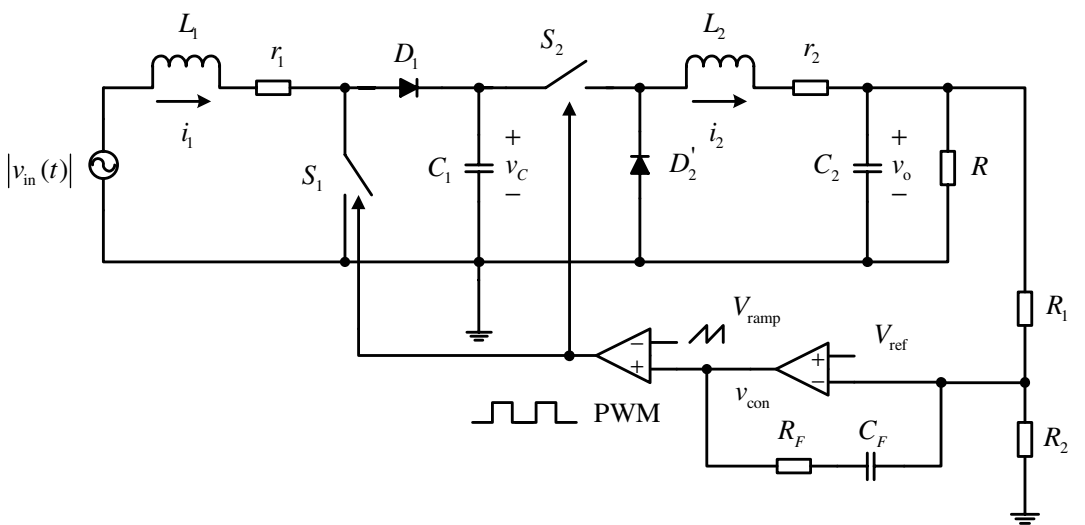


Fig. 2. Equivalent circuit model of the SSIPP under PI control.

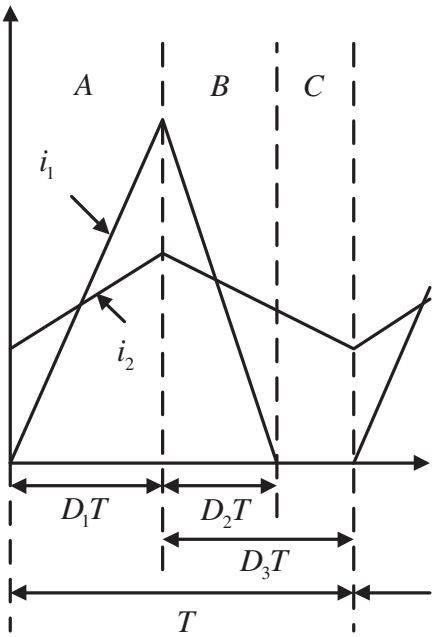


Fig. 3. Typical current waveforms of the SSIPP. The boost stage operates in DCM and the buck stage operates in CCM. The corresponding equivalent circuit presents a sequence of switch states as "ABC" in a switching cycle.

Typical current waveforms of the circuit operating with the above switching sequence are illustrated in Fig. 3.

Now, we can give the exact state equation corresponding to each switch state as follows:

$$\dot{x} = \begin{cases} A_1 x + B_1 & \text{for state A} \\ A_2 x + B_2 & \text{for state B} \\ A_3 x + B_3 & \text{for state C} \end{cases} \tag{2}$$

where x is the state vector defined as

$$x = [i_1 \quad v_C \quad i_2 \quad v_o \quad v_{\text{con}}]^T \tag{3}$$

and the system matrices As and Bs are given as

$$A_1 = \begin{bmatrix} -\frac{r_1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1}{L_2} & -\frac{r_2}{L_2} & -\frac{1}{L_2} & 0 \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{RC_2} & 0 \\ 0 & 0 & -\frac{K}{C_2} & \frac{K}{RC_2} - \frac{K}{\tau_F} & 0 \end{bmatrix} \tag{4}$$

$$A_2 = \begin{bmatrix} -\frac{r_1}{L_1} & -\frac{1}{L_1} & 0 & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{r_2}{L_2} & -\frac{1}{L_2} & 0 \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{RC_2} & 0 \\ 0 & 0 & -\frac{K}{C_2} & \frac{K}{RC_2} - \frac{K}{\tau_F} & 0 \end{bmatrix} \tag{5}$$

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{r_2}{L_2} & -\frac{1}{L_2} & 0 \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{RC_2} & 0 \\ 0 & 0 & -\frac{K}{C_2} & \frac{K}{RC_2} - \frac{K}{\tau_F} & 0 \end{bmatrix} \tag{6}$$

$$B_1 = B_2 = \begin{bmatrix} \frac{v_{\text{in}}}{L_1} \\ 0 \\ 0 \\ 0 \\ \frac{KV_{\text{ref}}}{\tau_F}\left(1 + \frac{R_1}{R_2}\right) \end{bmatrix} \tag{7}$$

$$B_3 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ \frac{KV_{\text{ref}}}{\tau_F}\left(1 + \frac{R_1}{R_2}\right) \end{bmatrix} \tag{8}$$

where v_{in} is the time-varying input voltage, $K = R_F/R_1$ is the DC gain of the PI controller, $\tau_F = R_F C_F$ is the time constant of the PI controller, and the other component symbols are as defined in the circuit diagram shown in Fig. 2.

3. Intermediate-Scale Instability from Circuit Simulations

In this section, we will present the observations of intermediate-scale instability of the SSIPP.

Table 1. Circuit parameters used in simulations.

Circuit Component	Values
Input Voltage v_{in}	110 V (V_{in}, rms), 50 Hz
Inductance L_1, ESR r_1	300 μH, 0.01 Ω
Inductance L_2, ESR r_2	3 mH, 0.01 Ω
Capacitance C_1	470 μF
Capacitance C_2	47 μF
Load Resistance R	15 Ω–90 Ω
Reference Voltage V_{ref}	1.5 V
R_1, R_2	19 kΩ, 1 kΩ
DC Gain of Controller K	0.04
Time Constant of Controller τ_F	1.5 T_0 ($T_0 = \sqrt{L_2 C_2}$)
Ramp signal	3 V–8 V, 20 kHZ

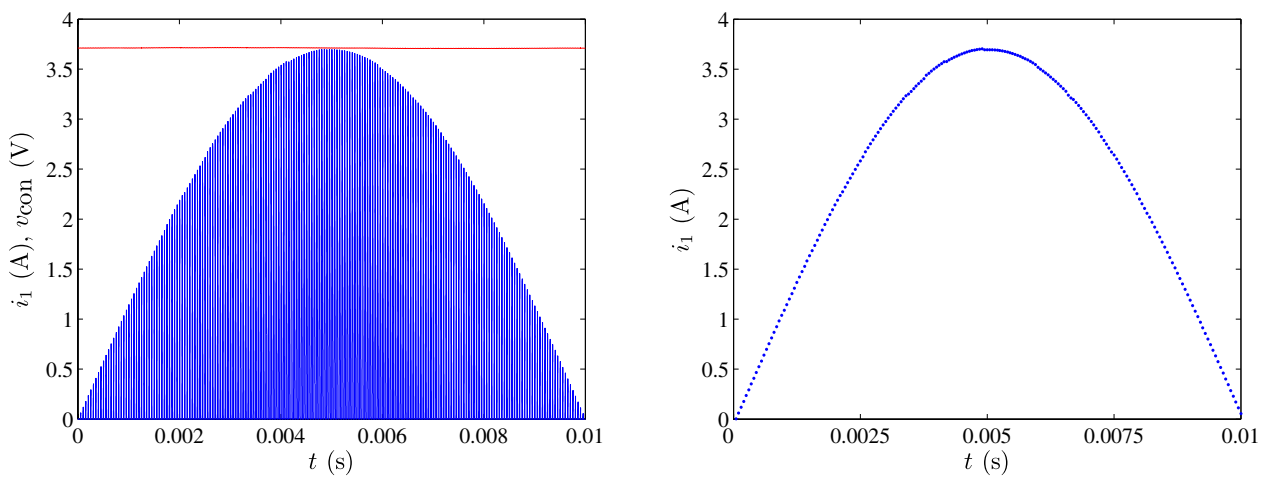
Our simulation is based on the exact piecewise switched model described in the foregoing section. Since practicing engineers are usually interested in the performance of SSIPP as the output power varies, we will accordingly observe the dynamical behaviors as the output power is changed. In our study, we will only change the load R and keep other circuit parameters fixed.[1] The circuit parameters used in our simulations are shown in Table 1.

3.1. *Stable operation*

When the output power is high, e.g. 60 W, the SSIPP can work in stable operation. Figure 4(a) shows the time-domain waveforms of i_1 and v_{con}. In order to see the change in dynamical behavior clearly, we collected the sampled peak values for i_1 and the corresponding values for v_C during each switching period in the steady state. Figure 4(b) shows the peak values of i_1 and Fig. 4(c) shows the phase portrait of the peak values of i_1 and v_C. Since the power factor is of practical importance in the SSIPP, we also calculate the total harmonic distortion (THD) using Fast Fourier Transform (FFT) [Brigham, 1988].[2] Figure 4(d) shows the FFT spectrum of i_1. The power factor is 0.9681, which is adequate for most practical applications.

3.2. *"Deep" intermediate-scale instability*

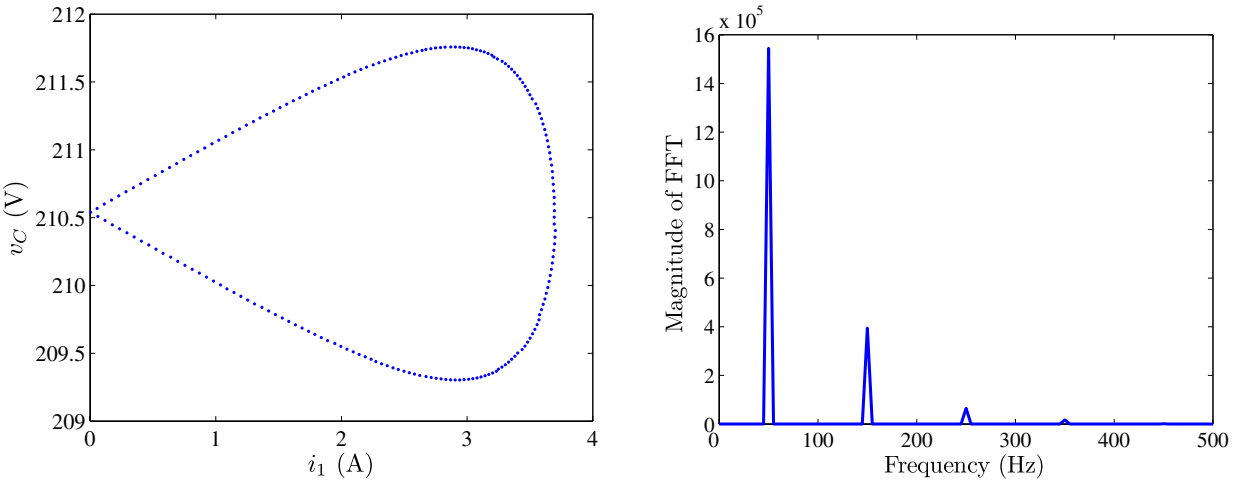
We now gradually increase the load resistance to obtain a lower output power. When the output power is adjusted below 48.1 W, we can clearly observe the occurrence of the intermediate-scale instability. Figures 5(a)–5(c) show the corresponding waveforms and phase portraits at 45 W, from which the local oscillations of i_1 and v_{con} with about 7 period within one half line cycle can be readily recognized. As a result, the power factor abruptly falls to 0.8633, which is much lower than that in the stable operation. Figure 5(d) shows the corresponding FFT spectrum of i_1, in which the fundamental



(a) (b)

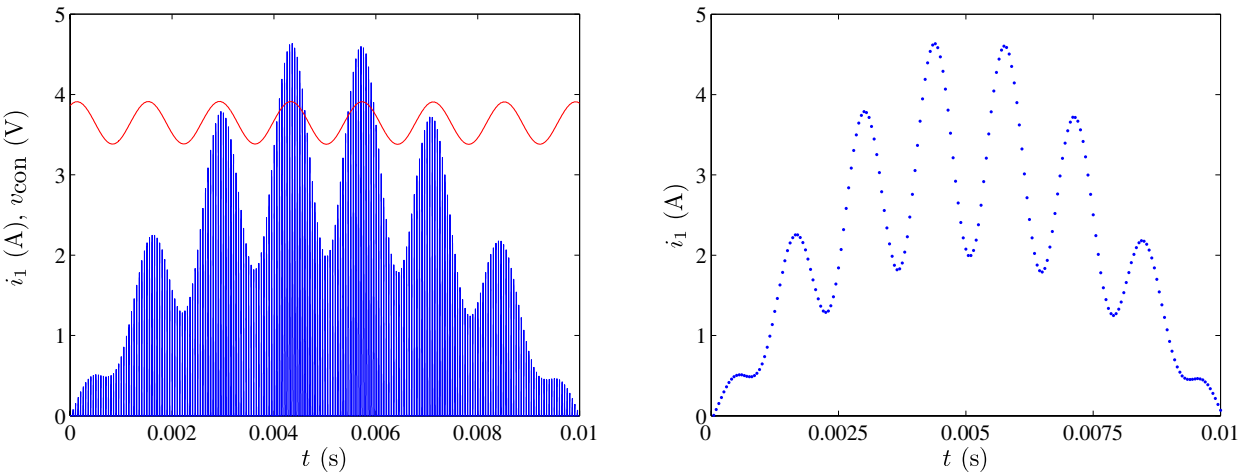
Fig. 4. Simulations at 60 W power. (a) Waveforms of i_1 and v_{con}; (b) peak values of i_1; (c) phase portrait of peak values of i_1 and v_C; (d) FFT of i_1.

[1]The output power equals V_o^2/R, where $V_o = V_{\text{ref}}(1 + R1/R2)$ is the expected regulated output voltage in the steady state.
[2]In the calculation of THD, we ignore those frequency components higher than 10 kHz as a filter is always present to remove the switching ripples of the input current.

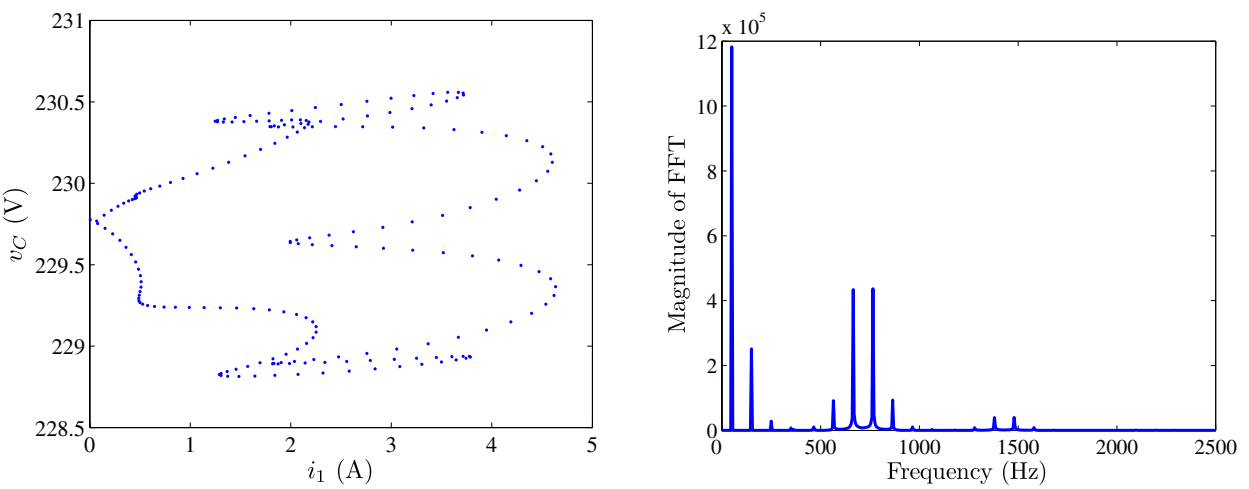


(c) (d)

Fig. 4. (*Continued*)



(a) (b)



(c) (d)

Fig. 5. Simulations at 45 W power. (a) Waveforms of i_1 and v_{con}; (b) peak values of i_1; (c) phase portrait of peak values of i_1 and v_C; (d) FFT of i_1.

component of the local oscillations (about 700 Hz) and its harmonics can be clearly observed.

3.3. *"Weak" intermediate-scale instability*

On further decreasing the output power, the intermediate-scale instability can still be observed, but with "weak" oscillations of i_1 and $v_{\rm con}$. Figures 6(a)–6(c) show the corresponding waveforms and phase portraits at 20 W. The explicit oscillations of i_1 and $v_{\rm con}$ indicate the existence of intermediate-scale instability. The power factor, however, can still maintain as high as 0.951. Figure 6(d) shows the FFT spectrum of i_1, which, compared with the "deep" case shown in Fig. 5(d), includes relatively "weak" fundamental component and its harmonics corresponding to the local oscillations caused by the intermediate-scale instability.

Remarks. "Weak" intermediate-scale instability may have little effect on power factor. But, it still deserves specific attentions for practical consideration because the oscillation of i_1 will change the original power distribution along the line cycle corresponding to the stable operation, resulting in larger current stresses on the switching devices.

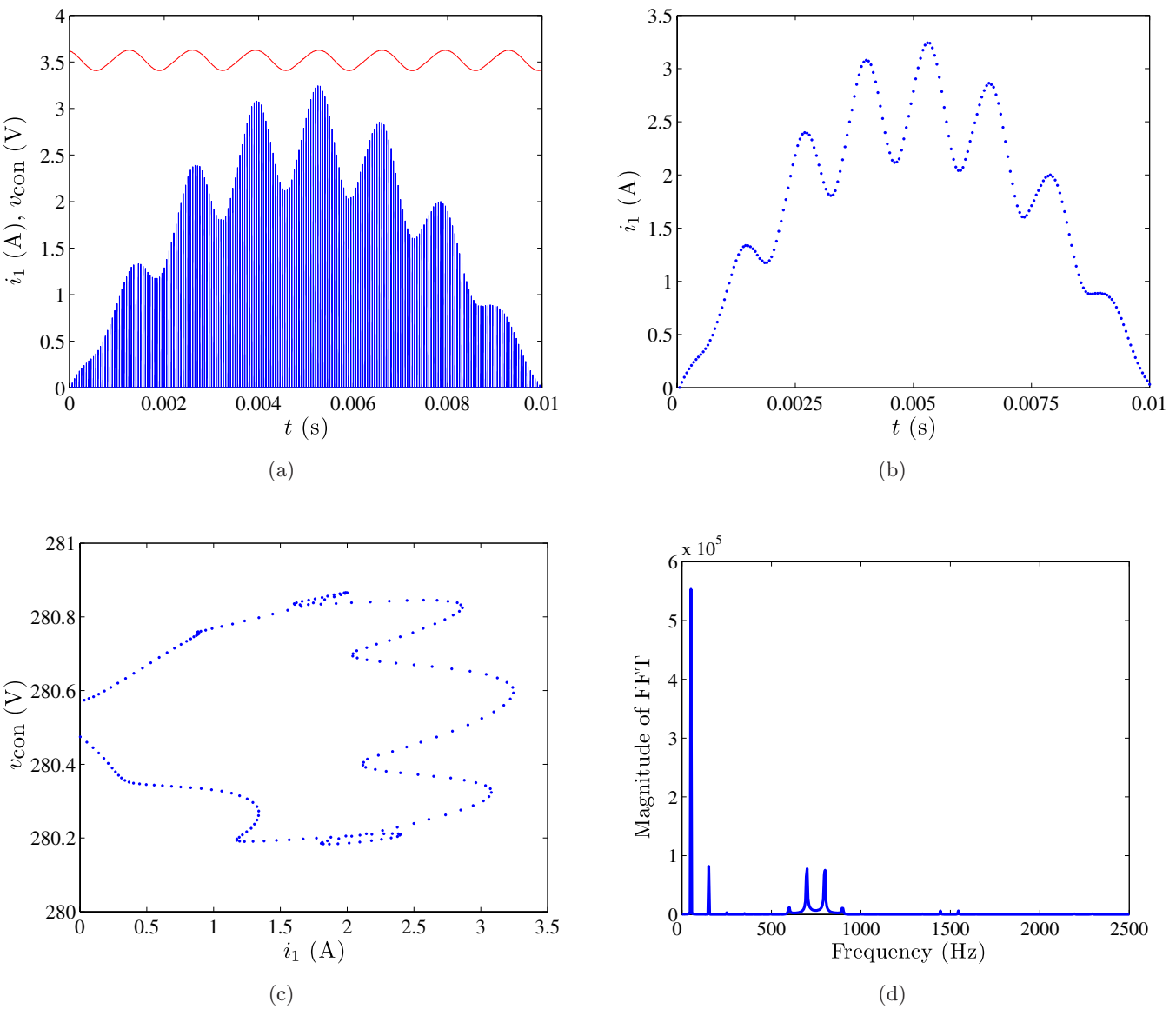


Fig. 6. Simulations at 20 W power. (a) Waveforms of i_1 and $v_{\rm con}$; (b) peak values of i_1; (c) phase portrait of peak values of i_1 and v_C; (d) FFT of i_1.

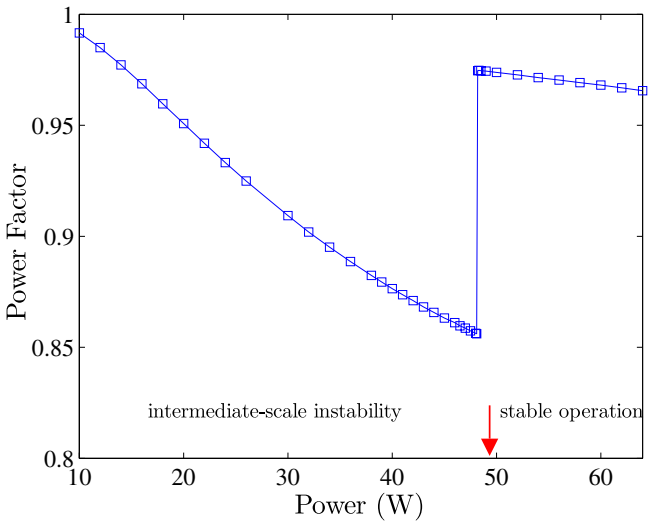


Fig. 7. Power factor of the SSIPP as the output power varies. The arrow indicates where intermediate-scale instability occurs.

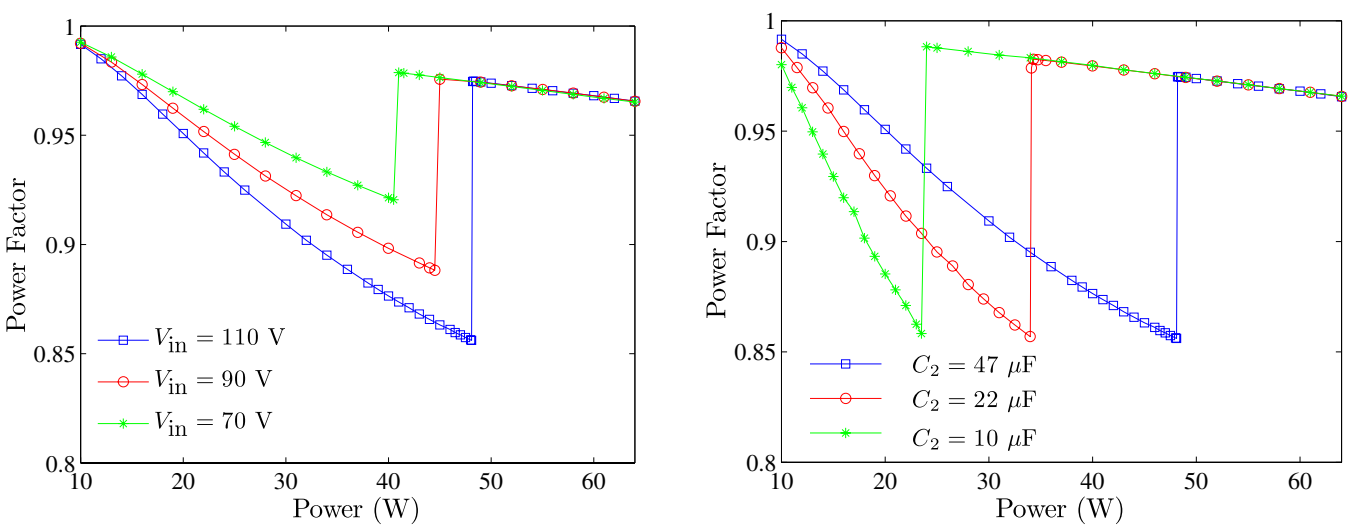
4. Effect of Intermediate-Scale Instability on Power Factor

In this section, we will look more closely at the effects of intermediate-scale instability on the power factor. Figure 7 shows the variation of the power factor as the output power decreases. It is readily observed that the SSIPP has a near unity power factor at high output power. When the output power is decreased below 48.1 W, the power factor is abruptly degraded to a low level, about 0.86 here. As indicated in Fig. 7, the intermediate-scale instability begins to occur at this output power level and below. In the region where intermediate-scale exists, the power factor then gradually rises as the output power further decreases. This phenomenon can be explained as follows. When the output power decreases, the local oscillation of the input current will be attenuated, as shown in Figs. 5(a) and 6(a). As a result, the frequency component of the local oscillation will also reduce, as indicated in Figs. 5(d) and 6(d). Thus, the power factor in the intermediate-scale instability region increases as the output power decreases.

Clearly, it may not be suitable to operate the system with the parameters used in the foregoing section because the critical output power when intermediate-scale instability occurs is relatively close to the nominal power, leaving rather small headroom for a stable operation. Thus, it is of practical importance to move the instability boundary further away from the nominal point by appropriately designing the parameters. Figure 8 shows the results for different V_{in} and C_2, from which we can see how these circuit parameters will affect the location of the instability boundary.

5. Hopf Bifurcation: The Cause of Intermediate-Scale Instability

As shown in Figs. 5 and 6, the intermediate-scale instability usually manifests itself as local oscillations within a line cycle. Moreover, we can see that it is the oscillation of v_{con} that gives rise to the



(a) (b)

Fig. 8. Power factor of the SSIPP as the output power varies (a) for different V_{in}; (b) for different C_2.

distortion in i_1. Thus, it is natural to pay specific attention to the underlying mechanism for the oscillation of $v_{\rm con}$. In this section, we will give some analytical results and study the relationship of the intermediate-scale instability with Hopf bifurcation.

In our study, the forward output regulator is designed to operate in CCM. From the equivalent circuit given in Fig. 2, the input of the forward output regulator is the output of the boost PFC preregulator, i.e. the voltage v_C across the storage capacitor C_1. Usually, v_C is only crudely regulated by the boost PFC preregulator, and thus can be considered as a DC voltage V_C superposed by a small ripple. If the capacitance of C_1 is sufficiently large, the ripple is negligible and v_C at steady state is approximately the DC voltage V_C. In [Redl *et al.*, 1994], it has been pointed out that V_C is dependent on the load variation for SSIPP operating with CCM regulating stage. An equation for V_C, which can be solved numerically, was given in [Redl *et al.*, 1994] for the case of DCM regulating stage. For the system considered in our study, a similar equation can be obtained and is given by (see Appendix A for detailed derivation)

$$\int_0^{T_{\rm L}/2} \frac{v_{\rm in}^2}{V_C - v_{\rm in}} dt = \frac{L_1 T_{\rm L} V_C}{RT} \tag{9}$$

where $T_{\rm L}$ is the line period.[3]

Moreover, as shown in Fig. 9, we can get an equivalent model of the regulating stage. For simplicity of analysis, we will neglect r_2, i.e. the ESR of L_2. Then, this model is essentially a voltage-mode controlled buck converter operating in CCM with input voltage V_C which can be obtained by numerically solving (9). Now, suppose that intermediate-instability takes place in the overall SSIPP system. In this case, the corresponding buck model must also lose its stability, and the control voltage $v_{\rm con}$ will exhibit the similar oscillating waveforms shown in Figs. 5(a) and 6(a).[4] Thus, we can conclude that the critical condition for intermediate-scale instability of the overall SSIPP system is equivalent to that for Hopf bifurcation for the equivalent buck converter model of the regulating stage model shown in Fig. 9. Obviously, this conclusion reduces our study model from the complicated "SSIPP" form to a more simple "buck" form, which

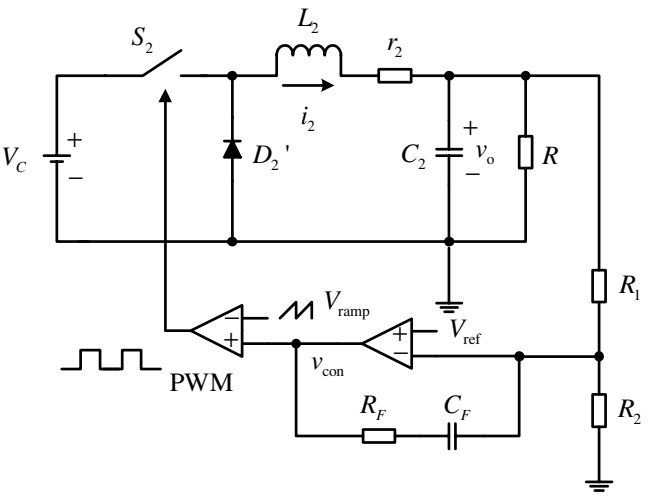


Fig. 9. Equivalent model of regulating stage.

greatly simplifies the analysis process. With respect to the study of bifurcation in the buck converter, previous work, however, has mainly focused on proportional feedback control, in which the typical period-doubling bifurcation can usually be observed [Di Bernardo *et al.*, 1998; Fossas & Oliver, 1996; Hamill *et al.*, 1992]. Little work has been done on the bifurcation type for the case of PI control considered here. To study the "low-frequency" Hopf bifurcation in the PI voltage-mode controlled buck converter, we can utilize the averaged model of the corresponding circuit. This method has been successfully used to analyze Hopf bifurcation in Ćuk converter and parallel-connected boost converters [Tse *et al.*, 2000; Iu & Tse, 2003]. With this method, the critical condition to judge Hopf bifurcation in the PI voltage-mode controlled buck converter operating in CCM can be derived and given by (see Appendix B for detailed derivation)

$$K_C = \frac{\tau_F (V_U - V_L)}{V_C(\tau - \tau_F)} \tag{10}$$

where $\tau = RC_2$. The buck converter will lose its stability via Hopf bifurcation when $K > K_C$.

Remarks. It should be noted that Appendix B does not give a formal condition for the occurrence of Hopf bifurcation. Actually, it provides information about when the equilibrium point of the

[3]The SSIPP in [Redl *et al.*, 1994] actually uses a flyback stage operating in DCM as the regulating stage, whereas a forward stage operating in CCM is used in our study here.

[4]Here, "the corresponding buck model" means that all parameters including V_C of the buck model are the same as those of the SSIPP system.

averaged equations loses its stability via a specific, but unknown, type of bifurcation. Hence, a further numerical check of the eigenvalues is required in order to confirm the occurrence of Hopf bifurcation. In our study, however, the analysis is based on the averaged model which will exclude any fast-scale bifurcation, e.g. period-doubling bifurcation. Therefore, we can assert that Hopf bifurcation occurs as the system loses stability, which will also be confirmed experimentally. On the other hand, it is worth pointing out that the critical condition is only valid when no other bifurcation has occurred prior to this predicted Hopf bifurcation.

By using (9) and (10), we can qualitatively explain the behavior observed in the foregoing section as follows. When the load R is relatively small, the K_C obtained from (10) is larger than K. Hopf bifurcation does not occur. As the load R increases, V_C will gradually increase from (9). At the same time, τ will also increase. Thus, from (10), the K_C will decrease as the load R increases. When the load R increases to the critical value, K_C will equal K. Then, Hopf bifurcation take places. Furthermore, we can also utilize (9) and (10) to obtain the operation boundary within which intermediate-scale instability does not occur. Figure 10 shows

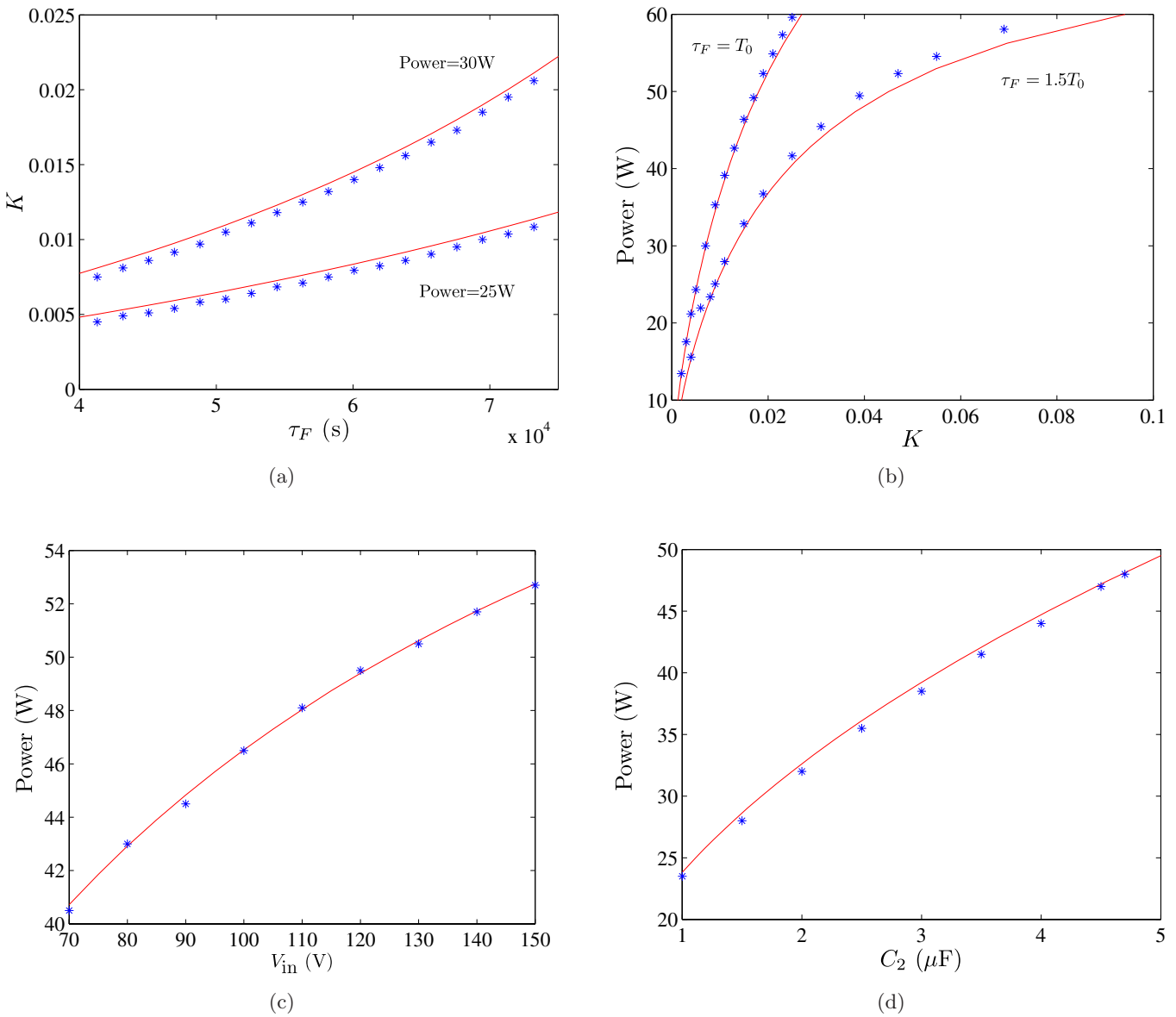


Fig. 10. Stability boundary in the parameter space of (a) K versus τ_F; (b) output power versus K; (c) output power versus V_{in}; (d) output power versus C_2. The stable region is located below the boundary curve for (a) and above the boundary curve for (b)–(d). The simulation results are indicated with $*$ and the analytical results are plotted with solid curves.

such a stability boundary in the parameter space of K versus τ_F, output power versus K, V_{in} and C_2, respectively. For the purpose of comparison, we also present the stability boundary from circuit simulations, which clearly verifies the validity of (9) and (10) in locating the normal operating region.

6. Experimental Verifications

To verify the observed intermediate-scale instability, an experimental circuit prototype of the SSIPP under study has been built. Figure 11 shows the full schematic diagram of the experimental circuit with detailed specifications indicated. It should be noted that our emphasis here is the qualitative behavior of the intermediate-scale instability. Thus, the absolute verification of the specific set of simulation results given in the foregoing section is not mandatory. As a result, the parameters used in the experiment are different from those in simulations. Nonetheless, the experimental results clearly verify the phenomena observed from simulations.

Figure 12 shows the measured waveforms for $R = 15.7\,\Omega$, where the system works in stable

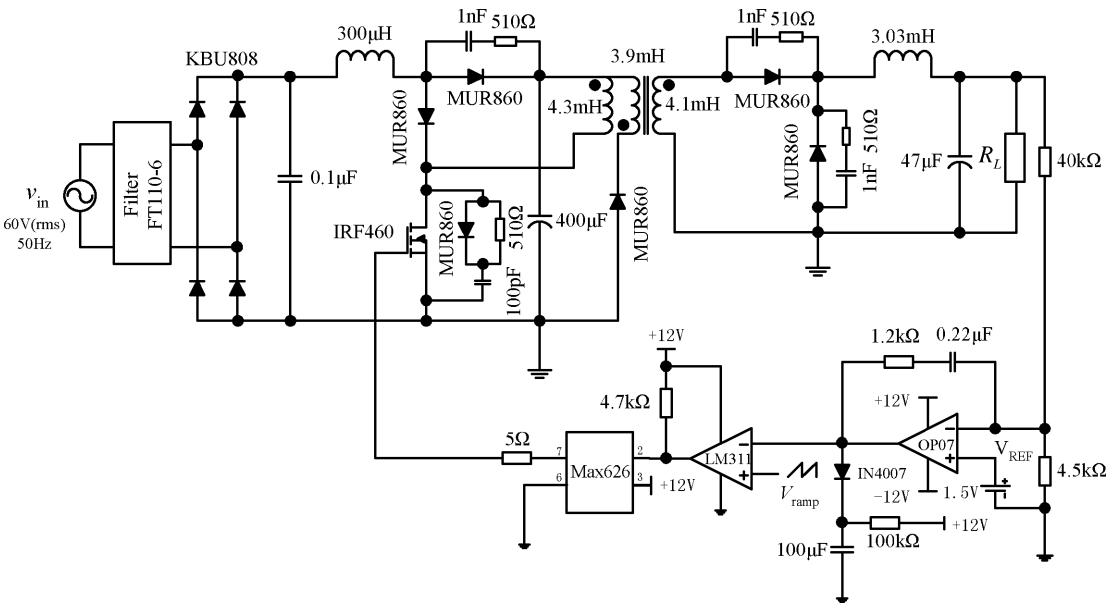
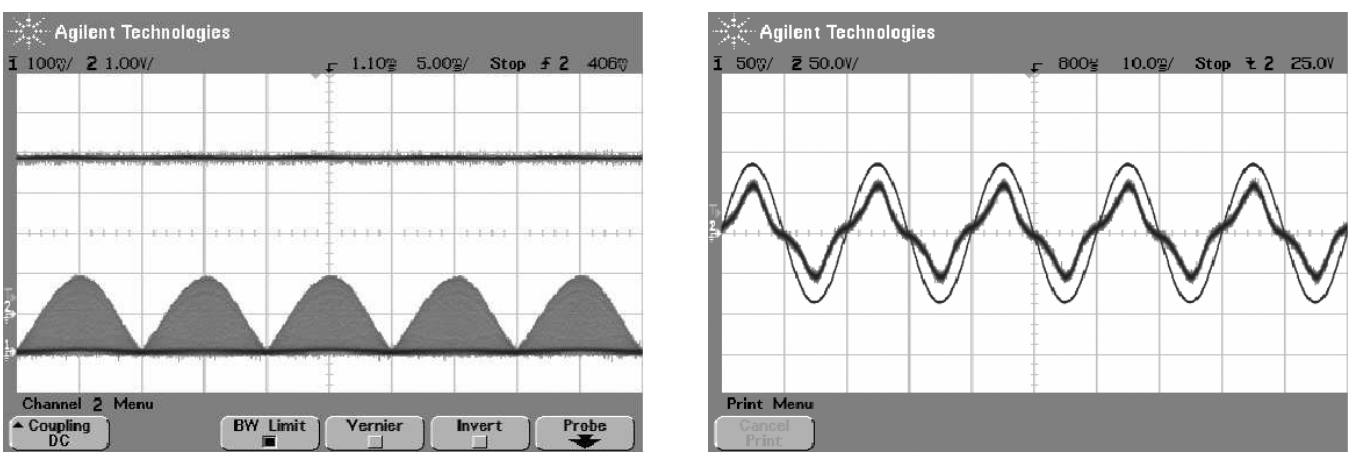
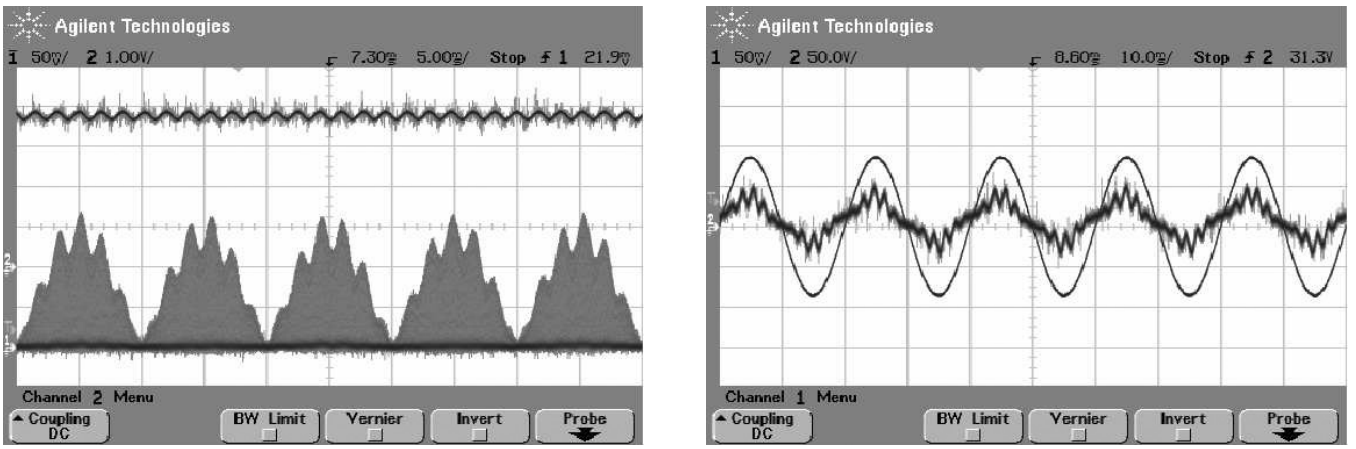


Fig. 11. Full schematic diagram of experimental circuit.



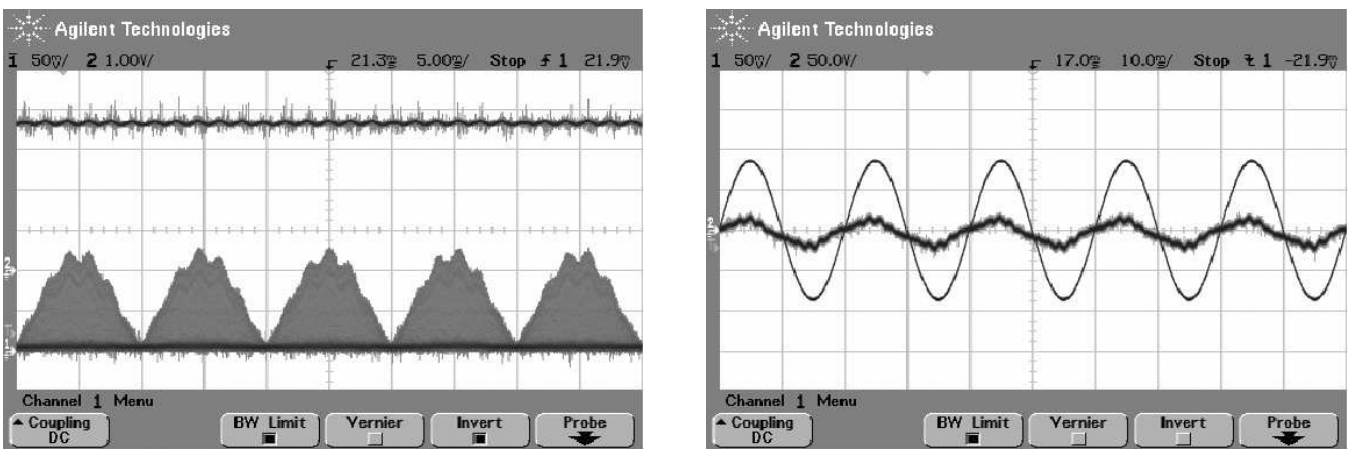
(a) (b)

Fig. 12. Measured waveforms for $R = 15.7\,\Omega$ with current probe (10 mV/A). (a) Upper trace: control voltage (1 V/div), lower trace: current of L_1 (100 mV/div), time scale: 5 ms/div; (b) mains input voltage (50 V/div) and input current (50 mV/div), time scale: 10 ms/div.



(a) (b)

Fig. 13. Measured waveforms for $R = 30.3\,\Omega$ with current probe (10 mV/A). (a) Upper trace: control voltage (1 V/div), lower trace: current of L_1 (50 mV/div), time scale: 5 ms/div; (b) mains input voltage (50 V/div) and input current (50 mV/div), time scale: 10 ms/div.



(a) (b)

Fig. 14. Measured waveforms for $R = 57.9\,\Omega$ with current probe (10 mV/A). (a) Upper trace: control voltage (1 V/div), lower trace: current of L_1 (50 mV/div), time scale: 5 ms/div; (b) mains input voltage (50 V/div) and input current (50 mV/div), time scale: 10 ms/div.

operation. Figure 12(a) shows the control voltage and the current of L_1. It can be clearly observed that the control voltage is approximately constant. Figure 12(b) shows the input current and voltage.

Figure 13 presents the measured waveforms for $R = 30.3\,\Omega$. In this case, the intermediate-scale instability can be observed from the seriously oscillating waveforms of the control voltage and the current of L_1, as shown in Fig. 13(a). Moreover, the input current and voltage are both shown in Fig. 13(b), from which we can observe a serious distortion of the input current.

Figure 14 shows the measured waveforms for $R = 57.9\,\Omega$. As predicted, the intermediate-scale instability will become "weak" for lower output power. Figure 14(a) shows the control voltage and the current of L_1. Compared with those shown in Fig. 13(a), the amplitudes of the control voltage and the current of L_1 are attenuated. Nonetheless, the intermediate-scale instability can be readily observed. The input current and voltage are further presented in Fig. 14(b), which shows a weakened distortion of the input current.

7. Conclusion

Power factor correction has become a primary design requirement for switching power supplies.

For low power applications, the SSIPP is a cost effective solution which is widely used in practice. Although the steady-state design and control of the SSIPP have been thoroughly studied for many years, the detailed dynamics of this system, so far, has not been completely explored or well understood. In this paper, the intermediate-scale instability of an SSIPP operating DCM boost stage and CCM forward stage has been reported. We have reported the results from "exact" cycle-by-cycle circuit simulations, and have discussed the adverse effects of the intermediate-scale instability on power factor. Furthermore, it has been found that such instability is essentially caused by Hopf bifurcation of the regulating stage. Analytical expressions that define the normal operation boundary have been derived. Finally, an experimental circuit prototype has been built to verify the observations made from simulations. Since the intermediate-scale instability can greatly affect power factor and harmonic distortion, the results obtained here will be useful to the design of sing-stage PFC power supplies.

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Appendix A

Calculation of Storage Capacitor Voltage Stress

In the steady state, the voltage V_C across the storage capacitor can be determined by equating the energy absorbed from the ac line during a half line cycle with the energy delivered to the load during the same half line cycle. Thus, the energy equality can be written as

$$\int_0^{T_{\rm L}/2} v_{\rm in} i_{\rm in} dt = \frac{1}{2} V_o I_o T_{\rm L} \tag{A.1}$$

where $i_{\rm in}$ is the input current from the ac line and I_o is the output current upon the load at steady state. Since $i_{\rm in} = i_1$, the above equation can be rewritten as

$$\int_0^{T_{\rm L}/2} v_{\rm in} i_1 dt = \frac{1}{2} V_o I_o T_{\rm L}. \tag{A.2}$$

As indicated in Fig. 3, we denote the on-time of switch S and diode $D_1$by D_1T and D_2T, respectively. By inspection of the waveforms shown in Fig. 3, D_2 can be represented by D_1 as follows:

$$D_2 = \frac{v_{\rm in}}{V_C - v_{\rm in}} D_1. \tag{A.3}$$

Furthermore, the averaged i_1 over the switching cycle is given by

$$\overline{i_1} = \frac{T}{2L_1} D_1 (D_1 + D_2) v_{\rm in} \tag{A.4}$$

$$= \frac{T D_1^2}{2L_1} \frac{v_{\rm in} V_C}{V_C - v_{\rm in}}. \tag{A.5}$$

Since $T \ll T_{\rm L}$ for most practical applications, we have

$$\int_0^{T_{\rm L}/2} v_{\rm in} i_1 dt \approx \int_0^{T_{\rm L}/2} v_{\rm in} \overline{i_1} dt \tag{A.6}$$

$$= \frac{V_C T D_1^2}{2L_1} \int_0^{T_{\rm L}/2} \frac{v_{\rm in}^2}{V_C - v_{\rm in}} dt. \tag{A.7}$$

For the forward output regulator operating in CCM, we can easily get

$$V_o I_o = \frac{D_1^2 V_C^2}{R}. \tag{A.8}$$

Hence, substituting both (A.6) and (A.8) into (A.2) yields

$$\int_0^{T_{\rm L}/2} \frac{v_{\rm in}^2}{V_C - v_{\rm in}} dt = \frac{L_1 T_{\rm L} V_C}{RT} \tag{A.9}$$

from which V_C can be numerically obtained.

Appendix B

Stability Condition for the Load-Side Buck Converter

For the buck converter shown in Fig. 9, the averaged model can be represented by the averaged equations

$$\frac{di}{dt} = -\frac{v}{L_2} + \frac{dV_C}{L_2} \tag{A.10}$$

$$\frac{dv}{dt} = \frac{i}{C_2} - \frac{v}{\tau} \tag{A.11}$$

$$\frac{dv_{\rm con}}{dt} = -\frac{Ki}{C_2} + \left(\frac{1}{\tau} - \frac{1}{\tau_F}\right) Kv + \frac{KV_{\rm ref}}{\tau_F} \left(1 + \frac{R_1}{R_2}\right) \tag{A.12}$$

where d is the duty cycle and can be easily given by

$$d = \frac{v_{\rm con} - V_L}{V_U - V_L}. \tag{A.13}$$

It is worth pointing out here that the averaged equations are valid only when $0 < d < 1$. Such a condition is satisfied when the system is operating in the stable equilibrium state.

The equilibrium point of the averaged equations can be calculated by setting all time-derivatives of (A.10)–(A.12) to zero and solving for i, v and $v_{\rm con}$. This gives the equilibrium point X_0 to be

$$\begin{bmatrix} \dfrac{D_0 V_C}{R} \\ D_0 V_C \\ V_L + D_0 (V_U - V_L) \end{bmatrix} \tag{A.14}$$

where

$$D_0 = \frac{V_{\rm ref}}{V_C} \left(1 + \frac{R_1}{R_2}\right). \tag{A.15}$$

It is well known that the stability of this equilibrium point is determined by the eigenvalues of the system's Jacobian at the equilibrium point. The standard procedure is to solve the following equation

for λ:

$$\det[\lambda I - J(X_0)] = 0. \tag{A.16}$$

Upon expanding, we get

$$a_0\lambda^3 + a_1\lambda^2 + a_2\lambda + a_3 = 0 \tag{A.17}$$

where $a_0 = 1$, $a_1 = 1/\tau$, $a_2 = (1/L_2C_2) + (KV_C/L_2C_2(V_U - V_L))$, and $a_3 = KV_C/L_2C_2\tau_F(V_U - V_L)$. Then, we may generate the so-called *Routh Table* associated with the polynomial (A.17), i.e.

$$\begin{array}{ll} 1 & a_2 \\ a_1 & a_3 \\ a_2 - \dfrac{a_3}{a_1} & \\ a_3 & \end{array} \tag{A.18}$$

The Routh–Hurwitz criterion states that all of the roots of the characteristic polynomial have real parts strictly less than zero if, and only if, all elements in the first column of the *Routh Table* are nonzero and have the same sign [Wiggins, 2003]. Since $a_i > 0$ $(i = 0, 1, 2, 3)$ here, applying the Routh–Hurwitz criterion, we can easily get the critical stability condition for the equilibrium point as $a_1a_2 = a_3$, which can be written as

$$K = \frac{\tau_F(V_U - V_L)}{V_C(\tau - \tau_F)}. \tag{A.19}$$