Integrated Adaptive DC/DC Conversion with Adaptive Pulse-Train Technique for Low-Ripple Fast-Response Regulation

Chuang Zhang
Electrical & Computer Engineering Dept.,
Louisiana State University
Baton Rouge, LA 70803
1-225-334-5048
Czhang5@lsu.edu

Dongsheng Ma
Electrical & Computer Engineering Dept.,
University of Arizona
Tucson, AZ 85721
1-520-621-6193
Ma@ece.arizona.edu

Ashok Srivastava
Electrical & Computer Engineering Dept.,
Louisiana State University
Baton Rouge, LA 70803
1-225-578-5622
Ashok@ece.lsu.edu

ABSTRACT

Dynamic voltage scaling (DVS) is a very effective low-power design technique in modern digital IC systems. On-chip adaptive DC/DC converter, which provides adjustable output voltage, is a key component in implementing DVS-enabled system. This paper presents a new adaptive DC/DC converter design, which adopts a delay-line controller for voltage regulation. With a proposed adaptive pulse-train technique, ripple voltages are reduced by 50%, while the converter still maintains satisfying transient response. With a supply voltage of 3.3V, the output of the converter is well regulated from 1.7 to 3.0V. Power consumption of the controller is below 100μW. Maximum efficiency of 92% is achieved with output power of 125mW. Chip area is 0.8 x 1.2mm^2 in 1.5μm standard CMOS process.

Categories and Subject Descriptors

B.7.1 **[Types and Design Styles]** [**Programming Languages**]

General Terms

Management, Performance, Design

Keywords

Adaptive output, DC/DC conversion, low ripple, transient response, adaptive pulse-train technique.

1. INTRODUCTION

With the proliferation of battery-operated portable devices such as personal digital assistants (PDAs) and cell phones, low power integrated circuits are highly desirable.

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Reducing supply voltage to reduce power consumption is widely accepted in low-power IC designs [1-4]. When system is not in its peak performance, lowering supply voltage can save much dynamic power, which shows quadratic dependence on supply voltage V_{DD}. In [4], a dynamic voltage scaling (DVS) method is applied to a processor system to satisfy both the performance and power consumption design targets. Adaptive supply voltage can also be used to compensate processing variations [5] to reduce the leakage currents and improve the reliability.

DC/DC converter is found out to be the best solution in adaptive supply voltage generation [6-9]. Recently digitally controlled DC/DC converter has drawn wide attentions due to its fast response, low power consumption and compatibility with standard digital CMOS processes [7]. Many existing implementations of digital controller need high-resolution, high-speed analog to digital (A/D) converter, which occupies large chip area and consumes significant power. The A/D converter samples and converts the regulated output voltage into digital signals in feed back loop to determine the duty ratio of the DC/DC converter. Its bandwidth limits the overall dynamic response of the power converter. Delay-line based controllers reported in [8, 9] transform voltage signal into frequency signal, and use digital signal processing circuits for voltage regulation. Power consumption of delay-line can be much lower than A/D converter implementations [10].

For improved performance and better control, a pulse-train technique is proposed in [10]. By adopting a pulse train instead of a constant pulse as a gate control signal of switches, the converter successfully avoids over-charging or -discharging of the inductor during transition. Resolution of the control is thus improved with smaller output ripple voltages. The details will be described in Section 3. However, the pulse-train technique slows down the transient response, since the converter takes a longer time to deliver the energy to the loads.

In this paper, an adaptive pulse-train technique is proposed which is incorporated in delay-line controller for the low ripple and fast transient response. An internal control signal can enable pulse-train function for high-resolution regulation in steady mode and disable it for the fast dynamic response in transient mode. The

paper is organized as follows. In Section 2, a new delay-line based controller is proposed. Operation of the adaptive DC/DC converter is described. The relation of frequency to output voltage is obtained. Section 3 discusses details of proposed adaptive pulse-train technique. Both advantages and disadvantages of the technique are addressed and verified by post-layout HSPICE simulations. Finally, we conclude our results in Section 4.

2. DC/DC CONVERTER WITH DELAY-LINE BASED CONTROLLER

Delay-line controller is used to replace traditional A/D converter due to its simplicity and low power consumption. However, complex auxiliary logic associated with delay-line may occupy large chip area and increase power consumption. In [8], a look-up table is needed to process error signal. The look-up is stored in external memory which is unwanted in integrated design. In [9], a large number of S-R latches and flip/flops are used to implement digital control law. In this work, a simple controller is designed which consists of delay-line, a few logic gates and adaptive pulse-train technique. Figure 1 depicts the block diagram of a delay-line based DC/DC converter. The converter consists of a power stage, a delay-line based digital controller to control the duty ratios of the switches in the power stage and a reference clock.

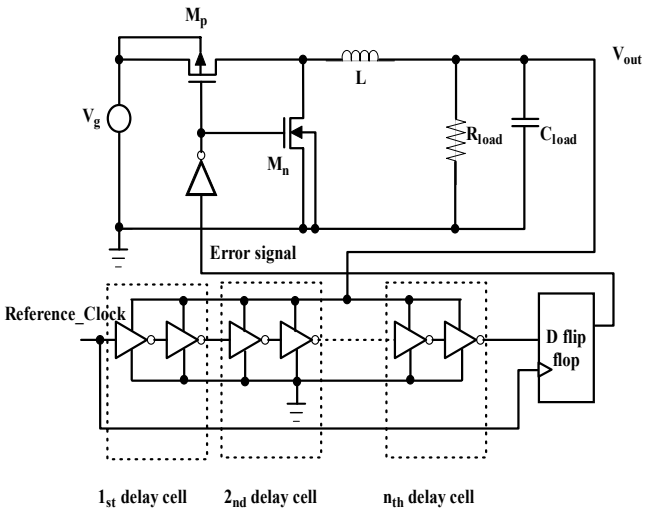

Figure 1. Schematic of a delay-line based DC/DC converter.

The delay-line is powered by the output voltage of the converter and used to detect variations in the output. Its propagation delay t_d is, thus, inversely proportional to output voltage V_{out}. First order relation is expressed as

$$t_d = \frac{2nKV_{out}}{(V_{out} - V_{th})^2}, \qquad (1)$$

where V_{th} is the threshold voltage of the transistors, n presents the number of stages in the delay line and K is a constant parameter related to the fabrication process. The propagation delay increases as V_{out} decreases. A linear relation is observed when V_{DD} is much higher than V_{th}. The resolution of delay line is determined by the number of the stages n. Larger number of stages in the delay-line give more accurate measure on variations of V_{out}. In this work, twenty-stage delay line is employed, which can differentiate a minimum voltage variation of 15mV at $V_{out.}$ When the reference clock is applied, it passes through the 20-stage delay line (each delay stage consists of two inverter cells) and is sampled at output of the 20^{th} stage at a fixed sampling rate of $1/T_{20}$. The propagation delay t_d is determined by its supply voltage V_{out}. When V_{out} decreases, t_d of the delay line increases accordingly. Thus, after T_{20}, the falling edge of the clock signal does not reach the 20^{th} delay stage, as shown in Fig. 2(a). The output of the 20th stages keeps its initial value, "1", to charge the inductor in power stage and increase the supply voltage. On the other hand, when V_{out} increases, t_d of the delay line decreases. Thus, after T_{20}, the falling edge of reference clock has passed the 20^{th} delay stage as shown in Fig. 2(b). The output of the 20^{th} stages becomes "0", to discharge inductor in power stage and decreases the supply voltage. Thus, the output voltage will be regulated at the desired level with small ripple voltages.

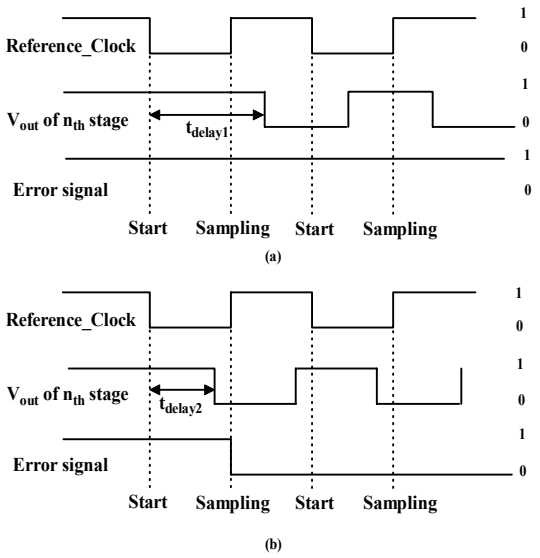

Figure 2. Timing diagrams of the converter (a) when V_{out} is too low, and (b) when V_{out} is too high.

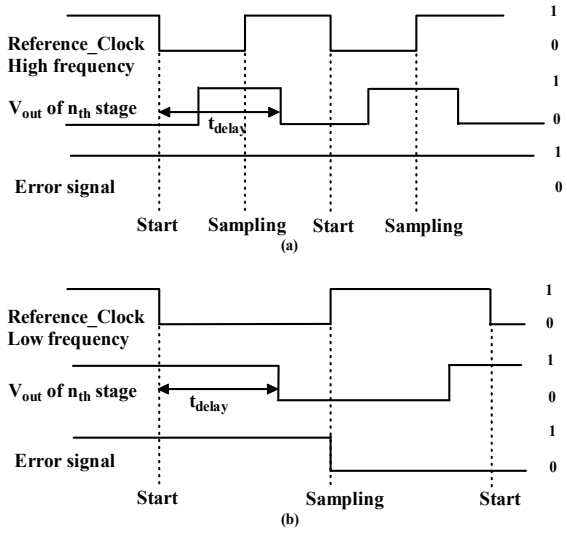

Figure 3. Timing diagram of the converter (a) when reference clock frequency increases, and (b) when reference clock frequency decreases.

On the other hand, the converter can also be regulated by a variable reference clock signal. Figure 3 shows the timing diagram of DC/DC converter in this case. Higher frequency is associated with longer duty ratio of the converter, while low frequency is associated with a shorter one. So the DC/DC converter is frequency-adaptive. Figure 4 shows the relation of V_{out} to the reference clock frequency.

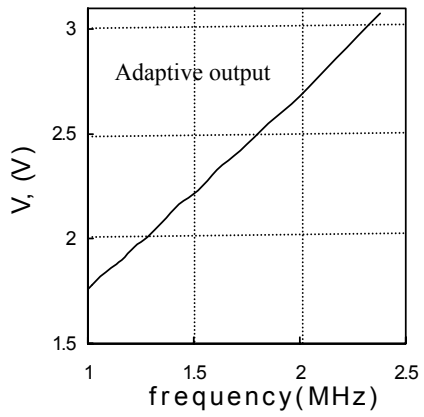

Figure 4. Adaptive output voltage versus reference clock frequency.

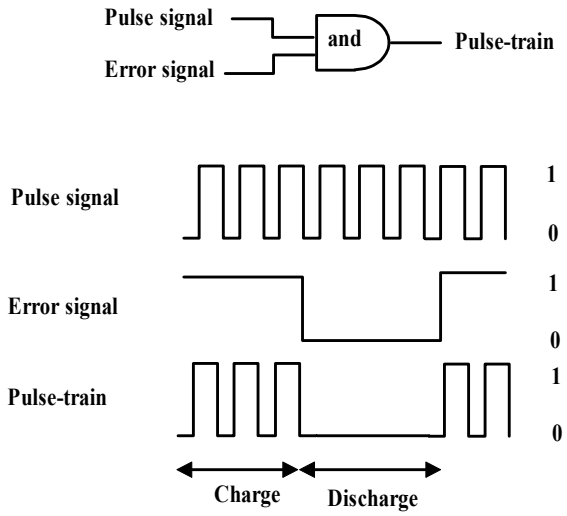

Figure 5. Illustration of pulse-train error signal.

3. PROPOSED ADPTIVE PULSE-TRAIN TECHNIQUE

The original pulse-train technique was proposed in [9]. Its concept can be illustrated by Fig. 5. Now, the duty ratio signal (or called as error signal) of the converter is modulated by a pulse train through an AND gate. As a result, the pulse train signals charge and discharge the inductor in the power stage in finer steps. Charging procedure is completed by a few pulses instead of one single period. It reduces high-peak inductor current and overcharging, thus lowers the ripples at the output voltage V_{out}. In addition, complexity of design remains almost unchanged, since only a few logic gates are added. However, this pulse-train technique extends the transient response time (from 50 μS to 100 μS) as shown in Fig. 6, since a longer charging period is required to deliver enough current to the load, which greatly degrades the dynamic performance of the adaptive converter.

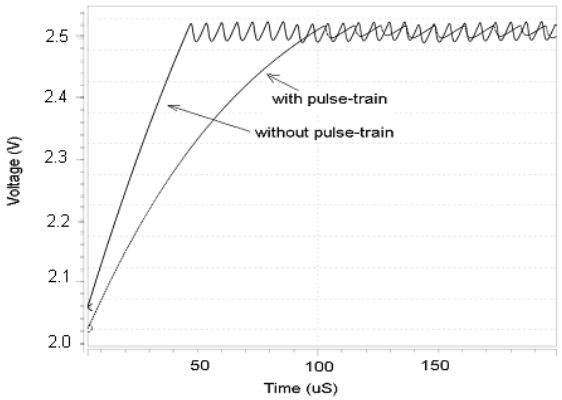

Figure 6. Transient response of a converter with and without pulse-train technique.

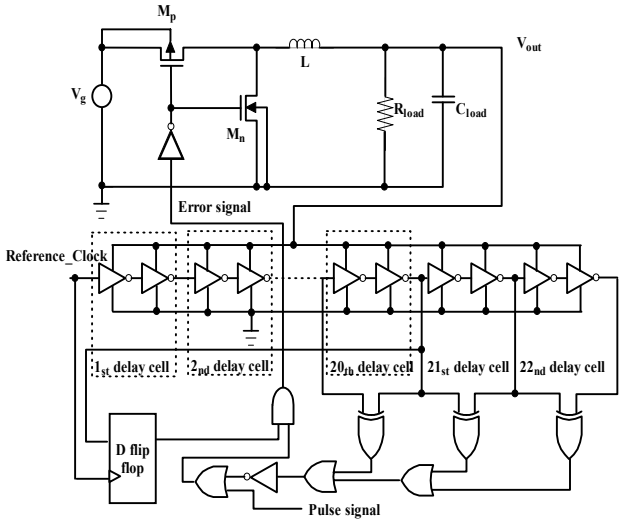

Figure 7. Circuit diagram of a DC/DC converter using adaptive pulse-train technique.

An adaptive pulse-train technique is thus proposed for the fast transience. The circuit diagram is shown in Fig. 7. The technique allows the converter to operate in two different operation modes: transient mode for fast response and steady mode for small ripple voltage. Three XORs are used to detect the falling edge of reference clock. If the falling edge is detected at output of 19^{th}, 20^{th} or 21^{st}, it means that output is very close to its destined value and output voltage is at quasi-steady mode. In quasi-steady mode, pulse-train is enabled to give slow charging and small ripple. If the falling edge is out of detectable range, it means that it is in transient mode. In transient mode, pulse-train is disabled and controller could give large charging current to enhanced transient response. Figure 8 shows post-layout simulations of transient response with traditional pulse-train technique and proposed adaptive pulse-train technique. It is seen that adaptive pulse-train reduced transient response time by 50 % and keeps output ripple low.

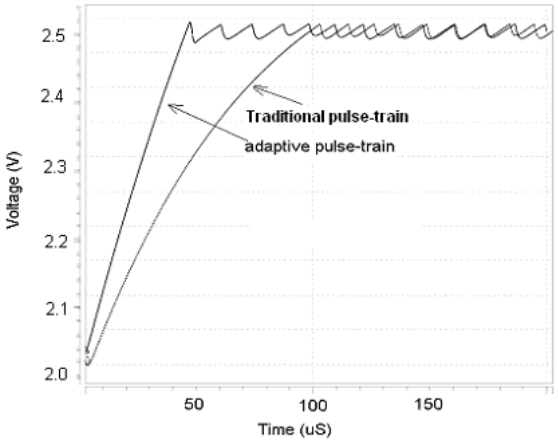

Figure 8. Transient response of output voltage using adaptive pulse-train technique.

In this research, the duty ratio of pulse is determined by ratio of V_{out}/V_g and is generated by the circuitry in Fig. 9. Output voltage is compared with an external ramp signal. Duty ratio is determined by the trip point. Higher output voltage gives high duty ratio. Amplitude of ramp, V_{ramp}, is set slightly lower than V_g (V_{ramp} = 3 V in the design) so that the duty ratio is high enough to charge up output voltage.

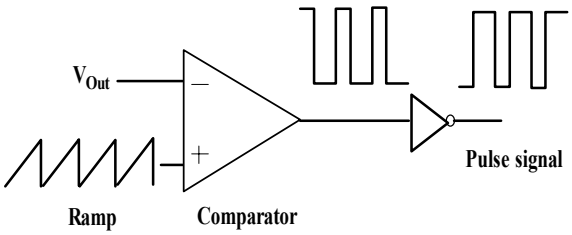

Figure 9. Block diagram of pulse width modulation circuit.

Figure 10 shows that the output ripple voltage decreases as the number of pulses increases in the charging phase when M_p in Fig. 1 is turned on. Pulse frequency of 2 MHz is selected which ensure 10 pulses in a single charging phase. Figure 11 shows the regulated output voltage with a pulse frequency of 2 MHz. Frequency of reference clock is 1.8 MHz. Figure 11 shows that the pulse-train technique reduces ripple by 50 %, giving output voltage ripple of 18 mV. The reduction of ripple is due to low charging current which is shown in Fig. 12.

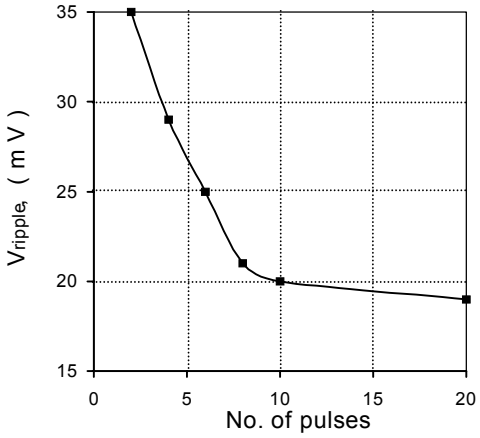

Figure 10. Ripple voltage versus number of pulses in one switching cycle.

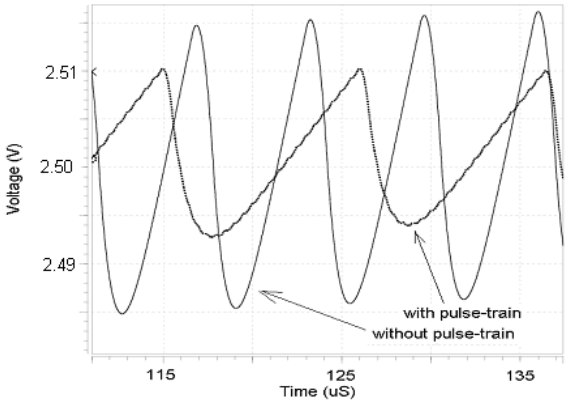

Figure 11. Output voltage ripple with and without pulse-train technique.

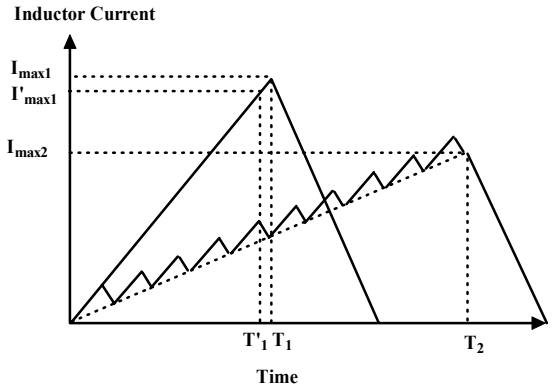

Figure 12. Inductor current of the converter with and without pulse-train technique in steady state (only the charging phase is shown).

The current in inductor charges and discharges load capacitor. The capacitor does not dissipate energy, so average current is zero. Variation of charges in capacitor causes output voltage ripple. Ripple in the delay-line controller DC/DC converter is given by

$$V_{ripple} = \frac{I'_{\max} T'}{2C_{load}} + \frac{I'_{\max} t_{loop}}{C_{load}}. \quad (2)$$

In Eq. (2), I'_{max} is ideal maximum charging current in capacitor without considering delay of feedback loop. T' is ideal charging time and t_{loop} is delay of feedback loop and is equal to $T_1 - T_1'$. The first term is system ripple determined by resolution of delay-line controller. The second term is determined by maximum charging current.

The maximum charging current without pulse-train technique is expressed as

$$I'_{\max 1} \approx I_{\max 1} = T_1 \frac{V_g - V_{out}}{L}, \quad (3)$$

where T_1 is the charging time and L is inductance. The maximum charging current with pulse-train technique is given by,

$$I_{\max 2} = T_2 \left[\frac{V_g - V_{out}}{L} D - \frac{V_{out}}{L}(1-D) \right]. \quad (4)$$

Further simplifying Eq. (4), we obtain,

$$I_{\max 2} = \frac{T_2 V_{out}}{L} \left(\frac{V_g}{V_{out}} D - 1 \right) \quad (5)$$

where T_2 is charging time in a single charging phase with pulse-train technique. D is the duty ratio of pulse. In Eq. (5), if D = 1, pulse-train technique does not apply. If $D = V_{out}/V_g$, maximum current will be zero. The duty ratio is set to about 10% higher than V_{out}/V_g as generated by circuit in Fig. 9. The duty ratio ensures a low maximum charging current.

In real situation, there is always equivalent series resistance (ESR) connected with the output capacitor, C_{load}. It exaggerates ripples of output voltage as shown in Fig. 13. With adaptive pulse-train technique, low ripples are still obtained. The jaw-saw shapes in output voltage of Fig. 13 using adaptive pulse-train control reflect finer charging steps in a single charging phase. The ripple is reduced to 22 from 36mV. Benefiting from low power consumption of the digital controller, maximum efficiency of 92% is achieved when the converter is regulated at 2.5V, with an output power of 125mW. The inductor (L) and capacitor (C_{load}) of DC-DC converter are 4.7µH and 10µF, respectively.

Results presented in this paper are obtained from post-layout simulations using models BSIM 3 Level 49 MOS Model parameters in HSPICE. The layout area is 0.8 x 1.2 mm^2 using 1.5 µm standard two-metal, two-poly, digital CMOS process and is shown in Fig. 14. Design in [8] without external memory occupies 1 x 1mm^2 silicon area in 0.5 µm CMOS technology. Design in [7] takes 1.1 x 1.3mm^2 area in 0.25µm CMOS technology. Compared with [7] and [8], present work uses reduced area.

3. SUMMARY

An adaptive high efficiency DC/DC converter is designed which is based on a low power delay-line controller and adaptive pulse-train technique. The power consumption of controller is less than 100µW, which is much lower than the traditional controller. Maximum power efficiency of 92% is obtained with output power of 125mW. The controller operates in two modes: transient mode and quasi-steady mode. Adaptive pulse-train technique enables pulse-train technique in steady mode for low current charging thus reduces output ripple voltage. The output ripple is reduced by 50%. The pulse-train is disabled in transient mode keeping high transient response. Compared with traditional pulse-train technique, response time is reduced by 50% in transient mode where high transient speed is highly desirable. An equivalent series resistor, 100mΩ, is also added for post layout simulation. The adaptive pulse-train technique keeps its ripple below 22mV. With a supply voltage V_g of 3.3V, the output is regulated over range of 1.7 to 3.0V.

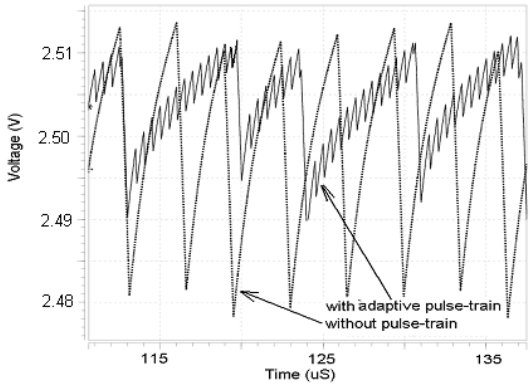

Figure 13. Ripple of output voltage with ESR.

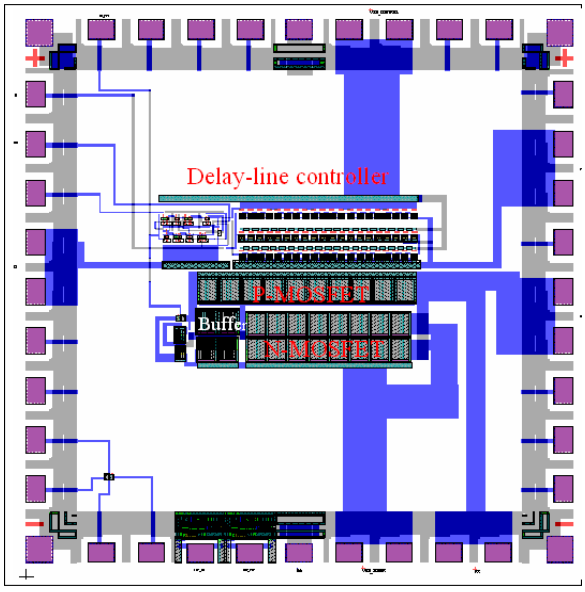

Figure 14. Layout of an adaptive DC/DC converter using delay-line based controller and adaptive pulse-train technique.

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